

# PHT4NQ10LT

## N-channel TrenchMOS logic level FET

Rev. 2 — 28 October 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Logic level compatible

### 1.3 Applications

- DC-to-DC converters
- High-speed line drivers
- General purpose switching

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 2</a>	-	-	3.5	A
$V_{GS}$	gate-source voltage		-16	-	16	V
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 1.75\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	200	250	mΩ

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	<p>SOT223 (SC-73)</p>	<p>mbb076 S</p>
2	D	drain		
3	S	source		
4	D	drain		



### 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHT4NQ10LT	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

### 4. Marking

Table 4. Marking codes

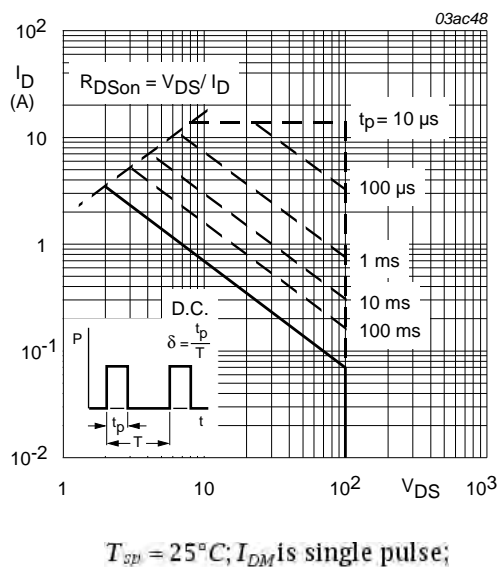
Type number	Marking code
PHT4NQ10LT	4NQ10L

### 5. Limiting values

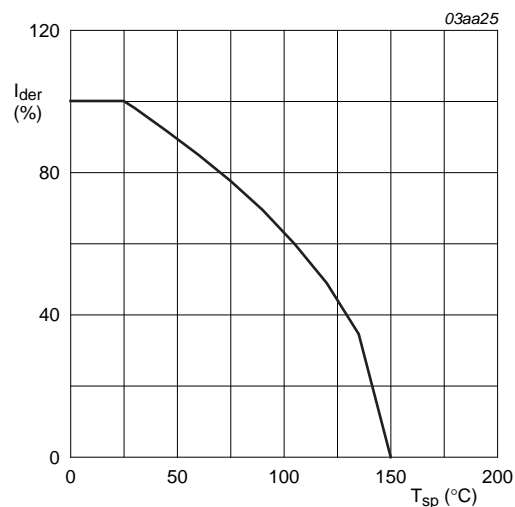
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

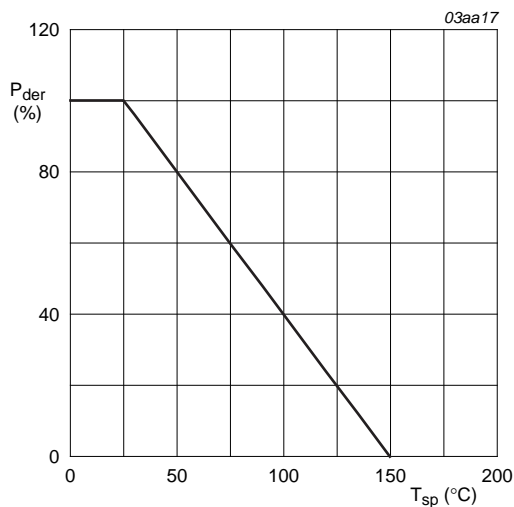
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 150\text{ }^{\circ}\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 150\text{ }^{\circ}\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-16	16	V
$I_D$	drain current	$T_{sp} = 100\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$	-	2.2	A
		$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 2</a>	-	3.5	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 1</a>	-	14	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 3</a>	-	6.9	W
$T_{stg}$	storage temperature		-65	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-65	150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	3.5	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	14	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 5\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; $I_D = 3.5\text{ A}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{sup} \leq 15\text{ V}$ ; unclamped; $t_p = 0.2\text{ ms}$ ; see <a href="#">Figure 4</a>	-	45	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 15\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; see <a href="#">Figure 4</a>	-	3.5	A



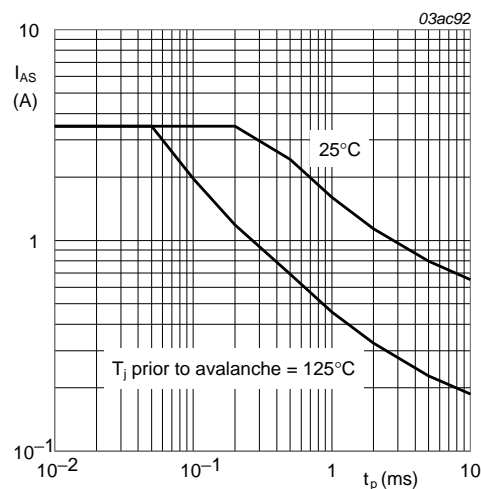
**Fig 1. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



**Fig 2. Normalized continuous drain current as a function of solder point temperature**



**Fig 3. Normalized total power dissipation as a function of solder point temperature**



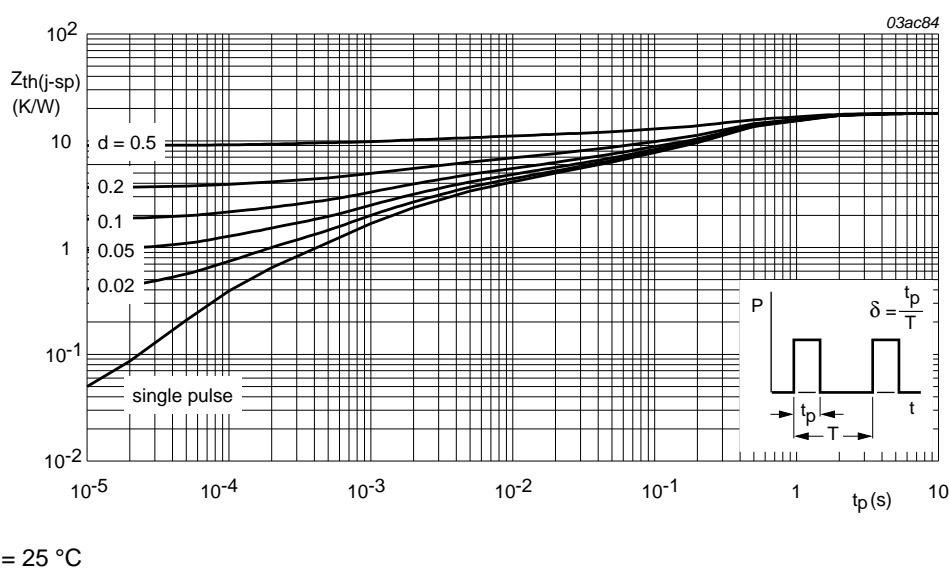
Unclamped inductive load;  $V_{DD} \leq 15$  V;  
 $R_{GS} = 50 \Omega$ ;  $V_{GS} = 5$  V; starting  $T_j = 25^\circ C$  and  $125^\circ C$ .

**Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration**

## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate	-	-	18	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board ; minimum footprint	-	-	150	K/W



$T_{sp} = 25\text{ °C}$

**Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration**

## 7. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = -55\text{ °C}$	89	-	-	V
		$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$	100	130	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150\text{ °C}$ ; see <a href="#">Figure 9</a>	0.6	-	-	V
		$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\text{ °C}$ ; see <a href="#">Figure 9</a>	-	-	2.3	V
		$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a>	1	-	2	V
$I_{GSS}$	gate leakage current	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$	-	10	100	nA
		$V_{GS} = 10\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$	-	10	100	nA

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 1.75 A; T <sub>j</sub> = 150 °C; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	-	575	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 1.75 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	200	250	mΩ
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 3.5 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	6.8	-	nC
Q <sub>GS</sub>	gate-source charge		-	1.1	-	nC
Q <sub>GD</sub>	gate-drain charge		-	3.6	-	nC
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 15 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C	-	4	-	ns
t <sub>r</sub>	rise time		-	10	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	52	-	ns
t <sub>f</sub>	fall time		-	21	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 3.5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	-	0.87	1.5	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 3.5 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C	-	50	-	ns
Q <sub>r</sub>	recovered charge		-	100	-	nC

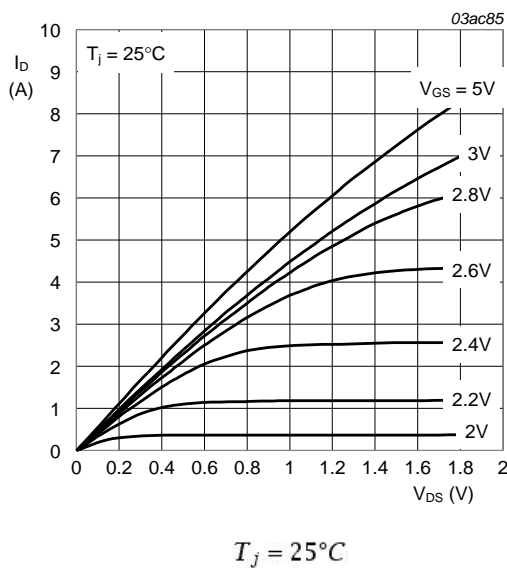


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

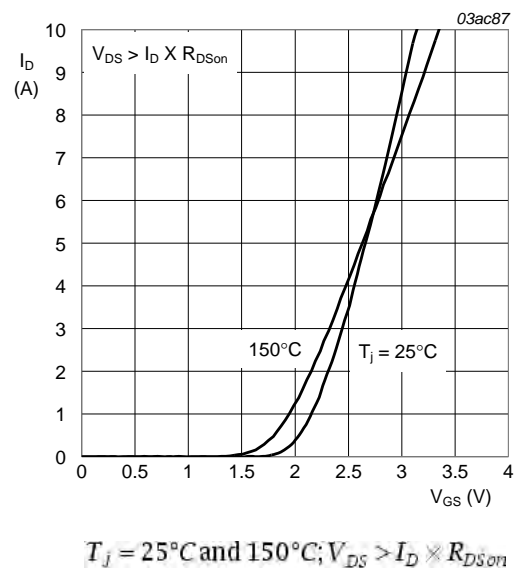


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

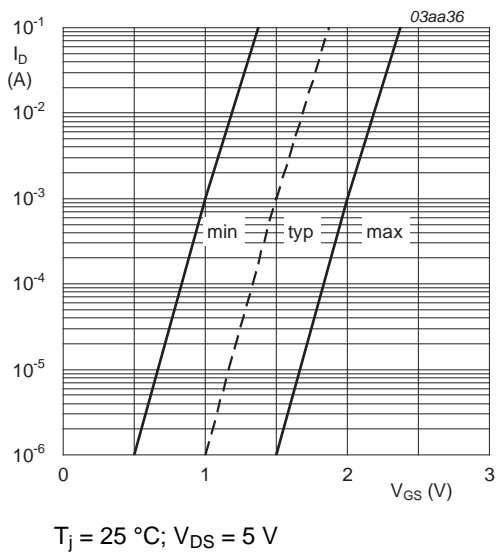


Fig 8. Sub-threshold drain current as a function of gate-source voltage

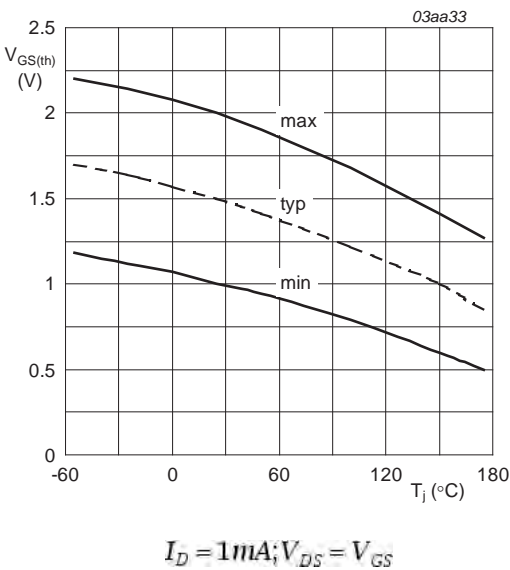


Fig 9. Gate-source threshold voltage as a function of junction temperature

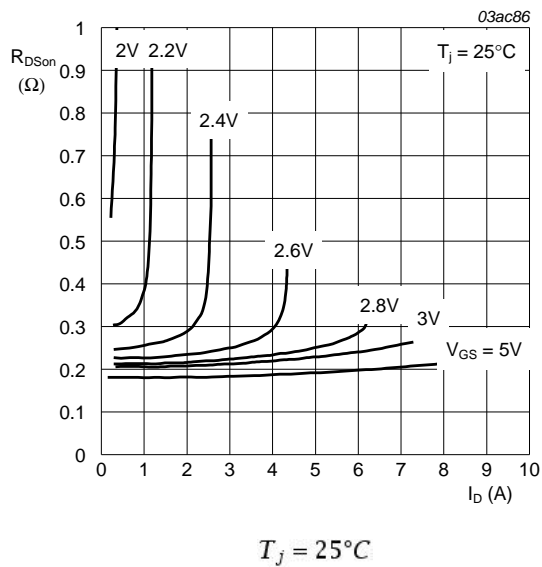


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

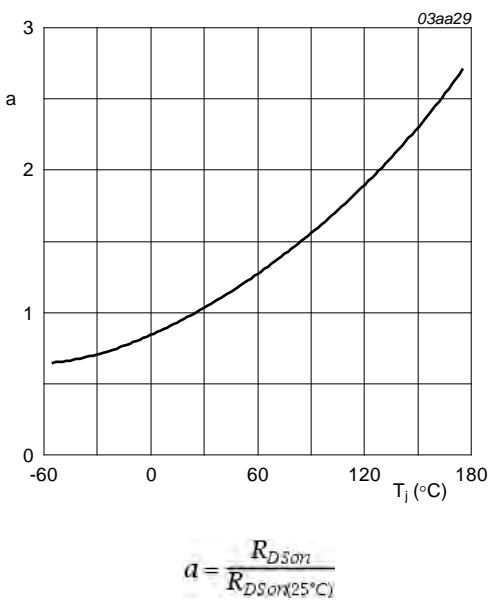


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

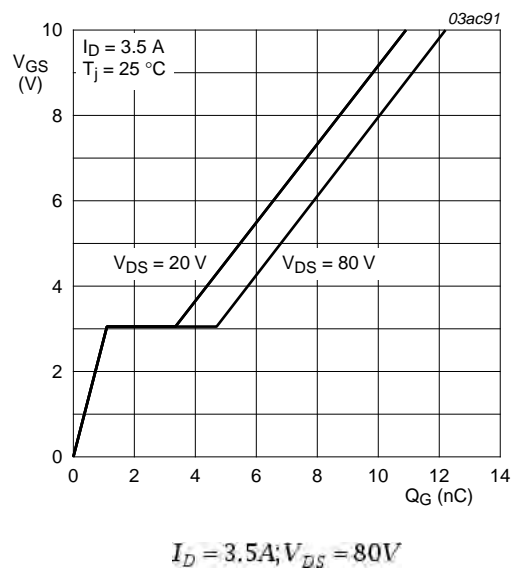


Fig 12. Gate-source voltage as a function of gate charge; typical values

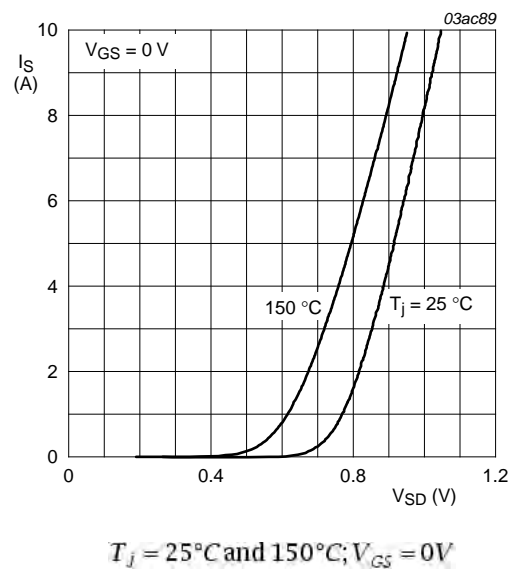


Fig 13. Source current as a function of source-drain voltage; typical values

8. Package outline

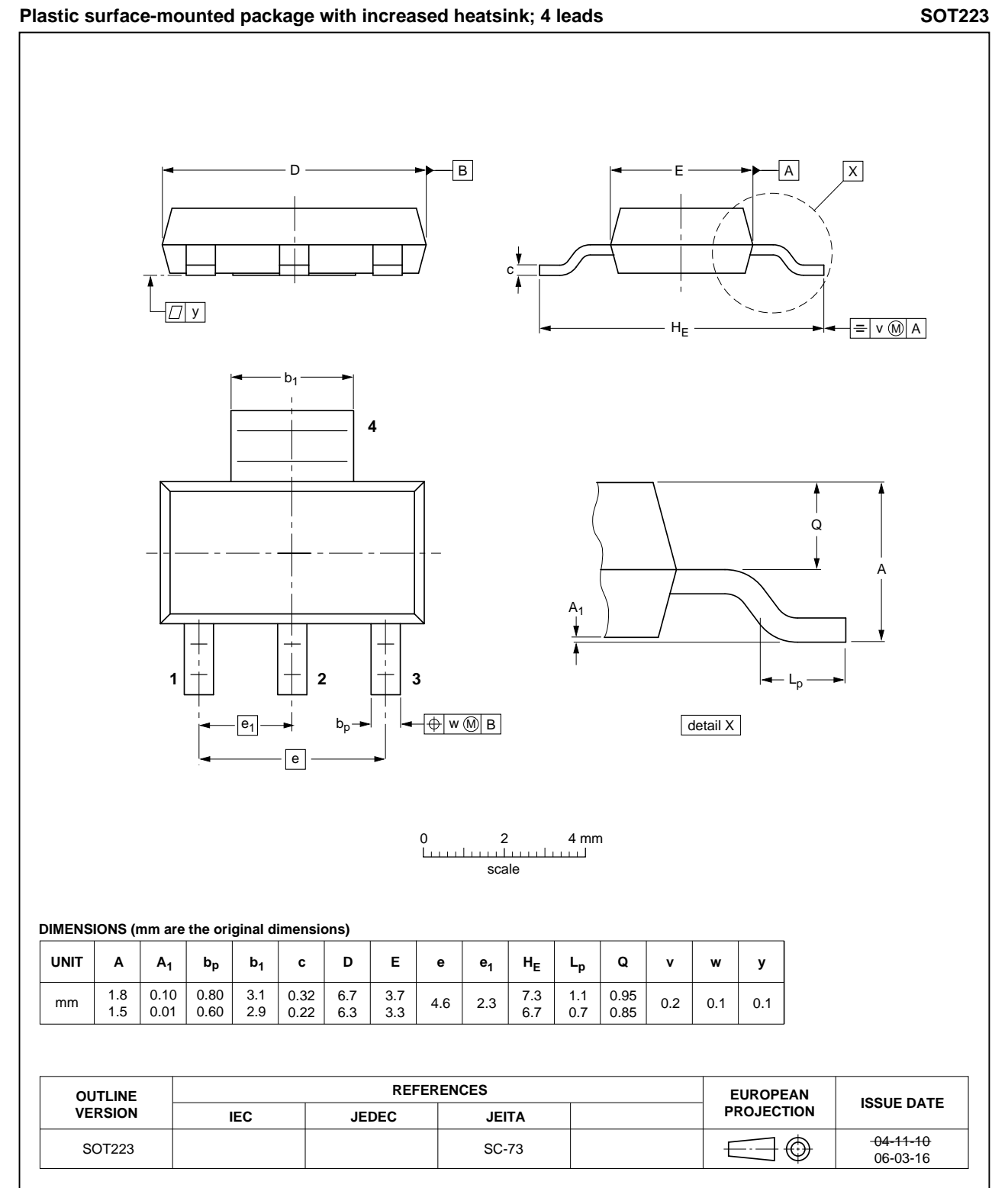


Fig 14. Package outline SOT223 (SC-73)



9. Soldering

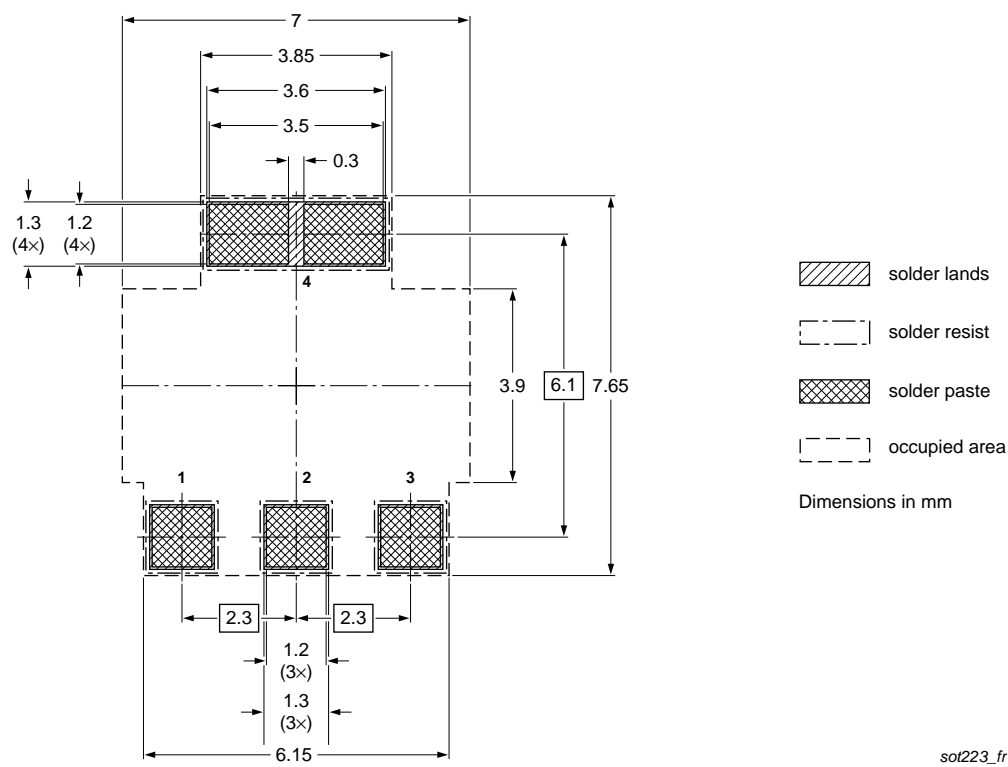


Fig 15. Reflow soldering footprint for SOT223 (SC-73)

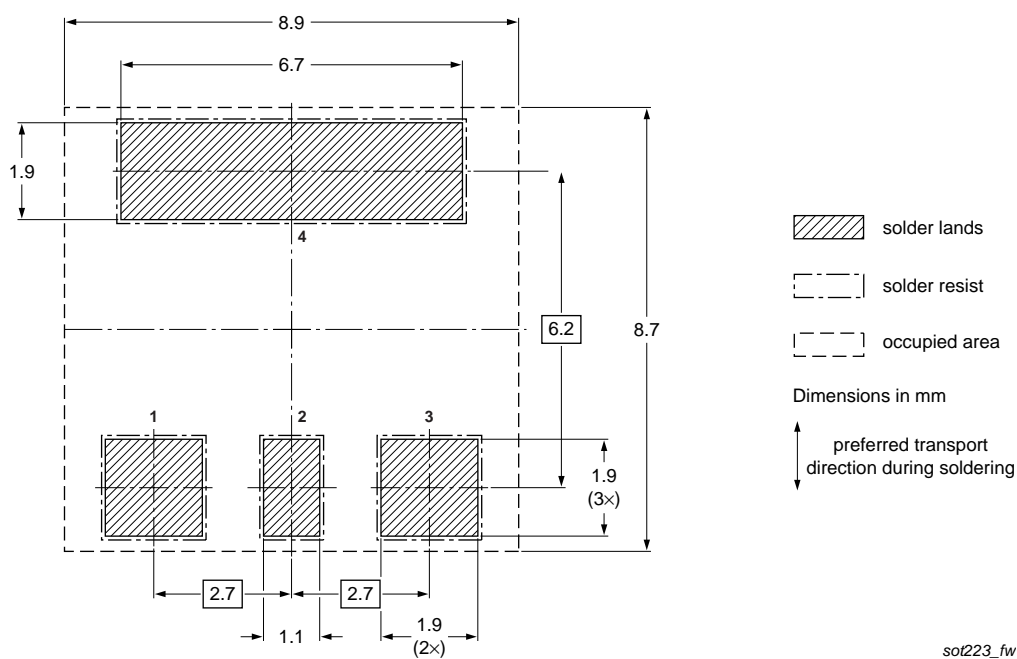


Fig 16. Wave soldering footprint for SOT223 (SC-73)

## 10. Revision history

**Table 8.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHT4NQ10LT v.2	20111028	Product data sheet	-	PHT4NQ10LT v.1
Modifications:	<ul style="list-style-type: none"><li>• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• <a href="#">1 "Product profile"</a>: updated</li><li>• <a href="#">7 "Characteristics"</a>: <math>Q_{G(tot)}</math> value corrected</li><li>• <a href="#">11 "Legal information"</a>: updated</li></ul>			
PHT4NQ10LT v.1	20000911	Product specification	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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