82541 Family of Gigabit Ethernet Controllers

Networking Silicon - 82541(PI/GI/EI)

Datasheet

Product Features

- PCI Bus
  - — PCI revision 2.3, 32-bit, 33/66 MHz
  - — Algorithms that optimally use advanced PCI, MWI, MRM, and MRL commands
  - — CLK_RUN# signal
  - — 3.3 V (5 V tolerant PCI signaling)
- MAC Specific
  - — Low-latency transmit and receive queues
  - — IEEE 802.3x-compliant flow-control support with software-controllable thresholds
  - — Caches up to 64 packet descriptors in a single burst
  - — Programmable host memory receive buffers (256 B to 16 KB) and cache line size (16 B to 256 B)
  - — Wide, optimized internal data path architecture
  - — 64 KB configurable Transmit and Receive FIFO buffers
- PHY Specific
  - — Integrated for 10/100/1000 Mb/s full- and half-duplex operation
  - — IEEE 802.3ab Auto-Negotiation and PHY compliance and compatibility
  - — State-of-the-art DSP architecture implements digital adaptive equalization, echo and cross-talk cancellation
  - — Automatic polarity detection
  - — Automatic detection of cable lengths and MDI vs. MDI-X cable at all speeds
- Host Off-Loading
  - — Transmit and receive IP, TCP, and UDP checksum off-loading capabilities
  - — Transmit TCP segmentation and advanced packed filtering
  - — IEEE 802.1Q VLAN tag insertion and stripping and packet filtering for up to 4096 VLAN tags
  - — Jumbo frame support up to 16 KB
  - — Intelligent Interrupt generation (multiple packets per interrupt)
- Manageability
  - — On-chip SMBus 2.0 port
  - — ASF 1.0 and 2.0
  - — Compliance with PCI Power Management v1.1/ACPI v2.0
  - — Wake on LAN* (WoL) support
  - — Smart Power Down mode when no signal is detected on the wire
  - — Power Save mode switches link speed from 1000 Mb/s down to 10 or 100 Mb/s when on battery power
- Additional Device
  - — Four programmable LED outputs
  - — On-chip power regulator control circuitry
  - — BIOS LAN Disable pin
  - — JTAG (IEEE 1149.1) Test Access Port built in silicon (3.3 V, 5 V tolerant PCI signaling)
- Lead-free[a] 196-pin Ball Grid Array (BGA). Devices that are lead-free are marked with a circled “e1” and have the product code: LUxxxxxx.

a. This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS)-banned materials, is available at: ftp://download.intel.com/design/packtech/material_content_IC_Package.pdf#pagemode=bookmarks
In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device.
For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative

318138-002
Revision 2.7

Revision History

Revision Date	Revision	Description
Aug 2002	0.25	• Initial Release.
Sep 2002	0.75	• Changed package diagram to molded plastic BGA. • Added DC/AC specifications. • Corrected pinout information.
Oct 2002	1.0	• Identified FIFO as 64 KB and verified ballout tables.
July 2003	1.5	• Added 82547GI coverage. • Signals CLKR_CAP and XTAL_CAP changed to RSVD_NC and NC, respectively.
Oct 2004	2.0	• Added Architecture Overview chapter. • Update signal names to match Design Guide and EEPROM Map and Programming Application Note.
Nov 2004	2.1	• Updated lead-free information. • Added information about migrating from a 2-layer 0.36 mm wide-trace substrate to a 2-layer 0.32 mm wide-trace substrate. Refer to the section on Package and Pinout Information. • Added statement that no changes to existing soldering processes are needed for the 2-layer 0.32 mm wide-trace substrate change in the section describing “Package Information”.
Jan 2005	2.2	• Added new maximum values for DC supply voltages on 1.2 V and 1.8 V pins. See Table 2, Recommended Operating Conditions and Table 6, DC Characteristics.
Apr 2005	2.3	• Corrected the FLSH_SO/LAN_DISABLE signal definition. If Flash functionality is not used then an external pull-down resistor is required.
June 2006	2.4	• Corrected the FLSH_SO/LAN_DISABLE signal definition. If Flash functionality is not used then an external pull-up resistor is required.
Aug 2006	2.5	• Removed note “b” from Table 2 and note “a” from Tables 3 and 4. • Moved the note following Table 5 before Table 3.
Aug 2007	2.6	• Replace Intel logo, updated the Product Features title page, and document ordering information.
Dec 2007	2.7	• Updated Section 3.3. Removed the internal pullup device text from the FLASH Serial Data Output / LAN Disable pin description.

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1.0 Introduction

The Intel® 82541(PI/GI/EI) Gigabit Ethernet is a single, compact component with an integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) functions. For desktop, workstation and mobile PC Network designs with critical space constraints, the Intel® 82541(PI/GI/EI) allows for a Gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs.

The Intel® 82541(PI/GI/EI) integrates fourth generation gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.3 compliant interface capable of operating at 33 or 66 MHz.

The 82541(PI/GI/EI) also incorporates the Clock Run protocol and hardware supported downshift capability to two-pair and three-pair 100 Mbps operation. These features optimize mobile applications.

The 82541(PI/GI/EI) on-board System Management Bus (SMB) port enables network manageability implementations required by information technology personnel for remote control and alerting via the Local Area Network (LAN). With SMB, management packets can be routed to or from a management processor. The SMB port enables industry standards, such as Intelligent Platform Management Interface (IPMI) and Alert Standard Forum (ASF) 2.0, to be implemented using the 82541(PI/GI/EI). In addition, on chip ASF 2.0 circuitry provides alerting and remote control capabilities with standardized interfaces.

The 82541(PI/GI/EI) Gigabit Ethernet Controller Architecture is designed for high performance and low memory latency. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82541(PI/GI/EI) controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes efficient bus usage. The 82541(PI/GI/EI) uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 64-KByte onchip packet buffer maintains superior performance as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The 82541(PI/GI/EI) is packaged in a 15 mm x 15 mm 196-ball grid array and is pin compatible with the 82551QM 10/100 Mbps Fast Ethernet Multifunction PCI/CardBus Controller, 82562EZ(EX) Platform LAN Connect devices, and the 82540EP(EM) Gigabit Ethernet Controller.

1.1 Document Scope

The 82541EI is the original device and is now being manufactured in a B0 stepping. The 82541GI (B1 stepping) and 82541PI (C0 stepping) are pin compatible, however, a different Intel software driver is required from the 82541EI. This document contains datasheet specifications for the 82541(PI/GI/EI) Gigabit Ethernet Controllers including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This document assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82540EP/82541(PI/GI/EI) & 825462EZ(EX) Dual Footprint Design Guide, AP-444. Intel Corporation.
- 82547GI(EI)/82541(PI/GI/EI)/82541ER EEPROM Map and Programming Information Guide, AP-446. Intel Corporation.
- PCI Local Bus Specification, Revision 2.3. PCI Special Interest Group (SIG).
- PCI Bus Power Management Interface Specification, Revision 1.1. PCI Special Interest Group (SIG).
- IEEE Standard 802.3, 2000 Edition. Incorporates various IEEE standards previously published separately. Institute of Electrical and Electronic Engineers (IEEE).
- PCI Mobile Design Guide, Revision 1.1. PCI Special Interest Group (SIG).

Software driver developers should contact their local Intel representatives for programming information.

1.3 Product Codes

The product ordering codes for the 82541 Family of Gigabit Ethernet Controllers:

- GD82541PI
- GD82541GI
- GD82541EI
- LU82541PI
- LU82541GI
- LU82541EI

2.0 Architectural Overview

2.1 External Architecture Block Diagram

The 82541(PI/GI/EI) architecture is a derivative of the 82542, 82543, and 82544 designs that provided Media Access Controller (MAC) functionality as well as an integrated 10/100/1000Mbps copper PHY. The 82541(PI/GI/EI) family architecture now adds SMBus-based manageability and an integrated ASF controller functionality to the MAC.

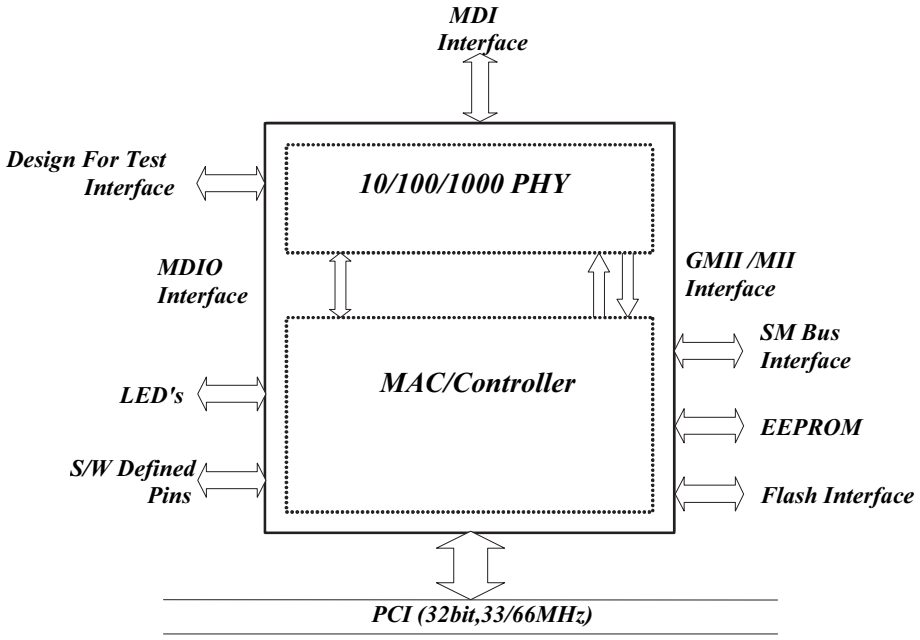


Figure 1. 82541(PI/GI/EI) External Architecture Block Diagram

2.2 Internal MAC Architecture Block Diagram

Figure 2 shows the major internal function blocks of 82541(PI/GI/EI) MAC device. Compared to its predecessors, the 82541(PI/GI/EI) MAC adds improved receive-packet filtering to support SMBus-based manageability, as well as the ability to support transmit of SMBus-based manageability packets. In addition, an ASF-compliant TCO controller is integrated into the MAC for reduced-cost basic ASF manageability.

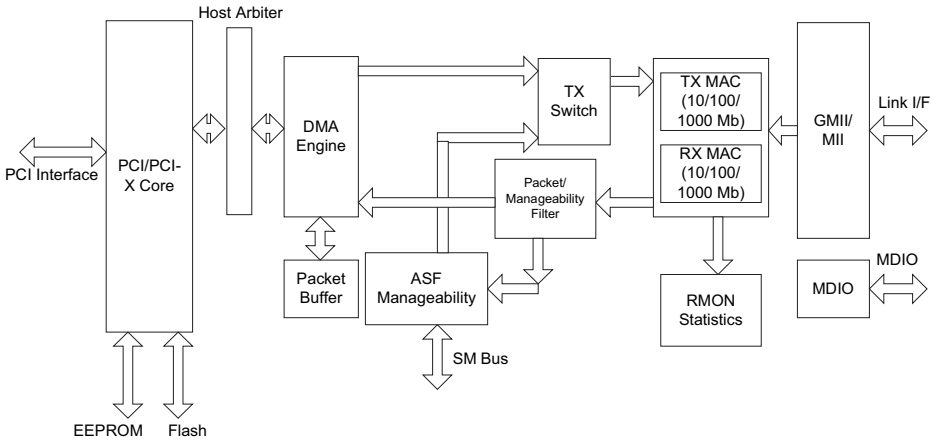


Figure 2. Internal Architecture Block Diagram

2.3 Integrated 10/100/1000Mbps PHY

The 82541(PI/GI/EI) contains an integrated 10/100/1000Mbps-capable Copper PHY. This PHY communicates with the MAC controller using a standard GMII/MII interface internal to the component to transfer transmit and receive data. A standard MDIO interface, accessible to software via MAC control registers, is used to configure and monitor the PHY operation.

2.4 System Interface

82541(PI/GI/EI) provides a 32-bit PCI 2.2 bus interface which is capable of up to 66 MHz operation in conventional PCI mode. In conventional PCI systems with a dedicated I/O bus per connector, this interface should provide sufficient bandwidth to support a sustained 1000 Mb/sec transfer rate. 64 KB of on-chip buffering mitigates instantaneous receive bandwidth demands and eliminates transmit under-runs by buffering the entire outgoing packet prior to transmission.

3.0 Signal Descriptions

3.1 Signal Type Definitions

The signals of the 82541(PI/GI/EI) controller are electrically defined as follows:

Name	Definition
I	**Input.** Standard input only digital signal.
O	**Output.** Standard output only digital signal.
TS	**Tri-state.** Bi-directional tri-state digital input/output signal.
STS	**Sustained Tri-state.** An active low tri-state signal owned and driven by only one agent at a time. The agent that drives an STS pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an STS signal any sooner than one clock after the previous owner tri-states it. A pull-up resistor is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OD	**Open Drain.** Wired-OR with other agents. The signaling agent asserts the OD signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may require two or three clock periods to fully restore the signal to the de-asserted state.
A	**Analog.** PHY analog data signal.
P	**Power.** Power connection, voltage reference, or other reference connection.

3.2 PCI Bus Interface Signals (56)

When the Reset signal (RST#) is asserted, the 82541(PI/GI/EI) will not drive any PCI output or bi-directional pins. The Power Management Event signal (PME#) can be active by configuring manageability functions.

3.2.1 PCI Address, Data and Control Signals (44)

Symbol	Type	Name and Function
AD[31:0]	TS	**Address and Data.** Address and data signals are multiplexed on the same PCI pins. A bus transaction includes an address phase followed by one or more data phases. The address phase is the clock cycle when the Frame signal (FRAME#) is asserted low. During the address phase AD[31:0] contain a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, a DWORD address. The 82541(PI/GI/EI) device uses little endian byte ordering. During data phases, AD[7:0] contain the least significant byte (LSB) and AD[31:24] contain the most significant byte (MSB).
C/BE#[3:0]	TS	**Bus Command and Byte Enables.** Bus command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE#[3:0] define the bus command. In the data phase, C/BE#[3:0] are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes contain meaningful data. C/BE[0]# applies to byte 0 (LSB) and C/BE#[3] applies to byte 3 (MSB).
PAR	TS	**Parity.** The Parity signal is issued to implement even parity across AD[31:0] and C/BE#[3:0]. PAR is stable and valid one clock after the address phase. During data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82541(PI/GI/EI) controller is a bus master, it drives PAR for address and write data phases, and as a slave device, drives PAR for read data phases.
FRAME#	STS	**Cycle Frame.** The Frame signal is driven by the 82541(PI/GI/EI) device to indicate the beginning and length of a bus transaction. While FRAME# is asserted, data transfers continue. FRAME# is de-asserted when the transaction is in the final data phase.
IRDY#	STS	**Initiator Ready.** Initiator Ready indicates the ability of the 82541(PI/GI/EI) controller (as a bus master device) to complete the current data phase of the transaction. IRDY# is used in conjunction with the Target Ready signal (TRDY#). The data phase is completed on any clock when both IRDY# and TRDY# are asserted. During the write cycle, IRDY# indicates that valid data is present on AD[31:0]. For a read cycle, it indicates the master is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82541(PI/GI/EI) controller drives IRDY# when acting as a master and samples it when acting as a slave.
TRDY#	STS	**Target Ready.** The Target Ready signal indicates the ability of the 82541(PI/GI/EI) controller (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with the Initiator Ready signal (IRDY#). A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted. During a read cycle, TRDY# indicates that valid data is present on AD[31:0]. For a write cycle, it indicates the target is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82541(PI/GI/EI) device drives TRDY# when acting as a slave and samples it when acting as a master.
STOP#	STS	**Stop.** The Stop signal indicates the current target is requesting the master to stop the current transaction. As a slave, the 82541(PI/GI/EI) controller drives STOP# to request the bus master to stop the transaction. As a master, the 82541(PI/GI/EI) controller receives STOP# from the slave to stop the current transaction.

Symbol	Type	Name and Function
IDSEL	I	**Initialization Device Select.** The Initialization Device Select signal is used by the 82541(PI/GI/EI) as a chip select signal during configuration read and write transactions.
DEVSEL#	STS	**Device Select.** When the Device Select signal is actively driven by the 82541(PI/GI/EI), it signals the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
VIO	P	**VIO.** The VIO signal is a voltage reference for the PCI interface (3.3 V or 5 V PCI signaling environment). It is used as the clamping voltage. **Note:** VIO should be connected to 3.3 V Aux or 5 V Aux in order to be compatible with the pull-up clamps specification.

3.2.2 Arbitration Signals (2)

Symbol	Type	Name and Function
REQ#	TS	**Request Bus.** The Request Bus signal is used to request control of the bus from the arbiter. This signal is point-to-point.
GNT#	I	**Grant Bus.** The Grant Bus signal notifies the 82541(PI/GI/EI) that bus access has been granted. This is a point-to-point signal.

3.2.3 Interrupt Signal (1)

Symbol	Type	Name and Function
INTA#	TS	**Interrupt A.** Interrupt A is used to request an interrupt of the 82541(PI/GI/EI). It is an active low, level-triggered interrupt signal.

3.2.4 System Signals (4)

Symbol	Type	Name and Function
CLK	I	**PCI Clock.** The PCI Clock signal provides timing for all transactions on the PCI bus and is an input to the 82541(PI/GI/EI) device. All other PCI signals, except the Interrupt A (INTA#) and PCI Reset signal (RST#), are sampled on the rising edge of CLK. All other timing parameters are defined with respect to this edge.
M66EN	I	**66 MHz Enable.** M66EN indicates whether the system bus is enabled for 66MHz.
RST#	I	**PCI Reset.** When the PCI Reset signal is asserted, all PCI output signals, except the Power Management Event signal (PME#), are floated and all input signals are ignored. The PME# context is preserved, depending on power management settings. Most of the internal state of the 82541(PI/GI/EI) is reset on the de-assertion (rising edge) of RST#.
CLK_RUN#	I/O OD	**Clock Run.** This signal is used by the system to pause the PCI clock signal. It is used by the 82541(PI/GI/EI) controller to request the PCI clock. When the CLK_RUN# feature is disabled, leave this pin unconnected.

3.2.5 Error Reporting Signals (2)

Symbol	Type	Name and Function
SERR#	OD	**System Error.** The System Error signal is used by the 82541(PI/GI/EI) controller to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR#	STS	**Parity Error.** The Parity Error signal is used by the 82541(PI/GI/EI) controller to report data parity errors during all PCI transactions except by a Special Cycle. PERR# is sustained tri-state and must be driven active by the 82541(PI/GI/EI) controller two data clocks after a data parity error is detected. The minimum duration of PERR# is one clock for each data phase a data parity error is present.

3.2.6 Power Management Signals (3)

Symbol	Type	Name and Function
LAN_ PWR_GOOD	I	**Power Good (Power-on Reset).** The LAN_PWR_GOOD signal is used to indicate that stable power is available for the 82541(PI/GI/EI). When the signal is low, the 82541(PI/GI/EI) holds itself in reset state and floats all PCI signals.
PME#	OD	**Power Management Event.** The 82541(PI/GI/EI) device drives this signal low when it receives a wake-up event and either the PME Enable bit in the Power Management Control/Status Register or the Advanced Power Management Enable (APME) bit of the Wake-up Control Register (WUC) is 1b.
AUX_PWR	I	**Auxiliary Power.** If the Auxiliary Power signal is high, then auxiliary power is available and the 82541(PI/GI/EI) device should support the D3cold power state.

3.2.7 SMB Signals (3)

Symbol	Type	Name and Function
SMBCLK	TS OD	**SMB Clock.** The SMB Clock signal is an open drain signal for serial SMB interface.
SMBDATA	TS OD	**SMB Data.** The SMB Data signal is an open drain signal for serial SMB interface.
SMB_ALERT#/ LAN_PWR_ GOOD	TS OD	**Multiplexed pin: SMB Alert, LAN Power Good.** The SMB_ALERT# signal is open drain for serial SMB interface. The signal acts as an interrupt pin of a slave device on the SMBUS in TCO mode. (82559 mode). In ASF mode, this signal acts as LAN_PWR_GOOD input.

Note: If the SMB is disconnected, then an external pull-up resistor should be used for these pins.

3.3 EEPROM and Serial FLASH Interface Signals (9)

Symbol	Type	Name and Function
EEMODE	I	**EEPROM Mode.** The EEPROM Mode pin is used to select the interface and source of the EEPROM used to initialize the device. For a MIcrowire* EEPROM on the standard EEPROM pins, tie this pin to ground with a 1 KΩ pull-down resistor (for the 82541PI, use a 100 Ω pull-down resistor instead). For an Serial Peripheral Interface (SPI*) EEPROM attached to the Flash memory pins, leave this pin unconnected.
EEDI	O	**EEPROM Data Input.** The EEPROM Data Input pin is used for output to the memory device.
EEDO	I	**EEPROM Data Output.** The EEPROM Data Output pin is used for input from the memory device. EEDO includes an internal pull-up resistor.
EECS	O	**EEPROM Chip Select.** The EEPROM Chip Select signal is used to enable the device.
EESK	O	**EEPROM Serial Clock.** The EEPROM Shift Clock provides the clock rate for the EEPROM interface, which is approximately 1 MHz for Microwire* and 2 MHz for SPI.
FLSH_CE#	O	**FLASH Chip Enable Output.** Used to enable FLASH device.
FLSH_SCK	O	**FLASH Serial Clock Output.** The clock rate of the serial FLASH interface is approximately 1 MHz.
FLSH_SI	O	**FLASH Serial Data Input.** This pin is an output to the memory device.
FLSH_SO/ LAN_DISABLE#	I	**FLASH Serial Data Output / LAN Disable.** This pin is an input from the FLASH memory. Alternatively, the pin can be used to disable the LAN port from a system GP (General Purpose) port. If the 82541(PI/GI/EI) is not using Flash functionality, the pin should be connected to external pull-up resistor. If this pin is used as LAN_DISABLE#, the device goes to low power state and the LAN port is disabled when the pin is sampled low on rising edge of PCI reset.

3.4 Miscellaneous Signals

3.4.1 LED Signals (4)

Symbol	Type	Name and Function
LED0 / LINK_UP#	O	**LED0 / LINK Up.** Programmable LED indication. Defaults to indicate link connectivity.
LED1 / ACTIVITY#	O	**LED1 / Activity.** Programmable LED indication. Defaults to flash to indicate transmit or receive activity.
LED2 / LINK100#	O	**LED2 / LINK 100.** Programmable LED indication. Defaults to indicate link at 100 Mbps.
LED3 / LINK1000#	O	**LED3 / LINK 1000.** Programmable LED indication. Defaults to indicate link at 1000 Mbps.

3.4.2 Other Signals (4)

Symbol	Type	Name and Function
SDP[3:0]	TS	**Software Defined Pin.** The Software Defined Pins are reserved and programmable with respect to input and output capability. These default to input signals upon power-up but may be configured differently by the EEPROM. The upper two bits may be mapped to the General Purpose Interrupt bits if they are configured as input signals.

3.5 PHY Signals

3.5.1 Crystal Signals (2)

Symbol	Type	Name and Function
XTAL1	I	**Crystal One.** The Crystal One pin is a 25 MHz +/- 30 ppm input signal. It should be connected to a crystal, and the other end of the crystal should be connected to XTAL2.
XTAL2	O	**Crystal Two.** Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation.

Note: The 82541 clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used in place of the crystal with the proper design considerations. The 82540EP/ 82541(PI/GI/EI) & 825462EZ(EX) Dual Footprint Design Guide (AP-444) should be consulted for further details.

3.5.2 Analog Signals (10)

Symbol	Type	Name and Function
MDI[0]+/-	A	**Media Dependent Interface [0].** **1000BASE-T**: In MDI configuration, MDI[0]+/- corresponds to BI_DA+/-, and in MDI-X configuration, MDI[0]+/- corresponds to BI_DB+/-. **100BASE_TX**: In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair. **10BASE-T**: In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair.
MDI[1]+/-	A	**Media Dependent Interface [1].** **1000BASE-T**: In MDI configuration, MDI[1]+/- corresponds to BI_DB+/-, and in MDI-X configuration, MDI[1]+/- corresponds to BI_DA+/-. **100BASE_TX**: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transit pair. **10BASE-T**: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transit pair.
MDI[2]+/-	A	**Media Dependent Interface [2].** **1000BASE-T**: In MDI configuration, MDI[2]+/- corresponds to BI_DC+/-, and in MDI-X configuration, MDI[2]+/- corresponds to BI_DD+/-. **100BASE_TX**: Unused. **10BASE-T**: Unused.

MDI[3]+/-	A	**Media Dependent Interface [3].** **1000BASE-T**: In MDI configuration, MDI[3]+/- corresponds to BI_DC+/-, and in MDI-X configuration, MDI[3]+/- corresponds to BI_DD+/-. **100BASE_TX**: Unused. **10BASE-T**: Unused.
IEEE_TEST-	A	**IEEE test pin output minus.** Used to gain access to the internal PHY clock for 1000BASE-T IEEE physical layer conformance testing.
IEEE_TEST+	A	**Analog test pin output plus.** Used to gain access to the internal PHY clock for 1000BASE-T IEEE physical layer conformance testing.

3.6 Test Interface Signals (6)

Symbol	Type	Name and Function
TEST	I	**Test Enable.** Enables test mode. Normal mode: connect to VSS.
JTAG_TCK	I	**JTAG Test Access Port Clock.**
JTAG_TDI	I	**JTAG Test Access Port Data In.**
JTAG_TDO	O	**JTAG Test Access Port Data Out.**
JTAG_TMS	I	**JTAG Test Access Port Mode Select.**
JTAG_TRST#	I	**JTAG Test Access Port Reset.** This is an active low reset signal for JTAG. To disable the JTAG interface, this signal should be terminated using pull-down resistor (1 KΩ for the 82541GI(EI) and 100 Ω for the 82541PI) to ground. It must not be left unconnected.

3.7 Power Supply Connections

3.7.1 Digital and Analog Supplies

Symbol	Type	Name and Function
3.3V	P	**3.3 V I/O Power Supply.**
ANALOG_1.8V	P	**1.8 V Analog Power Supply.**
CLKR_1.8V	P	**1.8 V analog power supply for the clock recovery.**
XTAL_1.8V	P	**Input power for the XTAL regulator.**
1.2V	P	**1.2 V Power supply.** For analog and digital circuits.
ANALOG_1.2V	P	**1.2 V Analog Power Supply.**
PLL_1.2V	P	**Input power for the ICS regulator.**

3.7.2 Grounds, Reserved Pins and No Connects

Symbol	Type	Name and Function
VSS	P	**Ground.**
AVSS	P	**Shared analog Ground.**
RSVD_VSS	P	**Reserved Ground.** This pin is reserved by Intel and may have factory test functions. For normal operation, connect to ground.
RSVD_NC	P	**Reserved No connect.** This pin is reserved by Intel and may have factory test functions. For normal operation, do not connect any circuit to these pins. Do not connect pull-up or pull-down resistors.
NC	P	**No Connect.** This pin is not connected internally.

3.7.3 Voltage Regulation Control Signals (2)

Symbol	Type	Name and Function
CTRL12	A	**1.2 V Control.** LDO voltage regulator output to drive external PNP pass transistor. If 1.2 V is already present in the system, leave output unconnected. To achieve optimal D3 power consumption, leave the output unconnected and use a high-efficiency external regulator.
CTRL18	A	**1.8 V Control.** LDO voltage regulator output to drive external PNP pass transistor. If 1.8 V is already present in the system, leave output unconnected. To achieve optimal D3 power consumption, leave the output unconnected and use a high-efficiency external regulator.

4.0 Voltage, Temperature, and Timing Specifications

4.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[a]

Symbol	Parameter	Min	Max	Unit
VDD (3.3)	DC supply voltage on 3.3 V pins with respect to VSS	VSS - 0.5	4.6	V
VDD (1.8)	DC supply voltage on 1.8 V pins with respect to VSS	VSS - 0.5	2.5 or VDD (1.8) + 0.5[b]	V
VDD (1.2)	DC supply voltage on 1.2 V pins with respect to VSS	VSS - 0.5	1.7 or VDD (1.2) + 0.5[c]	V
VDD	DC supply voltage	VSS - 0.5	4.6	V
VI / VO	Input voltage	VSS - 0.5	4.6[d]	V
IO	Output current		40	mA
TSTG	Storage temperature range	-40	125	°C
	ESD per MIL_STD-883 Test Method 3015, Specification 2001V Latchup Over/Undershoot: 150 mA, 125 C		VDD overstress: VDD (3.3) * (7.2 V)	V

a. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded. These values should not be used as the limits for normal device operations.
b. The maximum value is the lesser value of 2.5 V or VDD (2.5) + 0.5 V. This specification applies to biasing the device to a steady state for an indefinite duration.
c. The maximum value is the lesser value of 1.7 V or VDD (2.5) + 0.5 V.
d. The maximum value must also be less than VIO.

4.2 Targeted Recommended Operating Conditions

4.2.1 General Operating Conditions

Table 2. Recommended Operating Conditions (Sheet 1 of 2)[a]

Symbol	Parameter	Min	Max	Unit
VDD (3.3)	DC supply voltage on 3.3 V pins	3.0	3.6	V
VDD (1.8)	DC supply voltage on 1.8 V pins	1.71[b]	1.89[c]	V
VDD (1.2)	DC supply voltage on 1.2 V pins	1.14[d]	1.26[e]	V
VIO	PCI bus reference voltage	3.0	5.25	V
tR / tF	Input rise/fall time (normal input)	0	200	ns

Table 2. Recommended Operating Conditions (Sheet 2 of 2)[a]

Symbol	Parameter	Min	Max	Unit
tr/tf	input rise/fall time (Schmitt input)	0	10	ms
T_A	Operating temperature range (ambient)	0	70	°C
T_J	Junction temperature		≤125	°C

a. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent damage.
b. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.67 V.
c. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.926 V.
d. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.12 V.
e. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.284 V.

4.2.2 Voltage Ramp and Sequencing Recommendations

Note: In any case or time period (greater than 1 ns), the supply voltage should comply with 3.3 V > 1.8 V > 1.2V. This is important to avoid stress in the ESD protection circuits. After 3.3 V reaches 10% of its final value, all voltage rails (1.8 V and 1.2 V) have 150 ms to reach their final operating values.

Table 3. 3.3V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp		0	mV
Slope	Ramp rate at any time between 10% to 90%		28800	V/s
Operational Range	Voltage range for normal operating conditions	3	3.6	V
Ripple	Maximum voltage ripple at a bandwidth equal to 50 MHz		70	mV
Overshoot	Maximum voltage allowed		4	V

Table 4. 1.8V Supply Voltage Ramp

Symbol	Parameter	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp		0	mV
Slope	Ramp rate at any time between 10% to 90%		57600	V/s
Operational Range	Voltage range for normal operating conditions	1.71	1.89	V
Ripple	Maximum voltage ripple at frequency below 1 MHz		280	$mV_{pk\text{-}to\text{-}pk}$
Ripple	Minimum voltage ripple at frequency below 1 MHz	1.55		V
Overshoot	Maximum voltage allowed		2.2	V

Table 4. 1.8V Supply Voltage Ramp

Output Capacitance	Capacitance range when using PNP circuit	4.7	20	µF
Input Capacitance	Capacitance range when using PNP circuit	4.7	20	µF
Capacitance ESR	Equivalent series resistance of output capacitance[a]	5	100	mΩ
Ictrl_18	Maximum output current rating to CTRL18		20	mA

a. Tantalum capacitors must not be used.

Table 5. 1.2V Supply Voltage Ramp

Symbol	Parameter	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.025		ms
Monotonicity	Voltage dip allowed in ramp		0	mV
Slope	Ramp rate at any time between 10% to 90%		38400	V/s
Operational Range	Voltage range for normal operating conditions	1.14	1.26	V
Ripple	Maximum voltage ripple at frequency below 1 MHz		180	$mV_{pk\text{-}to\text{-}pk}$
Ripple	Maximum voltage ripple at frequency below 1 MHz	1		V
Overshoot	Maximum voltage allowed		1.45	V
Output Capacitance	Capacitance range when using PNP circuit	4.7	20	µF
Input Capacitance	Capacitance range when using PNP circuit	4.7	20	µF
Capacitance ESR	Equivalent series resistance of output capacitance[a]	5	100	mΩ
Ictrl_12	Maximum output current rating to CTRL12		20	mA

a. Tantalum capacitors must not be used.

4.3 DC Specifications

Table 6. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD (3.3)	DC supply voltage on 3.3 V pins		3.00	3.3	3.60	V
VDD (1.8)	DC supply voltage on 1.8 V pins		1.71[a]	1.8	1.89[b]	V
VDD (1.2)	DC supply voltage on 1.2 V pins		1.14[c]	1.2	1.26[d]	V

a. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.67 V.
b. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.926 V.
c. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the minimum value is 1.12 V.
d. The value listed in this table is for external voltage regulation. If the internal voltage regulator is used, the maximum value is 1.284 V.

Table 7. Power Specifications - D0a

	D0a							
	unplugged no link		@10 Mbps		@100 Mbps		@ 1000 Mbps	
	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]
3.3 V	3 mA	5 mA	5 mA	10 mA	13 mA	15 mA	30 mA	40 mA
1.8 V	14 mA	15 mA	85 mA	85 mA	110 mA	115 mA	315 mA	320 mA
1.2 V	30 mA	35 mA	85 mA	90 mA	90 mA	100 mA	380 mA	400 mA
Total Device Power	75 mW	85 mW	270 mW	295 mW	350 mW	380 mW	1.1 W	1.2 W

a. Typical conditions: operating temperature (T_A) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.
b. Maximum conditions: minimum operating temperature (T_A) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

Table 8. Power Specifications - D3cold

	D3cold - wake-up enabled[a]						D3cold-wake disabled	
	unplugged link		@10 Mbps		@100 Mbps			
	Typ Icc (mA)[b]	Max Icc (mA)[c]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]
3.3 V	2 mA	3 mA	2 mA	3 mA	2 mA	3 mA	4 mA	5 mA
1.8 V	14 mA	15 mA	20 mA	25 mA	110 mA	115 mA	1 mA	2 mA
1.2 V	21 mA	25 mA	30 mA	35 mA	80 mA	85 mA	7 mA	10 mA
Total Device Power	60 mW	70 mW	80 mW	100 mW	300 mW	320 mW	25 mW	35 mW

a. At 1000 Mbps, power consumption is not shown since the controller switches to the 10/100 Mbps state before entering D3 to conserve power.
b. Typical conditions: operating temperature (T_A) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.
c. Maximum conditions: minimum operating temperature (T_A) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

Table 9. Power Specifications D(r) Uninitialized

	D(r) Uninitialized (FLSH_SO/LAN_DISABLE# = 0)	
	Typ Icc (mA)	Max Icc (mA)
3.3 V	5 mA	10 mA
1.8 V	1 mA	2 mA
1.2 V	12 mA	15 mA
Total Device Power	35 mW	

Table 10. Power Specifications - Complete Subsystem

	Complete Subsystem (Reference Design) Including Magnetics, LED, Regulator Circuits											
	D3cold - wake disabled		D3cold wake-enabled @ 10 Mbps		D3cold wake-up enabled @ 100 Mbps		D0 @10 Mbps active		D0 @100 Mbps active		D0 @ 1000 Mbps active	
	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]	Typ Icc (mA)[a]	Max Icc (mA)[b]
3.3 V	4	5	2	3	6	7	7	12	19	21	36	46
1.8 V	1	2	20	25	110	115	85	85	110	115	315	320
1.2 V	7	10	30	35	80	85	85	90	90	100	380	400
Sub-system Power	40 mW	60 mW	175 mW	210 mW	650 mW	685 mW	585 mW	620 mW	725 mW	780 mW	2.4 W	2.5 W

a. Typical conditions: operating temperature (T_A) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.
b. Maximum conditions: minimum operating temperature (T_A) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

Table 11. I/O Characteristics (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIH	Input high voltage	3.3 V PCI	0.5 * VDD (3.3)		VDD (3.3) or VIO	V
		SMB	2.1		VDD (3.3) or VIO	
VIL	Input low voltage	Non-SMB[a]	VSS		0.3 * VDD (3.3)	V
		SMB	VSS		0.8	
IIN	Input current	0 < VIN < VDD (3.3)	-10		10	µA
	Input with pull-down resistor (50 K Ω)	VIN = VDD (3.3)	28		191	
	Inputs with pull-up resistor (50 K Ω)	VIN = VSS	-28		-191	
IOL	Output low current	3.3 V PCI[b]			2.09	mA
		$0 \le V_{OUT} \le 3.6V$			$100 * V_{OUT}$	
		$0 \le V_{OUT} \le 1.3V$	$48 * V_{OUT}$			
		$1.3V \le V_{OUT} \le 3.6V$	$5.7 * V_{OUT} + 55$			

Table 11. I/O Characteristics (Sheet 2 of 2) (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
IOH	Output high current:	$0 \le (V_{DD}\text{-}V_{OUT}) \le 3.6V$			$-74 * (V_{DD} - V_{OUT})$	mA
		$0 \le (V_{DD}\text{-}V_{OUT}) \le 1.2V$	$-32 * (V_{DD} - V_{OUT})$			
		$1.2V \le (V_{DD}\text{-}V_{OUT}) \le 1.9V$	$-11 * (V_{DD} - V_{OUT})-25.2$			
		$1.9V \le (V_{DD}\text{-}V_{OUT}) \le 3.6V$	$-1.8 * (V_{DD} - V_{OUT})-42.7$			
VOH	Output high voltage: 3.3 V PCI	IOH = -500 mA	0.9 * VDD (3.3)			V
VOL	Output low voltage: 3.3 V PCI	IOL = 1500 mA			0.1 * VDD (3.3)	V
IOZ	Off-state output leakage current	VO = VDD or VSS	-10		10	µA
IOS	Output short circuit current				-250	
CIN	Input capacitance[c]	Input and bi-directional buffers		8		pF

a. This is only applicable to the 82541PI. The maximum VIL is 0.6 V for the following pins: A13, C5, C8, J4, L7, L13, L12, M8, M12, M13, N10, N11, N13, N14, P9, and P13.
b. This is only applicable to the 82541PI.
c. V_{DD} (3.3) = 0 V; T_A = 25 C; f = 1 Mhz

4.4 AC Characteristics

Table 12. AC Characteristics: 3.3 V Interfacing

Symbol	Parameter	Min	Typ	Max	Unit
CLK	Clock frequency in PCI mode			66	MHz

Table 13. 25 MHz Clock Input Requirements

Symbol	Parameter	Specifications			Units
		Min	Typ	Max	
f0	Frequency		25		MHz
df0	Frequency variation	-50		+30	ppm
Dc	Duty cycle	40		60	%
tr	Rise time			5	ns
tf	Fall time			5	ns
Jptp	Clock jitter (peak-to-peak)[a]			250	ps

Table 13. 25 MHz Clock Input Requirements

Symbol	Parameter	Specifications			Units
		Min	Typ	Max	
Cin	Input capacitance		20		pF
T	Operating temperature			70	° C
Aptp	Input clock amplitude (peak-to-peak)	1.0	1.2	1.3	V
Vcm	Clock common mode		0.6		V

a. Clock jitter is defined according to the recommendations of part 40.6.1.2.5 IEEE 1000BASE-T Standard (at least 10^5 clock edges, filtered by HPF with cut off frequency 5000 Hz).

Table 14. Reference Crystal Specification Requirements

Specification	Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C
Frequency Tolerance	• ±30 ppm recommended • ±30 ppm required for the 82541GI/EI • ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	• ±50 ppm at 0° C to 70° C • ±30 ppm at 0° C to 70° C (required for the 82541GI/EI)
Calibration Mode	Parallel
Load Capacitance	• 16 pF to 20 pF • 18 pF (required for the 82541GI/EI)
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	• 50 Ω maximum • 20 Ω maximum (required for the 82541GI/EI)
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum

Table 15. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fGTX[a]	GTX_CLK frequency		125		MHz

a. GTX_CLK is used externally for test purposes only.

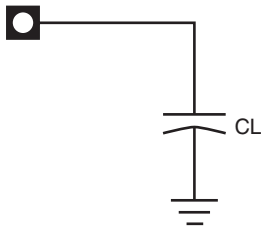
Table 16. EEPROM Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fSK	Microwire EEPROM Clock			1	MHz
	SPI EEPROM Clock			2	MHz

AC Test Loads for General Output Pins

Symbol	Signal Name	Value	Units
CL	TDO	10	pF
CL	PME#, SDP[3:0]	16	pF
CL	EEDI, EESK	18	pF
CL	LED[3:0]	20	pF

Figure 3. AC Test Loads for General Output Pins



4.5 Timing Specifications

Table 17. PCI Bus Interface Clock Parameters

Symbol	Parameter[a]	PCI 66 MHz		PCI 33 MHz		Units
		Min	Max	Min	Max	
TCYC	CLK cycle time	15	30	30		ns
TH	CLK high time	6		11		ns
TL	CLK low time	6		11		ns
	CLK slew rate	1.5	4	1	4	V/ns
	RST# slew rate[b]	50		50		mV/ns

a. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown.
b. The minimum RST# slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot render a monotonic signal to appear bouncing in the switching range.

Figure 4. AC Test Loads for General Output Pins

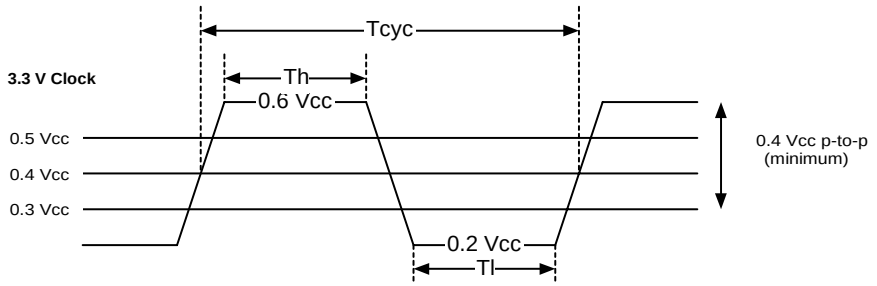


Table 18. PCI Bus Interface Timing Parameters

Symbol	Parameter	PCI 66MHz		PCI 33 MHz		Units
		Min	Max	Min	Max	
TVAL	CLK to signal valid delay: bussed signals	2	6	2	11	ns
TVAL(ptp)	CLK to signal valid delay: point-to-point signals	2	6	2	12	ns
TON	Float to active delay	2		2		ns
TOFF	Active to float delay		14		28	ns
TSU	Input setup time to CLK: bussed signals	3		7		ns
TSU(ptp)	Input setup time to CLK: point-to-point signals	5		10, 12		ns
TH	Input hold time from CLK	0		0		ns

NOTES:
1. Output timing measurements are as shown.
2. REQ# and GNT# signals are point-to-point and have different output valid delay and input setup times than bussed signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All other signals are bussed.
3. Input timing measurements are as shown.

Figure 5. AC Test Loads for General Output Pins

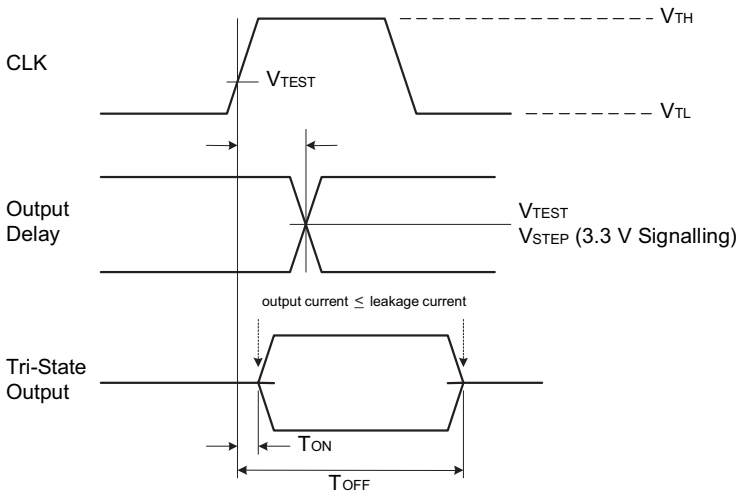


Figure 6. AC Test Loads for General Output Pins

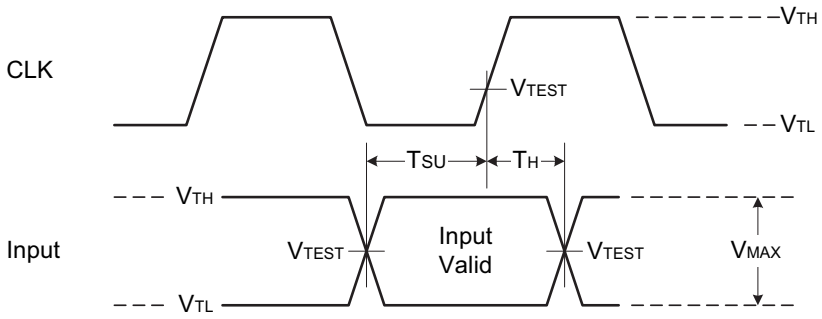


Table 19. PCI Bus Interface Timing Measurement Conditions

Symbol	Parameter	PCI 66 MHz 3.3 v	Unit
VTH	Input measurement test voltage (high)	0.6 * VCC	V
VTL	Input measurement test voltage (low)	0.2 * VCC	V
VTEST	Output measurement test voltage	0.4 * VCC	V
	Input signal slew rate	1.5	V/ns

Figure 7. TVAL (max) Rising Edge Test Load

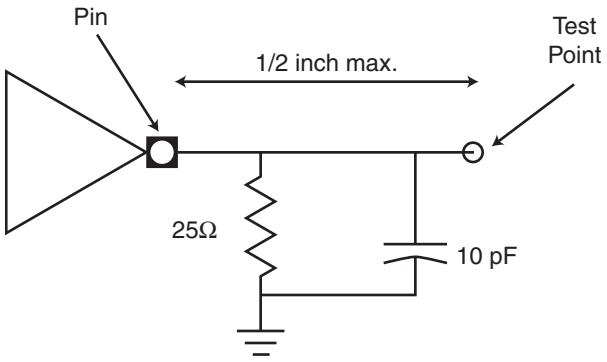


Figure 8. TVAL (max) Falling Edge Test Load

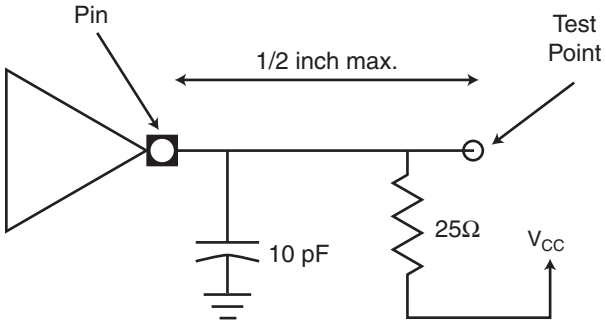


Figure 9. TVAL (min) Test Load

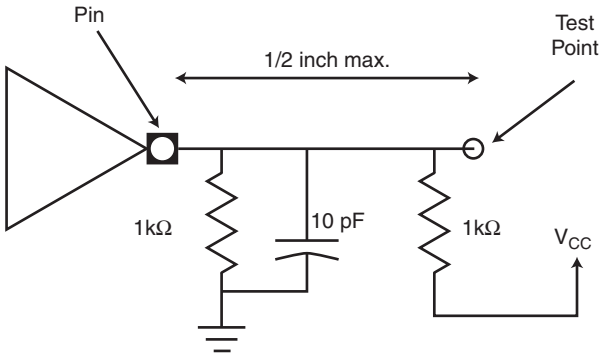
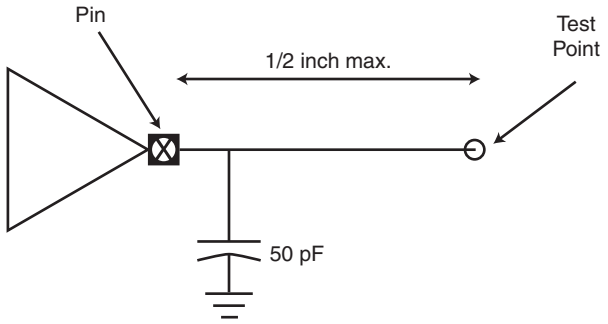


Figure 10. TVAL Test Load (PCI 5 V Signaling Environment)



NOTE: 50 pF load used for maximum times. Minimum times are specified with 0 pF load.

Table 20. Link Interface Rise and Fall Times

Symbol	Parameter	Condition	Min	Max	Unit
TR	Clock rise time	0.8 V to 2.0 V	0.7		ns
TF	Clock fall time	2.0 V to 0.8 V	0.7		ns
TR	Data rise time	0.8 V to 2.0 V	0.7		ns
TF	Data fall time	2.0 V to 0.8 V	0.7		ns

Figure 11. Link Interface Rise/Fall Timing

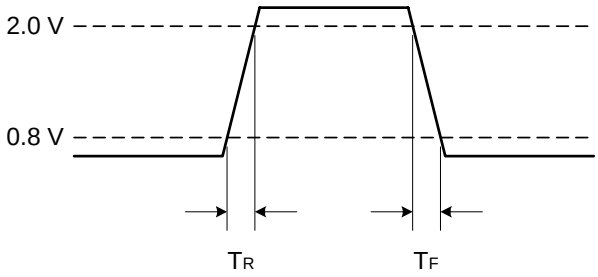


Table 21. EEPROM Link Interface Clock Requirements

Symbol	Parameter[a]	Min	Typ	Max	Unit
TPW	Microwire EESK pulse width		$T_{PERIOD} \times 64$		ns
	SPI EESK pulse width		$T_{PERIOD} \times 32$		ns

a. The EEPROM clock is derived from a 125 MHz internal clock.

Table 22. EEPROM Link Interface Clock Requirements

Symbol	Parameter[a]	Min	Typ	Max	Unit
TDOS	EEDO setup time	TCYC*2			ns
TDOH	EEDO hold time	0			ns

a. The EEDO setup and hold time is a function of the PCI bus clock cycle time but is referenced to O_EESK.

5.0 Package and Pinout Information

This section describes the 82541(PI/GI/EI) device physical characteristics. The pin number-to-signal mapping is indicated beginning with Table 14.

5.1 Package Information

The 82541(PI/GI/EI) device is a 196-lead plastic ball grid array (BGA) measuring 15 mm by 15 mm. The package dimensions are detailed below. The nominal ball pitch is 1 mm.

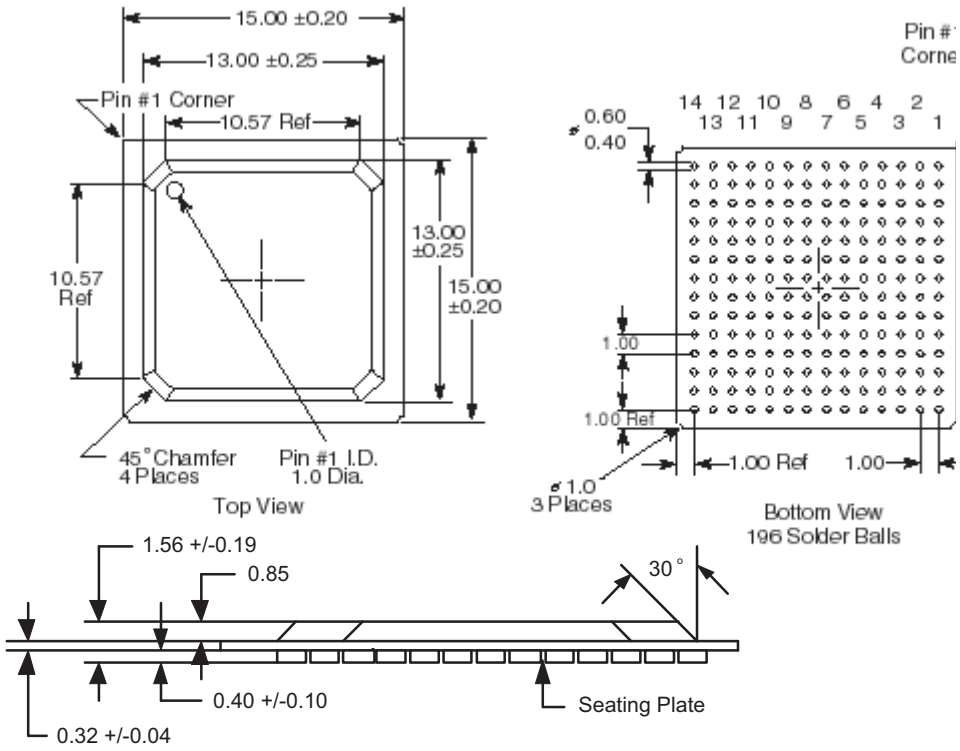


Figure 11. 82541(PI/GI/EI) Mechanical Specifications

Note: No changes to existing soldering processes are needed for the 0.32 mm substrate change.

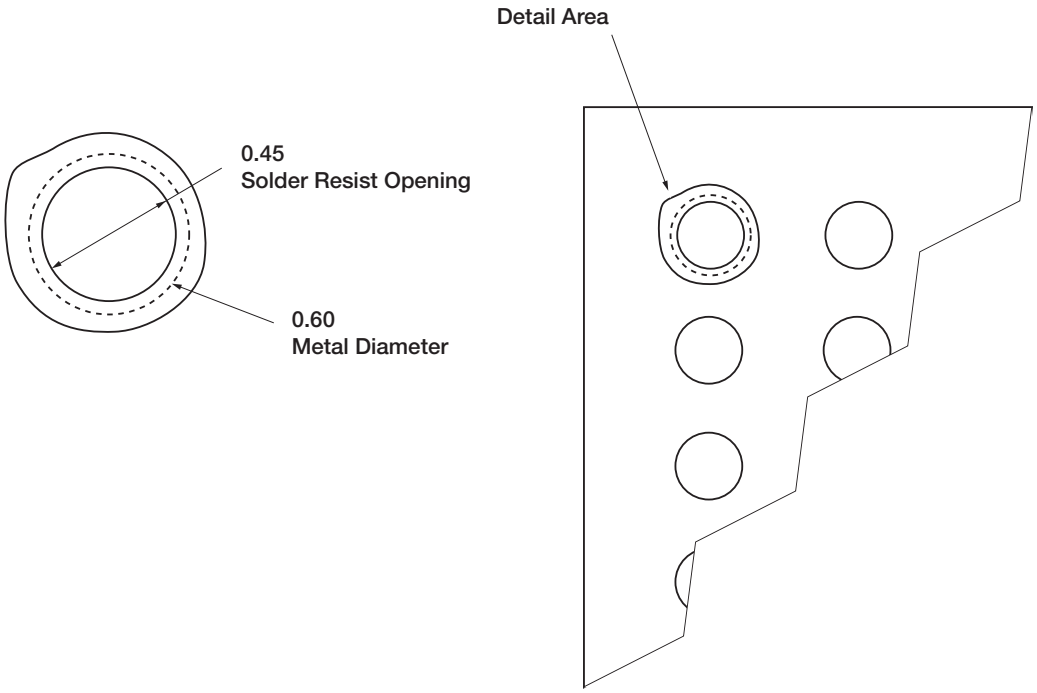


Figure 12. 196 PBGA Package Pad Detail

As illustrated in Figure 12, the Ethernet controller package uses solder mask defined pads. The copper area is 0.60 mm and the opening in the solder mask is 0.45 mm. The nominal ball sphere diameter is 0.50 mm.

5.2 Thermal Specifications

The 82541(PI/GI/EI) device is specified for operation when the ambient temperature (T_A) is within the range of 0° C to 70° C.

T_C (case temperature) is calculated using the equation:

$$T_C = T_A + P (\theta_{JA} - \theta_{JC})$$

TJ (junction temperature) is calculated using the equation:

$$T_J = T_A + P\ \theta_{JA}$$

P (power consumption) is calculated by using the typical I_{CC}, as indicated in Table 7 of Section 4.0, and nominal V_{CC}. The preliminary thermal resistances are shown in Table 13.

Table 13. Thermal Characteristics

Symbol	Parameter	Preliminary Value at specified airflow (m/s)			Units
		0	1	2	
θ_{JA}	Thermal resistance, junction-to-ambient	29	25.0	23.5	C/Watt
θ_{JC}	Thermal resistance, junction-to-case	11.1	11.1	11.1	C/Watt

Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. The case temperature measurements should be used to assure that the 82541(PI/GI/EI) device is operating under recommended conditions.

5.3 Pinout Information

Table 14. PCI Address, Data and Control Signals

Signal	Pin	Signal	Pin	Signal	Pin
AD[0]	N7	AD[16]	K1	C/BE#[0]	M4
AD[1]	M7	AD[17]	E3	C/BE#[1]	L3
AD[2]	P6	AD[18]	D1	C/BE#[2]	F3
AD[3]	P5	AD[19]	D2	C/BE#[3]	C4
AD[4]	N5	AD[20]	D3	PAR	J1
AD[5]	M5	AD[21]	C1	FRAME#	F2
AD[6]	P4	AD[22]	B1	IRDY#	F1
AD[7]	N4	AD[23]	B2	TRDY#	G3
AD[8]	P3	AD[24]	B4	STOP#	H1
AD[9]	N3	AD[25]	A5	DEVSEL#	H3
AD[10]	N2	AD[26]	B5	IDSEL	A4
AD[11]	M1	AD[27]	B6	VIO	G2
AD[12]	M2	PAD[28]	C6		
AD[13]	M3	AD[29]	C7		
AD[14]	L1	AD[30]	A8		
AD[15]	L2	AD[31]	B8		

Table 15. PCI Arbitration Signals

Signal	Pin
REQ#	C3
GNT#	J3

Table 16. Interrupt Signals

Signal	Pin
INTA#	H2

Table 17. System Signals

Signal	Pin	Signal	Pin
CLK	G1	RST#	B9
M66EN	C2	CLK_RUN#	C8

Table 18. Error Reporting Signals

Signal	Pin	Signal	Pin
SERR#	A2	PERR#	J2

Table 19. Power Management Signals

Signal	Pin	Signal	Pin
PME#	A6	AUX_PWR	J12
LAN_PWR_GOOD	A9		

Table 20. SMB Signals

Signal	Pin	Signal	Pin	Signal	Pin
SMBCLK	A10	SMBDATA	C9	SMB_ALERT#	B10

Table 21. Serial EEPROM Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
EESK	M10	EEDI	P10	EECS	P7
EEDO	N10	EEMODE	J4		

Table 22. Serial FLASH Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
FLSH_SCK	N9	FLSH_SI	M11	FLSH_CE#	M9
FLSH_SO/LAN_DISABLE#	P9				

Table 23. LED Signals

Signal	Pin	Signal	Pin
LED0 / LINK_UP#	A12	LED2 / LINK100#	B11
LED1 / ACTIVITY#	C11	LED3 / LINK1000#	B12

Table 24. Other Signals

Signal	Pin	Signal	Pin
SDP[0]	N14	SDP[2]	N13
SDP[1]	P13	SDP[3]	M12

Table 25. IEEE Test Signals

Signal	Pin	Signal	Pin
IEEE_TEST-	D14	IEEE_TEST+	B14

Table 26. PHY Signals

Signal	Pin	Signal	Pin	Signal	Pin
MDI[0]-	C14	MDI[2]-	F14	XTAL1	K14
MDI[0]+	C13	MDI[2]+	F13	XTAL2	J14
MDI[1]-	E14	MDI[3]-	H14		
MDI[1]+	E13	MDI[3]+	H13		

Table 27. Test Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
JTAG_TCK	L14	JTAG_TDO	M14	JTAG_TRST#	L13
JTAG_TDI	M13	JTAG_TMS	L12	TEST	A13

Table 28. Digital Power Signals (Sheet 1 of 2)

Signal	Pin	Signal	Pin	Signal	Pin
3.3V	A3	1.2V	G5	1.2V	J9
3.3V	A7	1.2V	G6	1.2V	K10
3.3V	A11	1.2V	H5	1.2V	K11
3.3V	E1	1.2V	H6	1.2V	K5
3.3V	K3	1.2V	H7	1.2V	K6
3.3V	K4	1.2V	H8	1.2V	K7
3.3V	K13	1.2V	J10	1.2V	K8
3.3V	N6	1.2V	J11	1.2V	K9
3.3V	N8	1.2V	J5	1.2V	L10

Table 28. Digital Power Signals (Sheet 2 of 2) (Continued)

Signal	Pin	Signal	Pin	Signal	Pin
3.3V	P2	1.2V	J6	1.2V	L4
3.3V	P12	1.2V	J7	1.2V	L5
		1.2V	J8	1.2V	L9

Table 29. Analog Power Signals

Signal	Pin	Signal	Pin	Signal	Pin
ANALOG_1.2V	E11	ANALOG_1.8V	D11	CLKR_1.8V	D12
ANALOG_1.2V	E12	ANALOG_1.8V	G12	XTAL_1.8V	J13
ANALOG_1.2V	G13	PLL_1.2V	G4		
ANALOG_1.2V	H11	PLL_1.2V	H4		

Table 30. Grounds and No Connect Signals

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VSS	B3	VSS	F10	VSS	L11	NC	D10
VSS	B7	VSS	F4	VSS	L6	NC	D9
VSS	C10	VSS	F5	VSS	M6	NC	H12
VSS	D5	VSS	F6	VSS	N1	NC	L8
VSS	D6	VSS	F7	VSS	N12	NC	P1
VSS	D7	VSS	F8	VSS	P8	NC	P14
VSS	D8	VSS	F9	AVSS	C12	RSVD_NC	C5
VSS	E10	VSS	G10	AVSS	D13	RSVD_NC	L7
VSS	E2	VSS	G7	AVSS	F11	RSVD_NC	M8
VSS	E5	VSS	G8	AVSS	G11	RSVD_NC	N11
VSS	E6	VSS	G9	AVSS	G14	RSVD_NC	F12
VSS	E7	VSS	H10	AVSS	K12	RSVD_VSS	D4
VSS	E8	VSS	H9	NC	A1	RSVD_VSS	E4
VSS	E9	VSS	K2	NC	A14		

Table 31. Voltage Regulation Control Signals

Signal	Pin	Signal	Pin
CTRL18	B13	CTRL12	P11

Table 32. Signal Names in Pin Order (Sheet 1 of 6)

Signal Name	Pin
NC	A1
SERR#	A2
3.3V	A3
IDSEL	A4
AD[25]	A5
PME#	A6
3.3V	A7
AD[30]	A8
LAN_PWR_GOOD	A9
SMBCLK	A10
3.3V	A11
LED0 / LINK_UP#	A12
TEST	A13
NC	A14
AD[22]	B1
AD[23]	B2
VSS	B3
AD[24]	B4
AD[26]	B5
AD[27]	B6
VSS	B7
AD[31]	B8
RST#	B9
SMB_ALERT#	B10
LED2 / LINK100#	B11
LED3 / LINK1000#	B12
CTRL18	B13
IEEE_TEST+	B14
AD[21]	C1
M66EN	C2
REQ#	C3
C/BE#[3]	C4
RSVD_NC	C5

Table 32. Signal Names in Pin Order (Sheet 2 of 6) (Continued)

Signal Name	Pin
AD[28]	C6
AD[29]	C7
CLK_RUN#	C8
SMBDATA	C9
VSS	C10
LED1 / ACTIVITY#	C11
AVSS	C12
MDI[0]+	C13
MDI[0]-	C14
AD[18]	D1
AD[19]	D2
AD[20]	D3
RSVD_VSS	D4
VSS	D5
VSS	D6
VSS	D7
VSS	D8
NC	D9
NC	D10
ANALOG_1.8V	D11
CLKR_1.8V	D12
AVSS	D13
IEEE_TEST-	D14
3.3V	E1
VSS	E2
AD[17]	E3
RSVD_VSS	E4
VSS	E5
VSS	E6
VSS	E7
VSS	E8
VSS	E9
VSS	E10
ANALOG_1.2V	E11
ANALOG_1.2V	E12

Table 32. Signal Names in Pin Order (Sheet 3 of 6) (Continued)

Signal Name	Pin
MDI[1]+	E13
MDI[1]-	E14
IRDY#	F1
FRAME#	F2
C/BE#[2]	F3
VSS	F4
VSS	F5
VSS	F6
VSS	F7
VSS	F8
VSS	F9
VSS	F10
AVSS	F11
RSVD_NC	F12
MDI[2]+	F13
MDI[2]-	F14
CLK	G1
VIO	G2
TRDY#	G3
PLL_1.2V	G4
1.2V	G5
1.2V	G6
VSS	G7
VSS	G8
VSS	G9
VSS	G10
AVSS	G11
ANALOG_1.8V	G12
ANALOG_1.2V	G13
AVSS	G14
STOP#	H1
INTA#	H2
DEVSEL#	H3
PLL_1.2V	H4
1.2V	H5

Table 32. Signal Names in Pin Order (Sheet 4 of 6) (Continued)

Signal Name	Pin
1.2V	H6
1.2V	H7
1.2V	H8
VSS	H9
VSS	H10
ANALOG_1.2V	H11
NC	H12
MDI[3]+	H13
MDI[3]-	H14
PAR	J1
PERR#	J2
GNT#	J3
EEMODE	J4
1.2V	J5
1.2V	J6
1.2V	J7
1.2V	J8
1.2V	J9
1.2V	J10
1.2V	J11
AUX_PWR	J12
XTAL_1.8V	J13
XTAL2	J14
AD[16]	K1
VSS	K2
3.3V	K3
3.3V	K4
1.2V	K5
1.2V	K6
1.2V	K7
1.2V	K8
1.2V	K9
1.2V	K10
1.2V	K11
AVSS	K12

Table 32. Signal Names in Pin Order (Sheet 5 of 6) (Continued)

Signal Name	Pin
3.3V	K13
XTAL1	K14
AD[14]	L1
AD[15]	L2
C/BE#[1]	L3
1.2V	L4
1.2V	L5
VSS	L6
RSVD_NC	L7
NC	L8
1.2V	L9
1.2V	L10
VSS	L11
JTAG_TMS	L12
JTAG_TRST#	L13
JTAG_TCK	L14
AD[11]	M1
AD[12]	M2
AD[13]	M3
C/BE#[0]	M4
AD[5]	M5
VSS	M6
AD[1]	M7
RSVD_NC	M8
FLSH_CE#	M9
EESK	M10
FLSH_SI	M11
SDP[3]	M12
JTAG_TDI	M13
JTAG_TDO	M14
VSS	N1
AD[10]	N2
AD[9]	N3
AD[7]	N4
AD[4]	N5

Table 32. Signal Names in Pin Order (Sheet 6 of 6) (Continued)

Signal Name	Pin
3.3V	N6
AD[0]	N7
3.3V	N8
FLSH_SCK	N9
EEDO	N10
RSVD_NC	N11
VSS	N12
SDP[2]	N13
SDP[0]	N14
NC	P1
3.3V	P2
AD[8]	P3
AD[6]	P4
AD[3]	P5
AD[2]	P6
EECS	P7
VSS	P8
FLSH_SO	P9
EEDI	P10
CTRL12	P11
3.3V	P12
SDP[1]	P13
NC	P14

5.4 Visual Pin Assignments

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	NC	AD[22]	AD[21]	AD[18]	3.3V	IRDY#	CLK	STOP#	PAR	AD[16]	AD[14]	AD[11]	VSS	NC
2	SERR#	AD[23]	M66EN	AD[19]	VSS	FRAME#	VIO	INTA#	PERR#	VSS	AD[15]	AD[12]	AD[10]	3.3V
3	3.3V	VSS	REQ#	AD[20]	AD[17]	C/BE#[2]	TRDY#	DVSEL#	GNT#	3.3V	C/B3#[1]	AD[13]	AD[9]	AD[8]
4	IDSEL	AD[24]	C/BE#[3]	RSVD_ VSS	RSVD_ VSS	VSS	PLL_ 1.2V	PLL_ 1.2V	EEMODE	3.3V	1.2V	C/BE#[0]	AD[7]	AD[6]
5	AD[25]	AD[26]	RSVD_ NC	VSS	VSS	VSS	1.2V	1.2V	1.2V	1.2V	1.2V	AD[5]	AD[4]	AD[3]
6	PME#	AD[27]	AD[28]	VSS	VSS	VSS	1.2V	1.2V	1.2V	1.2V	VSS	VSS	3.3V	AD[2]
7	3.3V	VSS	AD[29]	VSS	VSS	VSS	VSS	1.2V	1.2V	1.2V	RSVD_ NC	AD[1]	AD[0]	EECS
8	AD[30]	AD[31]	CLK_ RUN#	VSS	VSS	VSS	VSS	1.2V	1.2V	1.2V	NC	RSVD_ NC	3.3V	VSS
9	LAN_ PWR_ GOOD	RST#	SMBDATA	NC	VSS	VSS	VSS	VSS	1.2V	1.2V	1.2V	FLSH_ CE#	FLSH_ SCK	FLSH_ SO
10	SMBCLK	SMB_ ALERT	VSS	NC	VSS	VSS	VSS	VSS	1.2V	1.2V	1.2V	EESK	EEDO	EEDI
11	3.3V	LED2/ LINK 100#	LED1/ ACTIVITY#	ANALOG_ 1.8V	ANALOG_ 1.2V	AVSS	AVSS	ANALOG_ 1.2V	1.2V	1.2V	VSS	FLSH_ SI	RSVD_ NC	CTRL12
12	LED0/ LINK_ UP#	LED3/ LINK 1000#	AVSS	CLKR_ 1.8V	ANALOG_ 1.2V	RSVD_ NC	ANALOG_ 1.8V	NC	AUX_ PWR	AVSS	JTAG_ TMS	SDP[3]	VSS	3.3V
13	TEST	CTRL18	MDI[0]+	AVSS	MDI[1]+	MDI[2]+	ANALOG_ 1.2V	MDI[3]+	XTAL_ 1.8V	3.3V	JTAG_ TRST#	JTAG_ TDI	SDP[2]	SDP[1]
14	NC	IEEE_ TEST+	MDI[0]-	IEEE_ TEST-	MDI[1]-	MDI[2]-	AVSS	MDI[3]-	XTAL2	XTAL1	JTAG_ TCK	JTAG_ TDO	SDP[0]	NC

Figure 13. Visual Pin Assignments

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