

LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ SCSI & IDE Interfaces
- ✓ Parallel & Serial Port Protection (RS-232)
- ✓ Ethernet - 10/100 Base T
- ✓ Test & Measurement Equipment
- ✓ Industrial Control: Low Voltage Sensors

IEC COMPATIBILITY (EN61000-4)

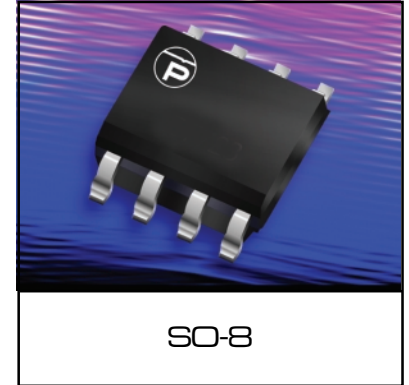
- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 12A, 8/20 μ s - Level 1(Line-Gnd) & Level 2(Line-Line)

FEATURES

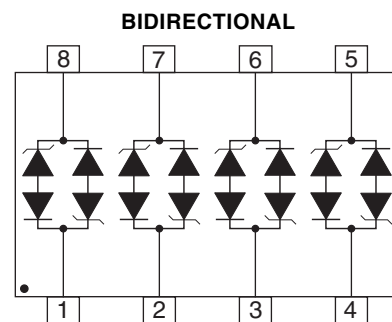
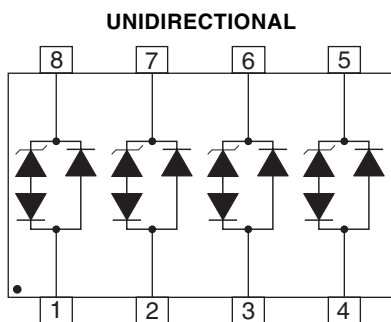
- ✓ 500 Watts Peak Pulse Power per Line ($t_p=8/20\mu$ s)
- ✓ Unidirectional & Bidirectional Configurations
- ✓ Available in Multiple Voltage Types Ranging From 3V to 24V
- ✓ Protects Up to Four (4) Lines
- ✓ ESD Protection > 40 kilovolts
- ✓ **LOW CAPACITANCE: 15pF**

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8 Package
- ✓ Weight 15 milligrams (Approximate)
- ✓ Flammability rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Logo, Marking Code, Date Code & Pin One Defined By Dot on Top of Package



PIN CONFIGURATIONS



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C
Forward Voltage @ 50mA, 300μs - Square Wave (Note 1)	V_F	1.5	Volts

Note 1: Only applies to unidirectional devices.

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (See Note 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_P = 1A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20μs $V_C @ I_{PP}$	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D μA	MAXIMUM CAPACITANCE 0V @ 1 MHz C pF
SMDA03LC	SLA	3.3	4.5	7.0	10.9V @ 43.0A	125	15
SMDA03LCC	SLB	3.3	4.5	7.0	10.9V @ 43.0A	125	15
SMDA05LC	SLC	5.0	6.0	9.8	13.5V @ 42.0A	20	15
SMDA05LCC	SLD	5.0	6.0	9.8	13.5V @ 42.0A	20	15
SMDA08LC	SLE	8.0	8.5	13.4	16.9V @ 34.0A	10	15
SMDA08LCC	SLF	8.0	8.5	13.4	16.9V @ 34.0A	10	15
SMDA12LC	SLG	12.0	13.3	19.0	25.9V @ 27.0A	1	15
SMDA12LCC	SLH	12.0	13.3	19.0	25.9V @ 27.0A	1	15
SMDA15LC	SLJ	15.0	16.7	24.0	30.0V @ 17.0A	1	15
SMDA15LCC	SLK	15.0	16.7	24.0	30.0V @ 17.0A	1	15
SMDA24LC	SLL	24.0	26.7	43.0	49.0V @ 12.0A	1	15
SMDA24LCC	SLM	24.0	26.7	43.0	49.0V @ 12.0A	1	15

Note 1: Part numbers with a "C" suffix are bidirectional devices, i.e., SMDA03LCC.

GRAPHS

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

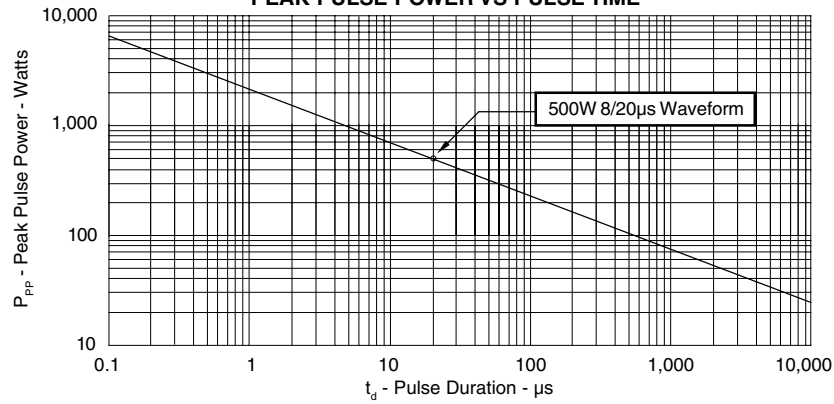


FIGURE 2
PULSE WAVE FORM

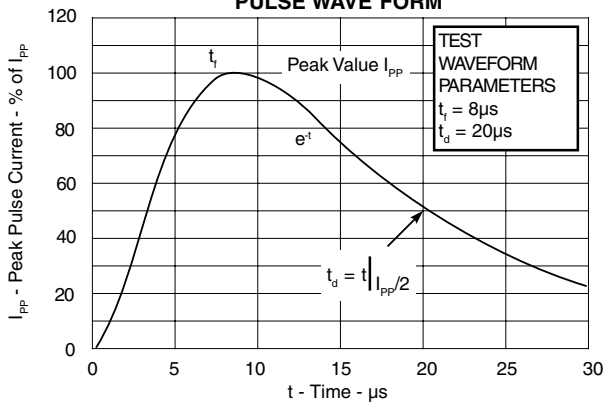


FIGURE 3
POWER DERATING CURVE

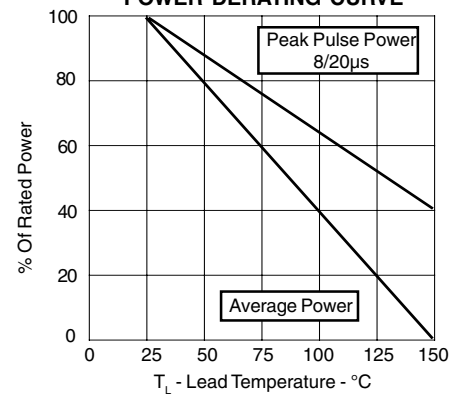
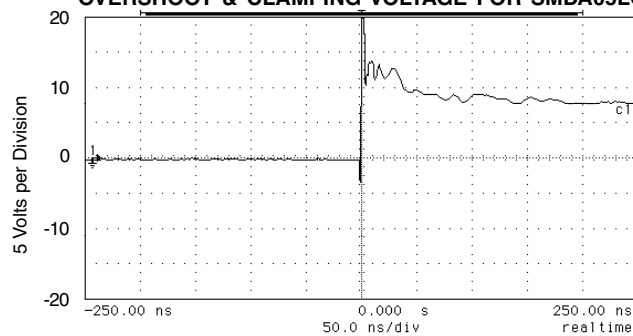


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR SMDA05LC



APPLICATION NOTE

The SMDAxxLC & SMDAxxLCC Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD, EFT and other types of surges. This product series provides both unidirectional and bidirectional protection, with a surge capability of 500 Watts P_{PP} per line for an 8/20 μ s waveform and ESD protection > 40kV.

UNIDIRECTIONAL COMMON-MODE CONFIGURATION(Figure 1)

The SMDAxxLC Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 5.
- ✓ Line 2 is connected to Pin 6.
- ✓ Line 3 is connected to Pin 7.
- ✓ Line 4 is connected to Pin 8.
- ✓ Pins 1-4 are connected to ground.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 2)

Ideal for Ethernet applications, SMDAxxLCC Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ TPIN is connected to Pin 5.
- ✓ TPIP is connected to Pin 6.
- ✓ TPON is connected to Pin 1.
- ✓ TPOP is connected to Pin 2.
- ✓ Pins 3, 4, 7 & 8 are connected to ground.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1. Unidirectional Common-Mode Protection

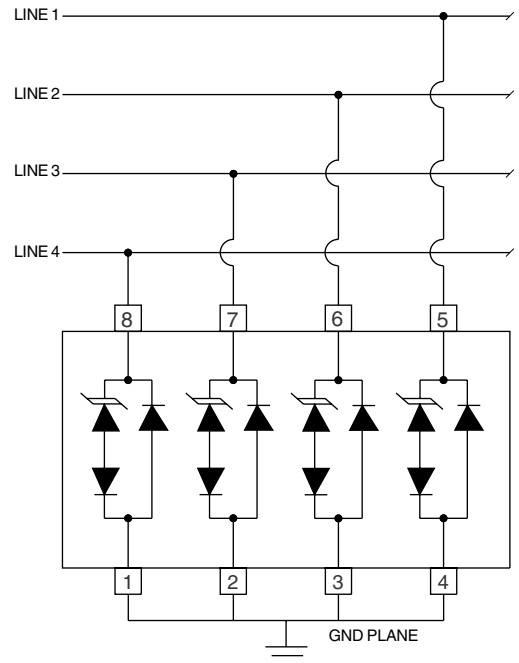
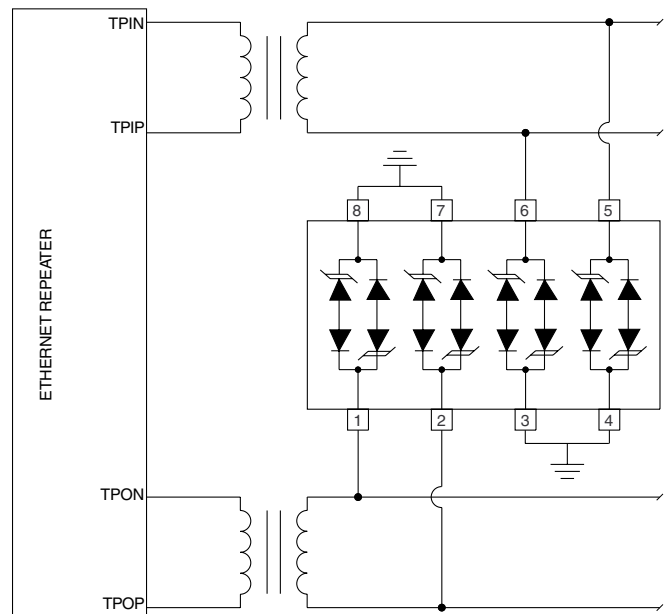
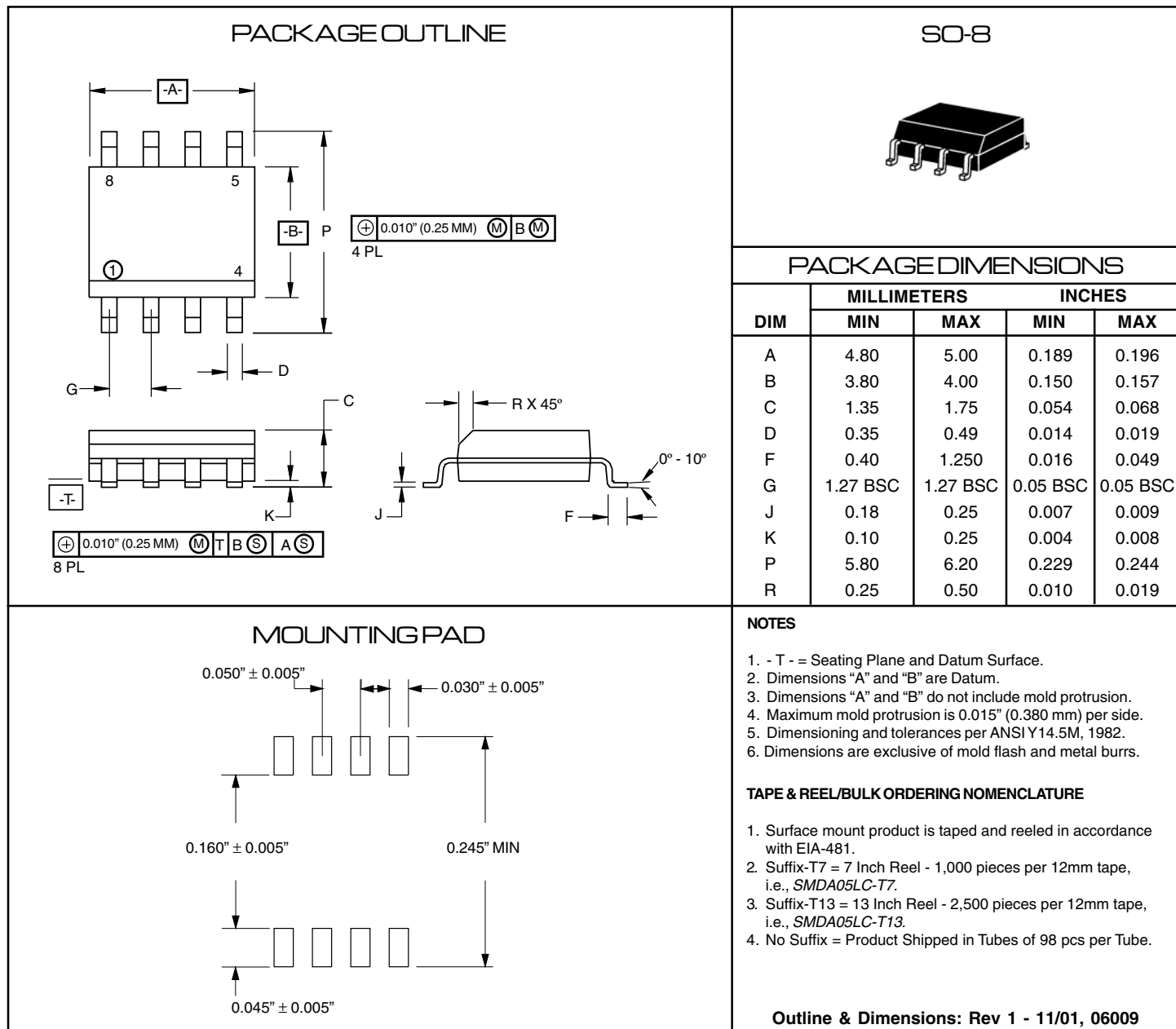


Figure 2. Bidirectional Common-Mode Protection



PACKAGE OUTLINE & DIMENSIONS



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