

# 74ACTQ74

## Quiet Series Dual D-Type Positive Edge-Triggered Flip-Flop

### Features

- $I_{CC}$  reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- 4kV minimum ESD immunity
- TTL-compatible inputs

### General Description

The 74ACTQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary ( $Q$ ,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

The ACTQ74 utilizes Fairchild Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### Asynchronous Inputs:

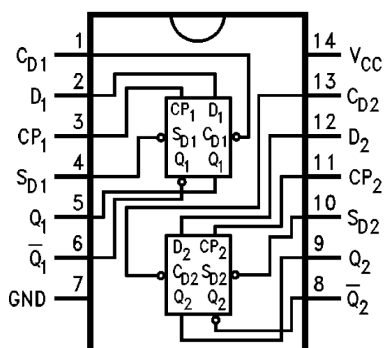
- LOW input to  $\bar{S}_D$  (Set) sets  $Q$  to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets  $Q$  to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both  $Q$  and  $\bar{Q}$  HIGH

### Ordering Information

Order Number	Package Number	Package Description
74ACTQ74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACTQ74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

### Connection Diagram

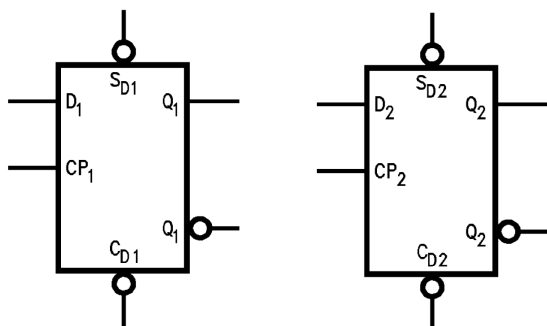


### Pin Descriptions

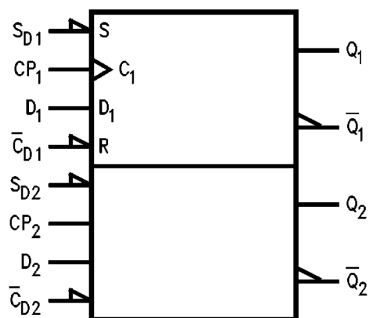
Pin Names	Description
$D_1, D_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

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## Logic Symbols



## IEEE/IEC



## Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	$Q_0$	$\overline{Q}_0$

H = HIGH Voltage Level

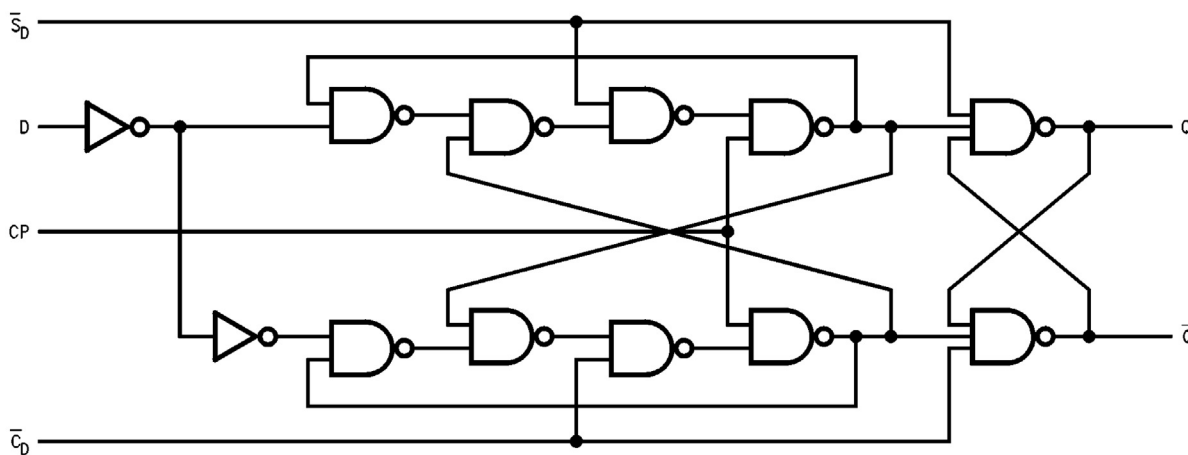
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

$Q_0(\overline{Q}_0)$  = Previous  $Q(\overline{Q})$  before LOW-to-HIGH Transition of Clock

## Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	−20mA +20mA
$V_I$	DC Input Voltage	−0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	−20mA +20mA
$V_O$	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	±50mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	±50mA
$T_{STG}$	Storage Temperature	−65°C to +150°C
	DC Latch-Up Source or Sink Current	±300mA
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	4.5	1.5	2.0	2.0		V
			5.5	1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	4.5	1.5	0.8	0.8		V
			5.5	1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	I <sub>OUT</sub> = −50 μA	4.5	4.49	4.4	4.4		V
			5.5	5.49	5.4	5.4		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OH</sub> = −24mA	4.5		3.86	3.76		
		I <sub>OH</sub> = −24mA <sup>(1)</sup>	5.5		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	I <sub>OUT</sub> = 50μA	4.5	0.001	0.1	0.1		V
			5.5	0.001	0.1	0.1		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OL</sub> = 24mA	4.5		0.36	0.44		
		I <sub>OL</sub> = 24mA <sup>(1)</sup>	5.5		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>I</sub> = V <sub>CC</sub> , GND	5.5		±0.1	±1.0		μA
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>O</sub> = V <sub>CC</sub> , GND	5.5		±0.5	±5.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	V <sub>I</sub> = V <sub>CC</sub> − 2.1V	5.5	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(1)</sup>	V <sub>OLD</sub> = 1.65V Max.	5.5			75		mA
I <sub>OHD</sub>		V <sub>OHD</sub> = 3.85V Min.	5.5			−75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5		2.0	20.0		μA
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	Figures 1 & 2 <sup>(3)</sup>	5.0	1.1	1.5			V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	Figures 1 & 2 <sup>(3)</sup>	5.0	−0.6	−1.2			V
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	<sup>(4)</sup>	5.0	1.9	2.2			V
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	<sup>(4)</sup>	5.0	1.2	0.8			V

## Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.
4. Max number of data inputs (n) switching. (n - 1) inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1MHz.

## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V) <sup>(5)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{\text{MAX}}$	Maximum Clock Frequency	5.0	145	200		125		MHz
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$	5.0	3.0	7.0	8.5	3.0	9.0	ns
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$	5.0	3.0	6.5	8.0	3.0	8.6	ns
$t_{\text{OSLH}}, t_{\text{OSHL}}$	Output to Output Skew <sup>(6)</sup>	5.0		0.5	1.0		1.0	ns

### Notes:

5. Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{\text{OSHL}}$ ) or LOW-to-HIGH ( $t_{\text{OSLH}}$ ). Parameter guaranteed by design.

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		T <sub>A</sub> = −40°C to +85°C, C <sub>L</sub> = 50pF	Units
			Typ.	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW, D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, D <sub>n</sub> to CP <sub>n</sub>	5.0	−0.5	1.5	1.5	ns
t <sub>W</sub>	CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ , Pulse Width	5.0	3.0	4.0	4.0	ns
t <sub>REC</sub>	Recovery Time, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	1.5	1.5	ns

### Note:

7. Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## Capacitance

Symbol	Parameter	Conditions	Typ.	Units
$C_{\text{IN}}$	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
$C_{\text{PD}}$	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	60.0	pF

## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

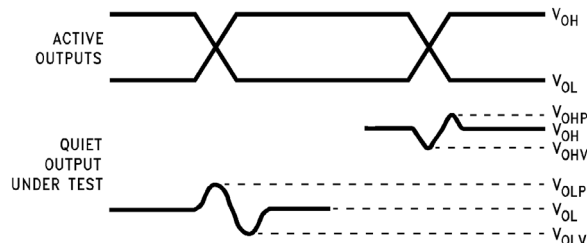
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.



### Notes:

8.  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.
9. Input pulses have the following characteristics:  
 $f = 1\text{MHz}$ ,  $t_r = 3\text{ns}$ ,  $t_f = 3\text{ns}$ , skew < 150ps.

**Figure 1. Quiet Output Noise Voltage Waveforms**

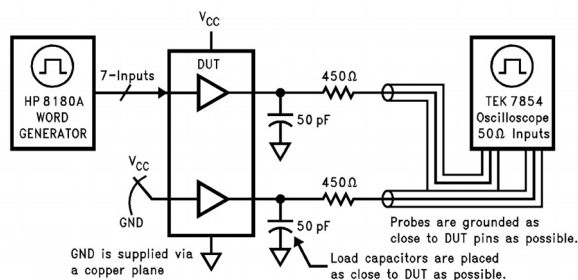
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

### $V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case transition for active and enable. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case transition for active and enable.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

### $V_{ILD}$ and $V_{IHD}$ :

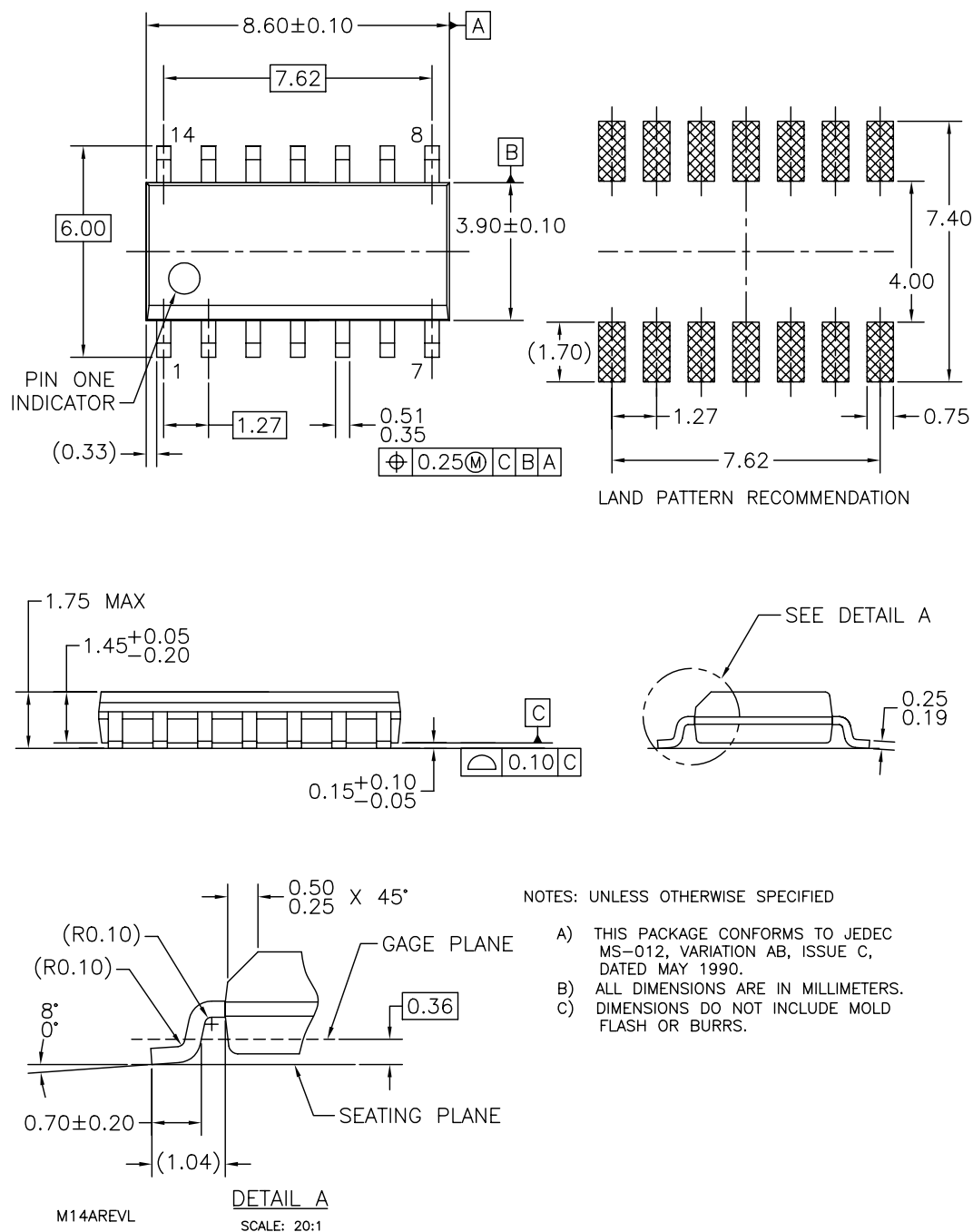
- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.



**Figure 2. Simultaneous Switching Test Circuit**

## Physical Dimensions

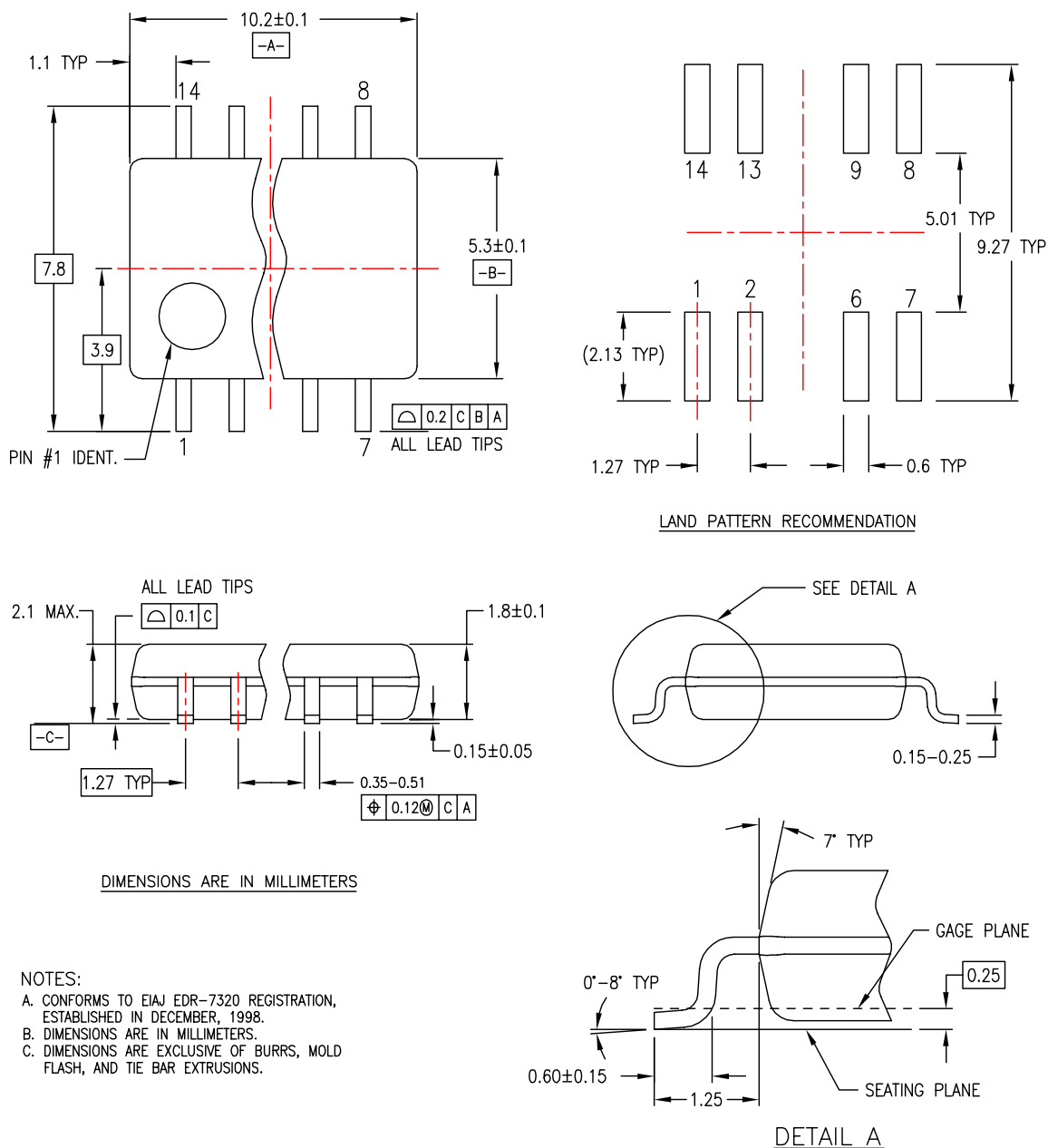
Dimensions are in inches (millimeters) unless otherwise noted.



**Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**

# Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




M14DREVC

**Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**



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FACT <sup>®</sup>	PACMAN <sup>™</sup>	SuperSOT <sup>™</sup> -3	
FAST <sup>®</sup>	PDP-SPM <sup>™</sup>	SuperSOT <sup>™</sup> -6	
FASTr <sup>™</sup>	POP <sup>™</sup>	SuperSOT <sup>™</sup> -8	
FPS <sup>™</sup>	Power220 <sup>®</sup>	SyncFET <sup>™</sup>	
FRFET <sup>®</sup>	Power247 <sup>®</sup>	TCM <sup>™</sup>	
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Datasheet Identification	Product Status	Definition
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