

3MHz, 2.4A Step Down Converter

Description

LX7167 is a step-down PWM Switching Regulator IC with integrated high side P-CH and low side N-CH MOSFETs. The IC operates using a hysteretic control topology with a full load operating switching frequency of 3MHz allowing small output filter components while maintaining excellent dynamic load response.

The operational input voltage range of LX7167 is from 3V to 5.5V. The part has a Power Save Mode (PSM) that automatically transitions between PWM and PSM mode depending on the load current. This allows the converter's efficiency to remain high when load current drops. There is a Power Good function to indicate the status of the IC.

In the shutdown mode, the IC's current consumption is reduced to less than 1 μ A and the output capacitor is discharged.

Other features of the part are: a) Cycle-by-cycle current limit followed by HICCUP mode which reduces the overall power dissipation of the internal MOSFETs, b) thermal protection and internal digital soft start.

The LX7167 is available in a 2mm x 2mm 8 pin exposed pad DFN package.

Features

- 2.4A Step-down Regulator
- Operational Input Supply Voltage Range: 3V-5.5V
- Integrated PMOS and NMOS
- Load Current from Zero to 2.4A
- 3MHz Switching Frequency
- SKIP Pulse to Improve Light Load Efficiency
- Input UVLO and OV Protection
- Enable Pin
- Power Good
- Internal Soft-start
- Cycle-by-Cycle Over Current Protection
- Hiccup Mode Operation Under FB UVLO
- RoHS Compliant for Pb Free

Applications

- HDD
- Set-Top Box
- LCD TV's
- Notebook/Netbook
- Routers
- Video Cards
- PC Peripherals
- PoE Powered Devices Smart Phone

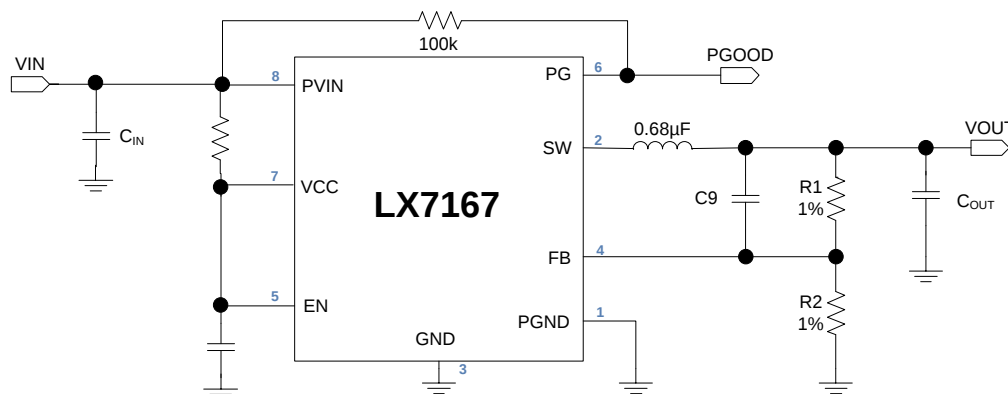


Figure 1 · Typical Application of LX7167

Pin Configuration and Pinout

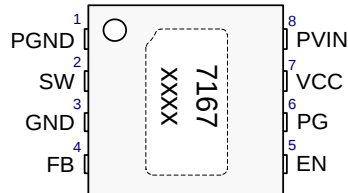


Figure 2 · Pinout DFN 2mmx2mm 8L Top View

Marking: First Line 7167

Second Line YWWA (Year/Work Week/Lot Code)

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-10°C to 85°C	RoHS Compliant, Pb-free	DFN 2mmx2mm 8L	LX7167CLD	Bulk / Tube
			LX7167CLD-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	PGND	Ground pin for the power stage.
2	SW	Switch-node pin. Connect the output inductor between this pin and output capacitor. When the chip is DISABLED, the internal discharge resistor will be enabled to discharge the output capacitance. The current will flow into this pin.
3	GND	Ground pin.
4	FB	Voltage feedback pin. Connect to the output terminal through a resistor divider network to set the output voltage of the regulator to the desired value.
5	EN	Pull this pin higher than 1V will enable the controller. When pulled low, the IC will turn off and the Internal discharge FET will turn on to discharge the output capacitor through the SW pin.
6	PG	Power-good pin. This is an open-drain output and should be connected to a voltage rail with an external pull-up resistor. During the power on, this pin switches from LOW to HI state when FB voltage reaches above the power good threshold and the internal soft start has finished its operation. It will be pulled low when the FB falls below the power-good threshold minus the hysteresis. It will turn back on when the pull FB rises above the threshold.
7	VCC	Analog input voltage terminal. Connect this pin to VIN with a 10ohm resistor and connect a 1μF ceramic capacitor from VCC to GND.
8	PVIN	Input voltage terminal of the regulator. A minimum of 10μF, X5R type ceramic capacitor must be connected as close as possible from this pin to PGND plane to insure proper operation.
	Power PAD	For good thermal connection, this PAD must be connected using thermal VIAs to the GND plane and to the LAND pattern of the IC.

Block Diagram

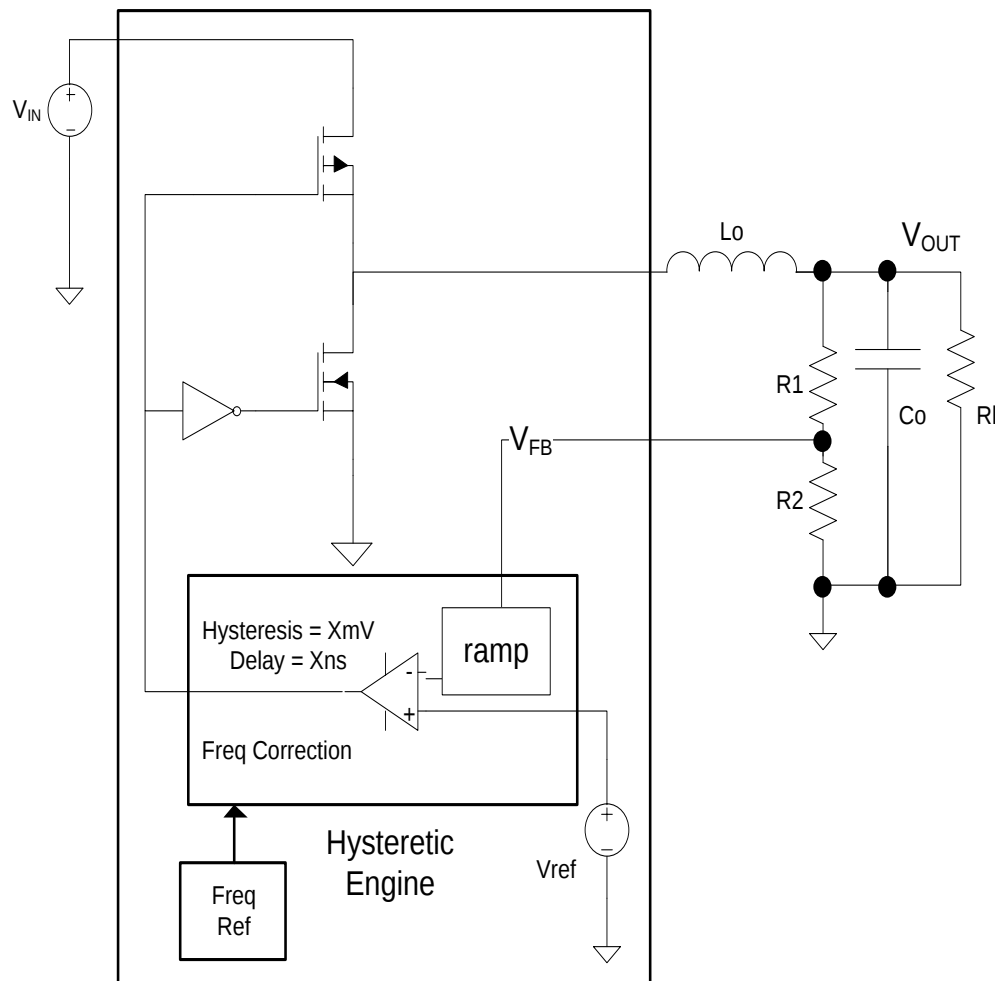


Figure 3 · Simplified Block Diagram of LX7167

Absolute Maximum Ratings

Parameter	Min	Max	Units
PVIN, EN, FB, PG to GND	-0.3	7	V
SW to GND	-0.3	7	V
SW to GND (Shorter than 50ns)	-2	7	V
Junction Temperature	0	150	°C
Storage Temperature	-65	150	°C
Peak Package Solder Reflow Temperature (40s, reflow)		260 (+0,-5)	°C

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

Parameter	Min	Max	Units
VCC, PVIN	3	5.5	V
V _{OUT}	0.6	V _{IN} – 0.5	V
Ambient Temperature	-10	85	°C
Output Current	0	2.4	A

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	75	°C/W

Note: The θ_{JA} number assumes no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: Unless otherwise specified, the following specifications apply over the operating ambient temperature of $-10^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ except where otherwise noted with the following test conditions: VCC = PVIN = 5V. Typical parameter refers to $T_J = 25^{\circ}\text{C}$

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Operating Current						
I _Q	Input Current	I _{LOAD} = 0		350		μA
I _{SHDN}	Input Current at Shut Down	V _{EN} = GND		0.1	2	μA
PVIN Input UVLO						
PVIN	Under Voltage Lockout	PVIN rising		2.4	2.8	V
	UVLO Hysteresis			260		mV

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
FEEDBACK						
V _{REF}	Feedback Voltage	T _A = 25°C	0.594	0.600	0.606	V
		-10°C to 85°C	0.591		0.609	
I _{FB}	FB Pin Input Current				10	nA
	Line Regulation	PVIN from 3V to 5.5V		0.70		%
	Load Regulation	I _{LOAD} = 0 to 2A. Note 1		1.0		%/A
FB UVLO						
V _{FBUVLO}	FB UVLO Threshold			70		%V _{REF}
OUTPUT DEVICE						
R _{DS(on)_H}	R _{DS(on)} of High Side			95	150	mΩ
R _{DS(on)_L}	R _{DS(on)} of Low Side			75	100	mΩ
I _L	Peak Current Limit		2.6	3.5	4.5	A
T _{SH}	Thermal Shutdown Threshold			150		°C
T _H	Thermal Shutdown Hysteresis			20		°C
PVIN OVP						
OVP _R	Rising Threshold			6.1		V
OVP _F	Falling Threshold		5.5			V
OSCILLATOR FREQUENCY						
f	Switching Frequency		2.6	3	3.4	MHz
SOFT START						
T _{SS}	Soft Start Time	From EN High to V _{OUT} reach regulation		500		μs
T _{HICCUP}	Hiccup Time	V _{FB} = 0.2V		1.2		ms
EN INPUT						
EN _{VIN}	Input High		1			V
EN _{VIL}	Input Low				0.4	V
EN _H	Hysteresis			0.1		V
EN _{II}	Input Bias			0.01	1	μA
PG (Power Good)						
V _{PG}	Power Good Transition High Threshold			83		%
V _{PGHY}	Hysteresis	Either V _{FB} rising or falling		40		mV
PG _{RDS(on)}	Power Good Internal FET R _{DS(on)}	VCC = 5V		100	300	Ω
	PG FET Leakage Current			0.01	1	μA
	PG internal Glitch Filter	Note 1		5		μs
OUTPUT DISCHARGE						
	Internal Discharge Resistor		80	200	1400	Ω

Note 1: Guaranteed by design, not tested during production.

Typical Performance Curves -- (Efficiency)

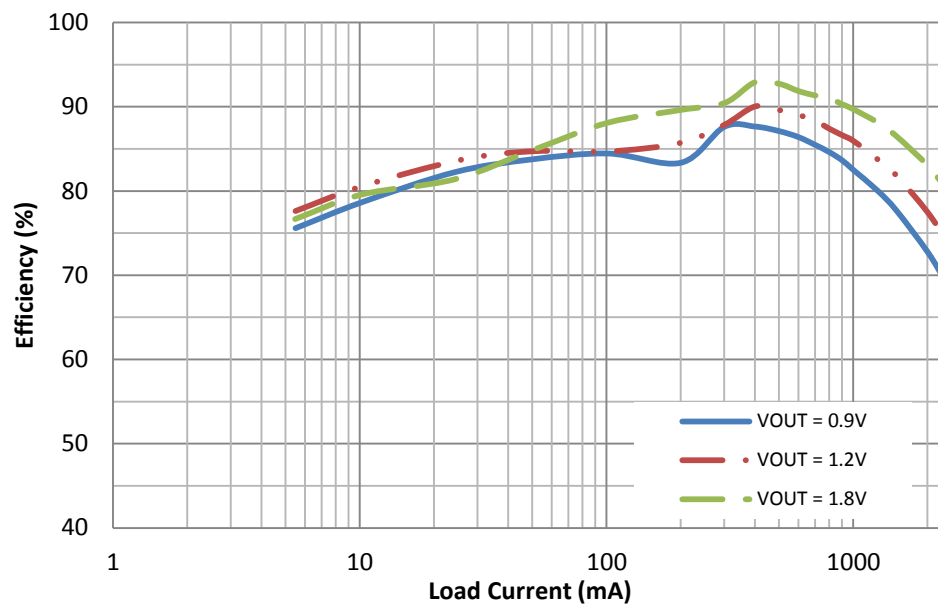


Figure 4 · Efficiency vs. Output Current with 3.3V Input

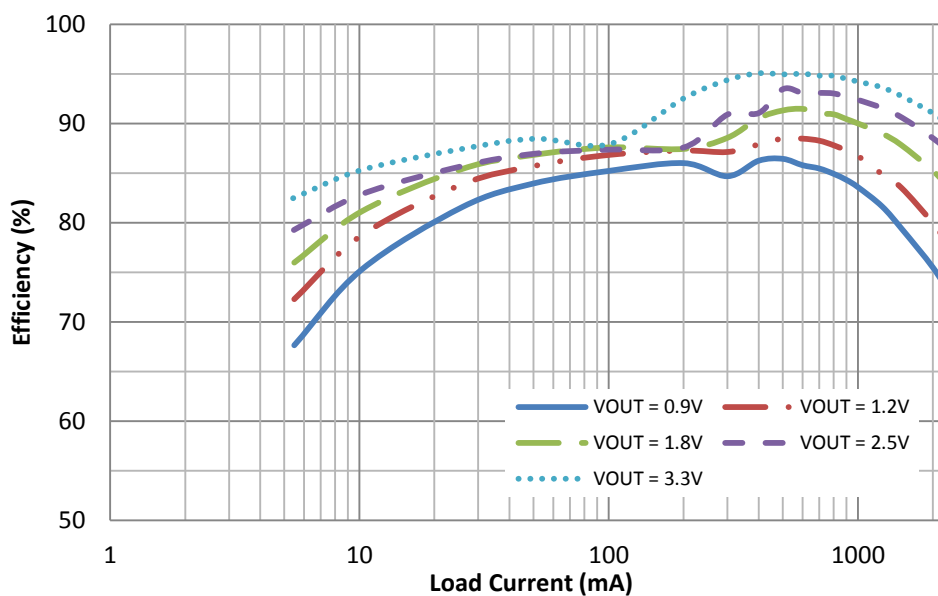


Figure 5 · Efficiency vs. Output Current with 5V Input

Typical Performance Curves -- (Step Load Response.)

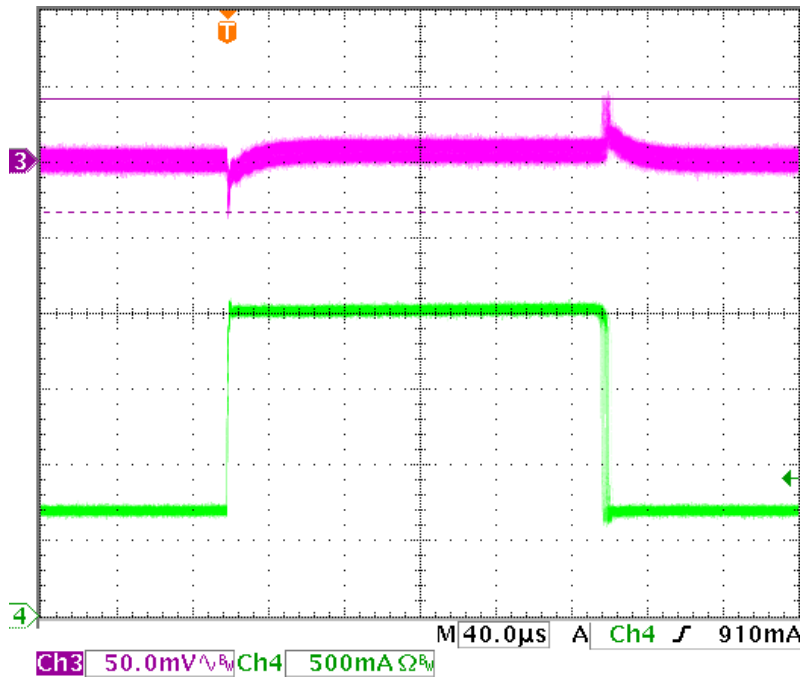


Figure 6 · **Step Response** ($V_{IN} = 5V$, $V_{OUT} = 3.3V$, $L = 0.47\mu H$, $C_{OUT} = 22\mu F$)

Theory of Operation / Application Information

Basic Operation

The operation of the controller consists of comparing the V_{FB} voltage to an internal reference. When the V_{FB} voltage is lower than the V_{REF} , the upper switch turns on. When the V_{FB} voltage is higher than V_{REF} , the upper switch turns off and the lower switch turns on. An internal ramp is used to stabilize the switching frequency and keep the V_{FB} immune to the output capacitor, C_O , value or parasitic components (i.e. esr, esl). In addition, a frequency control loop ensures the switching frequency is constant under continuous conduction mode of operation.

At light load, the converter automatically reduces the switching frequency to optimize efficiency while ensuring the ripple voltage is low.

Setting of the Output Voltage

The LX7167A develops a 0.6V reference voltage between the feedback pin, FB, and the signal ground. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

The output component values are recommended below.

VOUT	L	R1	R2	COUT	C9	
					5V input	3.3V input
1V	0.47μH & 0.68μH	66.5kΩ	100kΩ	22μF	10pF	
				2x22μF	15pF	
				4x22μF	22pF	
	1.0μH			22μF	15pF	12pF
				2x22μF	22pF	22pF
				4x22μF	27pF	27pF
1.8V	0.47μH & 0.68μH	100kΩ	49.9kΩ	22μF	10pF	
				2x22μF	15pF	
				4x22μF	22pF	
	1.0μH			22μF	15pF	
				2x22μF	22pF	
				4x22μF	27pF	
2.5V	0.47μH & 0.68μH	158kΩ	49.9kΩ	22μF	15pF	
				2x22μF	22pF	
				4x22μF	33pF	
	1.0μH			22μF	10pF	22pF
				2x22μF	15pF	27pF
				4x22μF	22pF	33pF
3.3V	0.47μH & 0.68μH	158kΩ	34.8kΩ	22μF	22pF	-
				2x22μF	33pF	-
				4x22μF	47pF	-
	1.0μH			22μF	22pF	-
				2x22μF	33pF	-
				4x22μF	47pF	-

Start Up

The reference (V_{REF}) is ramped up from zero voltage to 0.6V in 500 μ s. During this time, the PG is pulled low. When the reference reaches 0.6V, signaling the end of the soft start cycle, the PG pin will go high within 5 μ s.

Over Current Protection

The IC has the ability to protect against all types of short circuit protection. It has cycle by cycle short protection that turns off the upper MOSFET and ends the cycle when the current exceeds the OCP threshold, when this occurs, the off-time is at least 200ns before the upper FET is turned on again. After startup, if the FB pin drops below the Feedback UVLO threshold, the chip will go into a hiccup mode of operation. This helps to protect against a crowbar short circuit. The FB UVLO Alarm is not active during startup.

Hiccup Mode of Operation

Hiccup mode of operation will protect the IC during a short of the output. After startup, it will be triggered when the FB UVLO is exceeded.

Input Over Voltage Protection

The IC is protected against damage when the input voltage rapidly rises to the absolute maximum level. When the input voltage rises over the PVIN OVP rising threshold, the IC will turn off switching. It will resume switching when the input voltage drops below the PVIN OVP falling threshold with hysteresis.

Typical Application Diagram

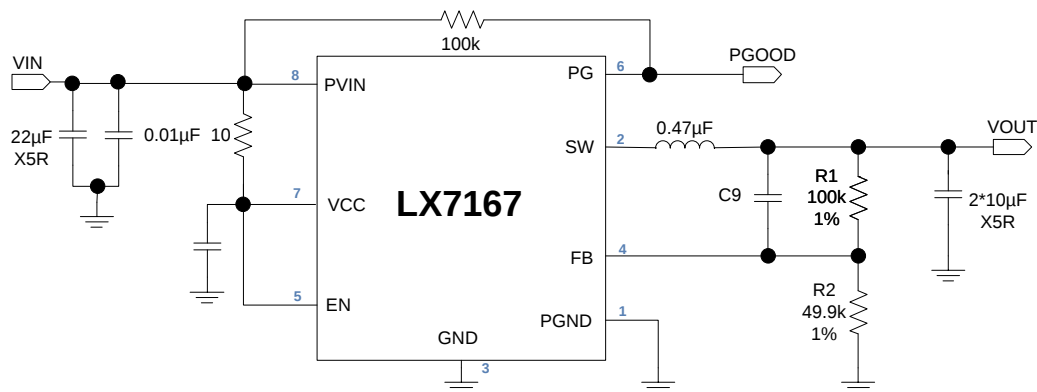


Figure 7 · LX7167 Typical Application Diagram

PACKAGE OUTLINE DIMENSIONS

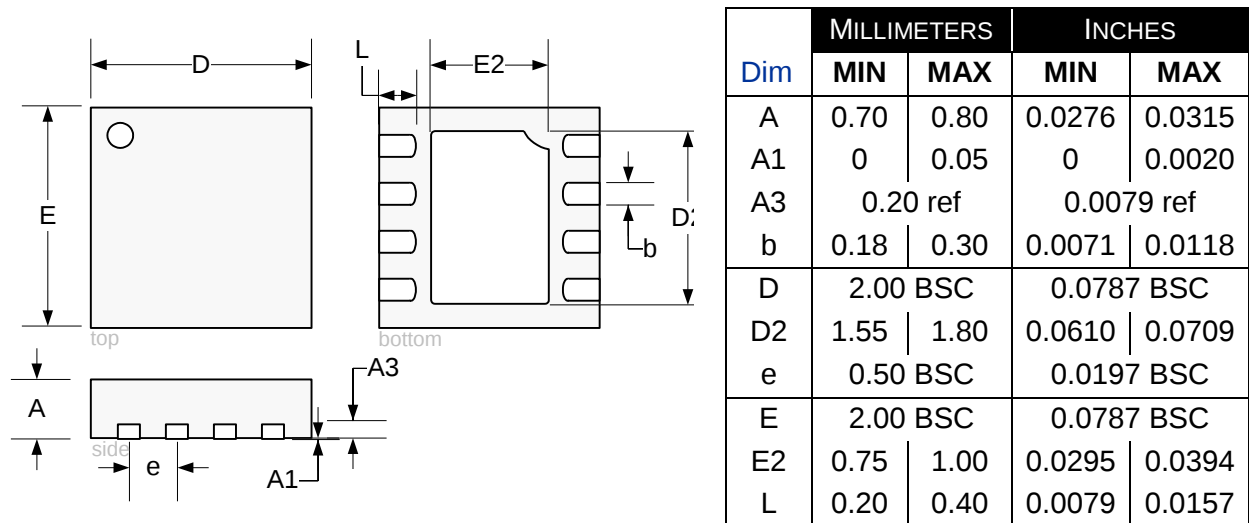


Figure 8 · 8 Pin Plastic DFN 2x2mm Dual Exposed Pad Package Dimensions

Note: 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

Note: 2. Dimensions are in mm, inches are for reference only.

LAND PATTERN RECOMMENDATION

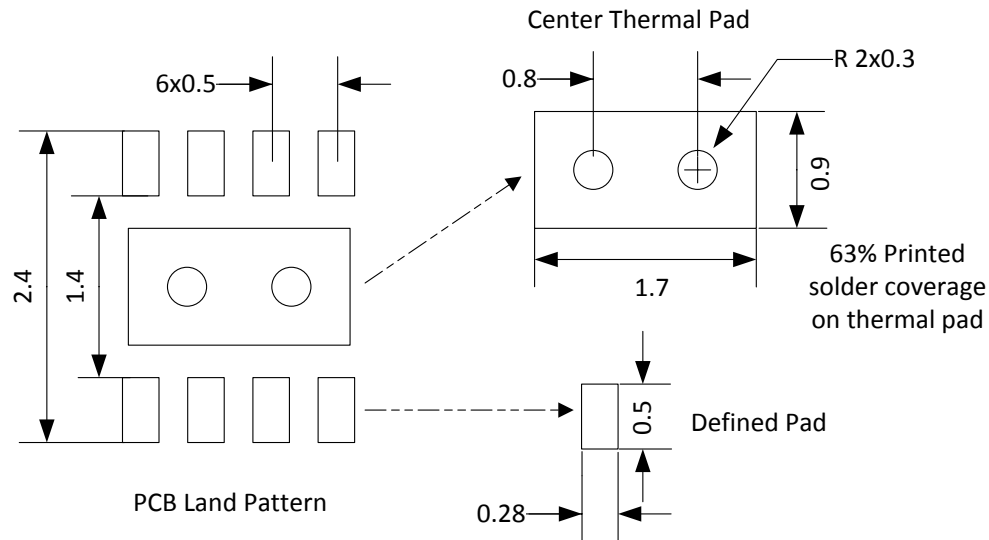


Figure 9 · 8 Pin Plastic DFN 2x2mm Dual Exposed Pad Package Footprint

Disclaimer:

This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern.

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