

8-Bit Registers

Features

- Function and pinout compatible with FCT and F logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 5.2 ns max. (Com'l)
FCT-A speed at 6.5 ns max. (Com'l)
- Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 12 mA (Com'l),
12 mA (Mil)
- Source current 15 mA (Com'l),
12 mA (Mil)
- Edge-triggered D-type inputs
- 250 MHz typical toggle rate

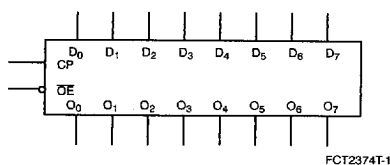
Functional Description

The FCT2374T and FCT2574T are high-speed low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2374T and FCT2574T can be used to replace the FCT374T and FCT574T to reduce noise in an existing design. Both devices have three-state outputs for bus oriented

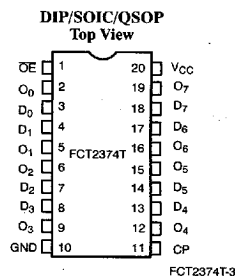
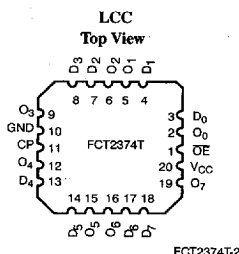
applications. A buffered clock (CP) and output enable (OE) are common to all flip-flops. The FCT2574T is identical to FCT2374T except that all the outputs are on one side of the package and inputs on the other side. The flip-flops contained in the FCT2374T and FCT2574T will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. When OE is LOW, the contents of the flip-flops are available at the outputs. When OE is HIGH, the outputs will be in the high-impedence state. The state of output enable does not affect the state of the flip-flops.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

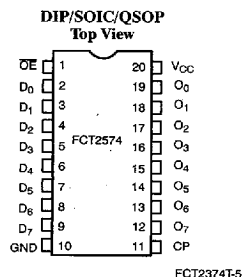
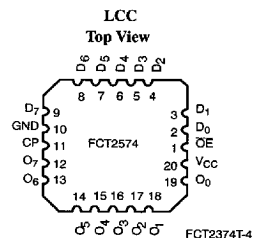
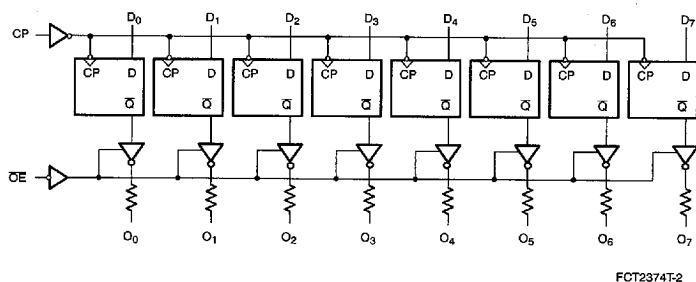
Logic Symbol



Pin Configurations



Logic Block Diagram



Function Table^[1]

Inputs			Outputs
D	CP	OE	O
H		L	H
L		L	L
X	X	H	Z

Maximum Ratings^[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA Com'l	20	25	40	Ω
		V _{CC} =Min., I _{OL} =12 mA Mil		25		Ω
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Hysteresis ^[6]	All inputs		0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA

Notes:

- H = HIGH Voltage Level.
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
┐ = LOW-to-HIGH clock transition
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance		5	10	pF
C _{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, f ₀ =10 MHz OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, f ₀ =10 MHz OE=GND, V _{IN} =3.4V or V _{IN} =GND	1.2	3.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, Fo=10 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.6	3.2 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, Fo=10 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	3.9	12.2 ^[11]	mA

- Notes:**
- Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
 - This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
 - $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{\text{HNT}} + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_{H} = Duty Cycle for TTL inputs HIGH
 - N_T = Number of TTL inputs at D_H
 - I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 - f₀ = Clock frequency for registered devices, otherwise zero
 - f₁ = Input signal frequency
 - N₁ = Number of inputs changing at f₁
- All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2374T/FCT2574T				FCT2374AT/FCT2574AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t _W	Clk Pulse Width HIGH or LOW	6.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT2374CT/FCT2574CT				FCT2374DT/ FCT2574DT		Unit	Fig. No. [13]
		Military		Commercial		Commercial			
		Min. [12]	Max.	Min. [12]	Max.	Min. [12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	6.5	2.0	5.2	2.0	4.2	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.9	1.5	6.2	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	6.5	1.5	5.0	1.5	4.0	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW D to CP	2.0		1.5		2.0		ns	4
t _H	Hold Time, HIGH or LOW D to CP	1.0		1.0		1.0		ns	4
t _W	Clk Pulse Width HIGH or LOW	5.0		4.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT2374DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2374DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT2374CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2374CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2374CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2374CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2374CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT2374ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2374ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2374ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT2374ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2374ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT2374TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2374TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2374TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2374TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2374TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT2574DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2574DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT2574CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2574CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2574CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2574CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2574CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT2574ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2574ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2574ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT2574TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2574ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT2574TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2574TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2574TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2574TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2574TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

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