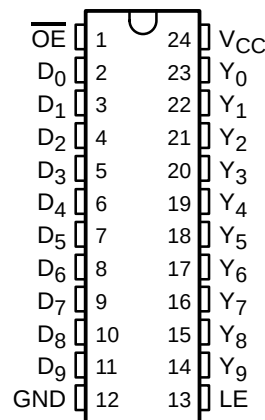


CY54FCT841T, CY74FCT841T 10-BIT LATCHES WITH 3-STATE OUTPUTS

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- Function, Pinout, and Drive Compatible With FCT, F, and AM29841 Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- High-Speed Parallel Latches
- Buffered Common Latch-Enable Input
- 3-State Outputs
- CY54FCT841T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT841T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

CY54FCT841T . . . D PACKAGE
CY74FCT841T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



description

The 'FCT841T bus-interface latches are designed to eliminate additional packages required to buffer existing latches and provide additional data width for wider address/data paths or buses carrying parity. The 'FCT841T devices are buffered 10-bit-wide versions of the FCT373 function.

The 'FCT841T devices' high-performance interface is designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	Latch data inputs
LE	I	Latch-enable input. The latches are transparent when LE is high. Input data is latched on the high-to-low transition.
Y	O	3-state latch outputs
$\overline{OE}$	I	Output-enable control. When $\overline{OE}$ is low, the outputs are enabled. When $\overline{OE}$ is high, the outputs are in the high-impedance (off) state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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 WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.5	CY74FCT841CTQCT	FCT841C
	SOIC – SO	Tube	5.5	CY74FCT841CTSOC	FCT841C
		Tape and reel	5.5	CY74FCT841CTSOCT	
	DIP – P	Tube	6.5	CY74FCT841BTPC	CY74FCT841BTPC
	SOIC – SO	Tube	9	CY74FCT841ATSOC	FCT841A
		Tape and reel	9	CY74FCT841ATSOCT	
–55°C to 125°C	CDIP – D	Tube	10	CY54FCT841ATDMB	

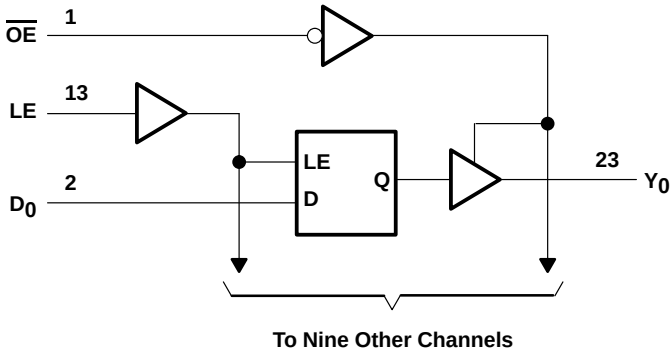
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	LE	D	O	Y	
H	X	X	X	Z	Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

H = High logic level, L = Low logic level, X = Don't care, NC = No change, Z = High-impedance state

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	67°C/W
(see Note 2): Q package	61°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	CY54FCT841T			CY74FCT841T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–12			–32	mA
I_{OL} Low-level output current			32			64	mA
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY54FCT841T, CY74FCT841T

10-BIT LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT841T			CY74FCT841T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$				-0.7	-1.2		
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OH} = -32 \text{ mA}$				2			
	$I_{OH} = -15 \text{ mA}$				2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 32 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 2.7 \text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0.5 \text{ V}$						± 1	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$			10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$						10	
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$			-10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$						-10	
$I_{OS}^\ddagger$	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
I_{off}	$V_{CC} = 0 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 3.4 \text{ V}^\S$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 3.4 \text{ V}^\S$, $f_1 = 0$, Outputs open				0.5	2		
$I_{CCD}^\P$	$V_{CC} = 5.5 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.06	0.12					mA/ MHz
	$V_{CC} = 5.25 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.06	0.12		

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT841T		CY74FCT841T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	
I _C [#]	V _{CC} = 5.5 V, Outputs open, OE = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4				mA
			V _{IN} = 3.4 V or GND	1	2.4				
		10 bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1	3.2				
			V _{IN} = 3.4 V or GND	4.1	13.2				
	V _{CC} = 5.25 V, Outputs open, OE = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7	1.4		
			V _{IN} = 3.4 V or GND			1	2.4		
		10 bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			1	3.2		
			V _{IN} = 3.4 V or GND			4.1	13.2		
C _i				5	10	5	10	pF	
C ₀				9	12	9	12	pF	

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT841AT		CY74FCT841AT		CY74FCT841BT		CY74FCT841CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	5		4		4		4		ns
t_{su}	Setup time, data before $LE\uparrow$	2.5		2.5		2.5		2.5		ns
t_h	Hold time, data after $LE\uparrow$	3		2.5		2.5		2.5		ns

CY54FCT841T, CY74FCT841T

10-BIT LATCHES

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switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT841AT		CY74FCT841AT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	10	1.5	9	ns
t _{PHL}				1.5	10	1.5	9	
t _{PLH}	D	Y	C _L = 300 pF, R _L = 500 Ω	1.5	15	1.5	13	ns
t _{PHL}				1.5	15	1.5	13	
t _{PLH}	LE	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	12	ns
t _{PHL}				1.5	13	1.5	12	
t _{PLH}	LE	Y	C _L = 300 pF, R _L = 500 Ω	1.5	20	1.5	16	ns
t _{PHL}				1.5	20	1.5	16	
t _{PZH}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	11.5	ns
t _{PZL}				1.5	13	1.5	11.5	
t _{PZH}	$\overline{OE}$	Y	C _L = 300 pF, R _L = 500 Ω	1.5	25	1.5	23	ns
t _{PZL}				1.5	25	1.5	23	
t _{PHZ}	$\overline{OE}$	Y	C _L = 5 pF, R _L = 500 Ω	1.5	9	1.5	7	ns
t _{PLZ}				1.5	9	1.5	7	
t _{PHZ}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	10	1.5	8	ns
t _{PLZ}				1.5	10	1.5	8	

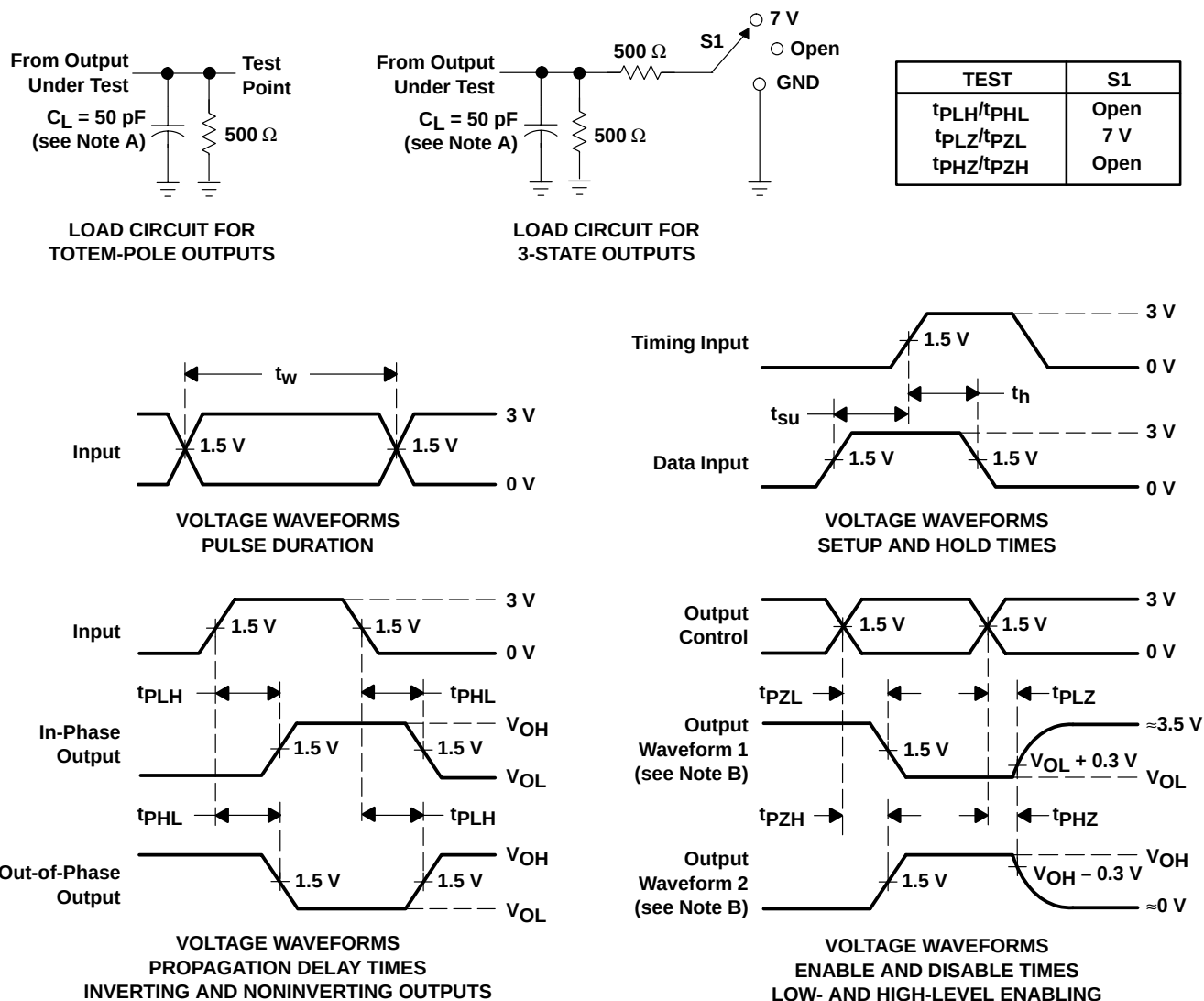
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT841BT		CY74FCT841CT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	6.5	1.5	5.5	ns
t _{PHL}				1.5	6.5	1.5	5.5	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	13	ns
t _{PHL}				1.5	13	1.5	13	
t _{PLH}	LE	Y	C _L = 50 pF, R _L = 500 Ω	1.5	8	1.5	6.4	ns
t _{PHL}				1.5	8	1.5	6.4	
t _{PLH}	LE	Y	C _L = 300 pF, R _L = 500 Ω	1.5	15.5	1.5	15	ns
t _{PHL}				1.5	15.5	1.5	15	
t _{PZH}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	8	1.5	6.5	ns
t _{PZL}				1.5	8	1.5	6.5	
t _{PZH}	$\overline{OE}$	Y	C _L = 300 pF, R _L = 500 Ω	1.5	14	1.5	12	ns
t _{PZL}				1.5	14	1.5	12	
t _{PHZ}	$\overline{OE}$	Y	C _L = 5 pF, R _L = 500 Ω	1.5	6	1.5	5.7	ns
t _{PLZ}				1.5	6	1.5	5.7	
t _{PHZ}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	7	1.5	6	ns
t _{PLZ}				1.5	7	1.5	6	



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY54FCT841ATDMB	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CY54FCT841ATDM B
CY74FCT841ATSOC	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841ATSOC.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841ATSOCT	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841ATSOCT.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841CTQCT	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT841C
CY74FCT841CTQCT.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT841C
CY74FCT841CTSOC	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C
CY74FCT841CTSOC.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C
CY74FCT841CTSOCT	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C
CY74FCT841CTSOCT.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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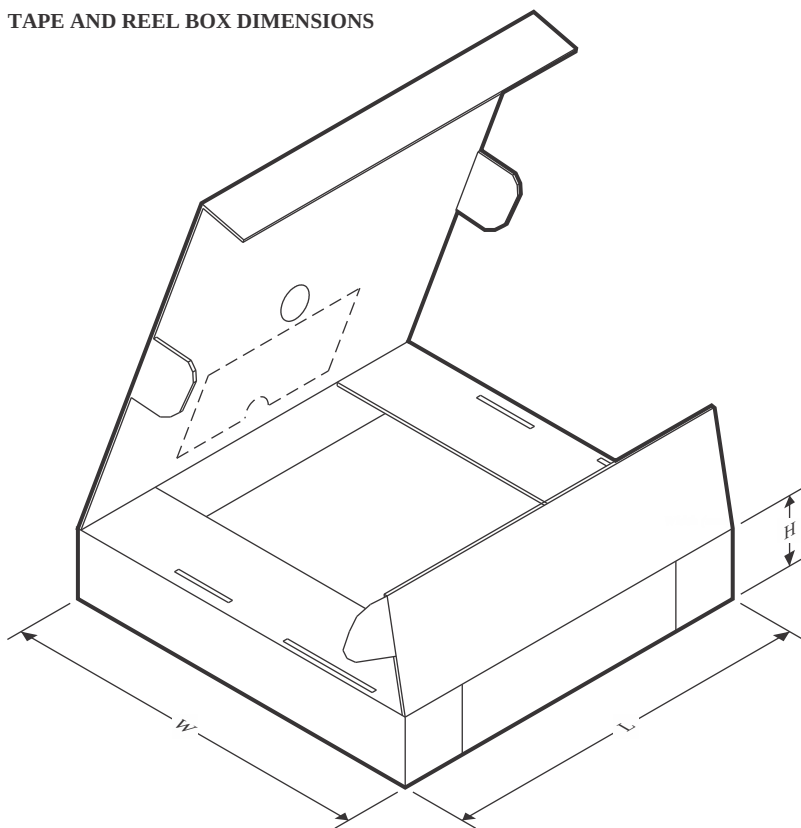
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT841ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT841CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT841CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

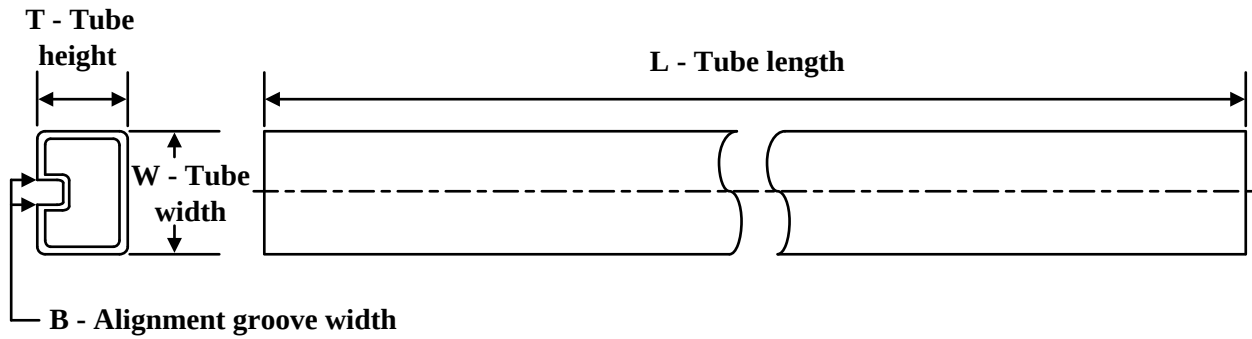
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT841ATSOCT	SOIC	DW	24	2000	350.0	350.0	43.0
CY74FCT841CTQCT	SSOP	DBQ	24	2500	353.0	353.0	32.0
CY74FCT841CTSOCT	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT841ATSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841ATSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841CTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841CTSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

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