W137

FTG for Mobile 440BX & Transmeta's Crusoe CPU

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum Technology**
- **Two copies of CPU output**
- **Six copies of PCI output (Synchronous w/CPU output)**
- **One 48-MHz output for USB support**
- **One selectable 24 /48 MHz output**
- **Two Buffered copies of 14.318 MHz input reference signal**
- **Supports 100 MHz or 66 MHz CPU operation**
- **Power management control input pins**
- **Available in 28-pin SSOP (209 mils) and 28-pin TSSO (173 mils)**
- **SS function can be disabled**
- **See W40S11-02 for 2 SDRAM DIMM support**

Key Specifications

Supply Voltages:.....V_{DDQ3} = 3.3V±5%
V_{DDQ2} = 2.5V±5%

CPU0:1 Output to Output Skew: ..... 175 ps

CPU0:1 Cycle to Cycle Jitter: ..... 200 ps

PCI_F, PCI1:5 Output to Output Skew:..... 500 ps

PCI_F, PCI1:5 Cycle to Cycle Jitter: ..... 250 ps

CPU to PCI Output Skew:.....1.5–4.0 ns (CPU Leads)

Output Duty Cycle:..... 45/55%

PCI_F, PCI Edge Rate: .....>1 V/ns

CPU_STOP#, OE, SPREAD#, SEL48#, PCI_STOP#, PWR_DWN# all have a 250-kW pull-up resistor.

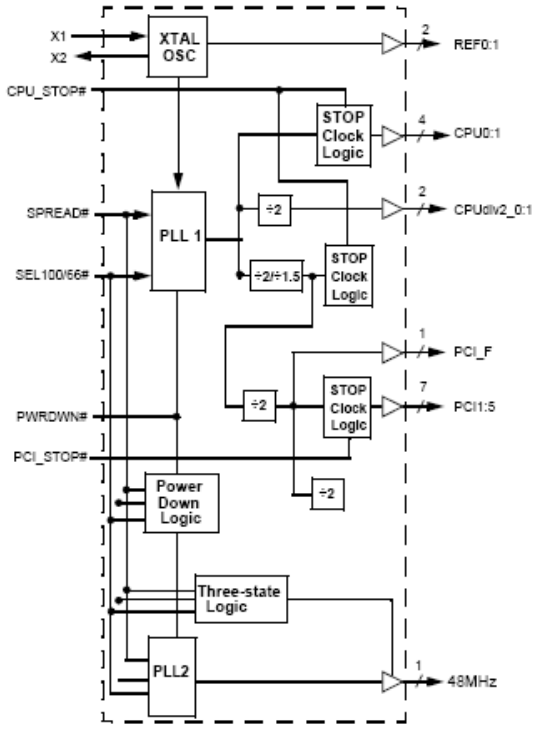
Table 1. Pin Selectable Frequency

SEL100/66#	OE	CPU	PCI	Spread%
0/1	0	Hi-Z	Hi-Z	Don't Care
0	1	66.6 MHz	33.3	See Table 2
1	1	100 MHz	33.3	See Table 2

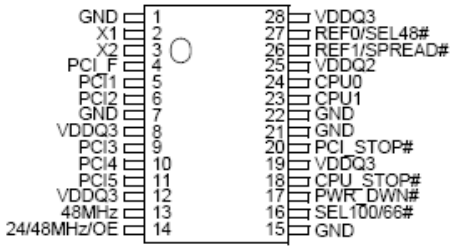
Table 2. Spread Spectrum Feature

SPREAD#	Spread Profile
0	–0.5% (down spread)
1	0% (spread disabled)

Block Diagram



Pin Configuration



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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	24, 23	O	CPU Clock Outputs 0 and 1. These two CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2. Frequency is selected per Table 1.
PCI1:5	5, 6, 9, 10, 11	O	PCI Bus Clock Outputs 1 through 5. These five PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3. Frequency is selected per Table 1.
PCI_F	4	O	Fixed PCI Clock Output. Unlike PCI1:5 outputs, this output is not controlled by the PCI_STOP# control pin; it cannot be forced LOW by PCI_STOP#. Output voltage swing is controlled by voltage applied to VDDQ3. Frequency is selected per Table 1.
CPU_STOP#	18	I	CPU_STOP# Input. When brought LOW, clock outputs CPU0:1 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:1 start with a full clock cycle (2–3 CPU clock latency).
PCI_STOP#	20	I	PCI_STOP# Input. The PCI_STOP# input enables the PCI1:5 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP# signal is latched on the rising edge of PCI_F. Its effect takes place on the next PCI_F clock cycle.
REF0/SEL48#	27	I/O	I/O Dual-Function REF0 and SEL48# Pin. Upon power-up, the state of SEL48# is latched. The state is set by either a 10K resistor to GND or to V_{DD}. A 10K resistor to GND causes pin 14 to provide a 48-MHz clock. If the pin is strapped to V_{DD}, pin 14 will provide a 24-MHz clock. After 2 ms, the pin becomes a high-drive output that produces a copy of 14.318 MHz.
REF1/SPREAD#	26	I/O	I/O Dual-Function REF1 and SPREAD# Pin. Upon power-up, the state of SPREAD# is latched. The state is set by either a 10K resistor to GND or to V_{DD}. A 10K resistor to GND enables Spread Spectrum function. If the pin is strapped to V_{DD}, Spread Spectrum is disabled. After 2 ms, the pin becomes a high-drive output that produces a copy of 14.318 MHz.
24/48MHz/OE	14	I/O	***I***/O Dual-Function 24 MHz or 48 MHz Output and Output Enable Input. Upon power-up, the state of pin 14 is latched. The state is set by either a 10K resistor to GND or to V_{DD}. A 10K resistor to GND latches OE LOW, and all outputs are tri-stated. If the pin is strapped to V_{DD}, OE is latched HIGH and all outputs are active. After 2 ms, the pin becomes an output whose frequency is set by the state of pin 27 on power-up.
48MHz	13	O	48 MHz Output. Fixed 48 MHz USB output. Output voltage swing is controlled by voltage applied to VDDQ3.
SEL100/66#	16	I	Frequency Selection Input. Select power-up default CPU clock frequency as shown in Table 1.
X1	2	I	Crystal Connection or External Reference Frequency Input. This pin can either be used as a connection to a crystal or to a reference signal.
X2	3	I	Crystal Connection. An input connection for an external 14.318 MHz crystal. If using an external reference, this pin must be left unconnected.
PWR_DWN#	17	I	Power Down Control. When this input is LOW, device goes into a low-power standby condition. All outputs are held LOW. CPU and PCI clock outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock cycle latency). When brought HIGH, CPU and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
VDDQ3	8, 12, 19, 28	P	Power Connection. Connected to 3.3V.
VDDQ2	25	P	Power Connection. Power supply for CPU0:1 output buffers. Connected to 2.5V.
GND	1, 7, 15, 21, 22	G	Ground Connection. Connect all ground pins to the common system ground plane.

Overview

The W137 was developed to meet the Intel® Mobile Clock specification for the BX chipset, including Super I/O and USB support. The W40S11-02 is the Intel-defined companion part used for driving 2 SDRAM DIMM modules. Please see that data sheet for additional information.

Cypress's proprietary spread spectrum frequency synthesis technique is a feature of the CPU and PCI outputs. When enabled, this feature reduces the peak EMI measurements of not only the output signals and their harmonics, but also of any other clock signals that are properly synchronized to them. The –0.5% modulation profile matches that defined as acceptable in Intel's clock specification.

Functional Description

I/O Pin Operation

Pins 14, 26, and 27 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and the pins then become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-kΩ "strapping" resistor is connected between each I/O pin and ground or VDD. Connection to ground sets a latch to "0," connection to VDD sets a latch to "1." Figure 1 and Figure 2 show two suggested methods for strapping resistor connection.

Upon W137 power-up, the first 2 ms of operation are used for input logic selection. During this period the output buffers are tri-stated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or logic LOW state. At the end of the 2-ms period, the established logic 0 or 1 condition of each I/O pin is then latched. Next, the output buffers are enabled, which converts both I/O pins into operating clock outputs. The 2-ms timer is started when V_{DD} reaches 2.0V. The input latches can only be reset by turning V_{DD} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of the clock output is <40Ω (nominal) which is minimally affected by the 10-kΩ strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, target (normal) output frequency is delivered assuming that V_{DD} has stabilized. If V_{DD} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DD} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

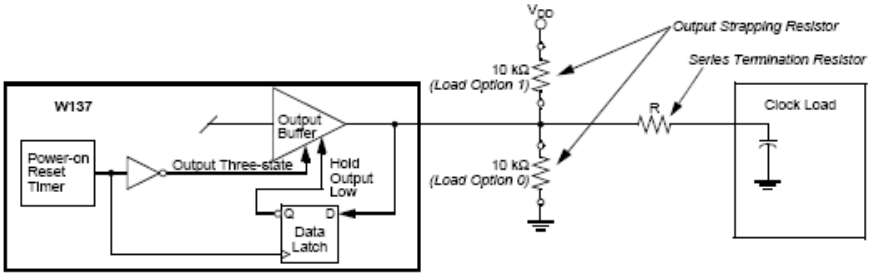

Figure 1. Input Logic Selection Through Resistor Load Option

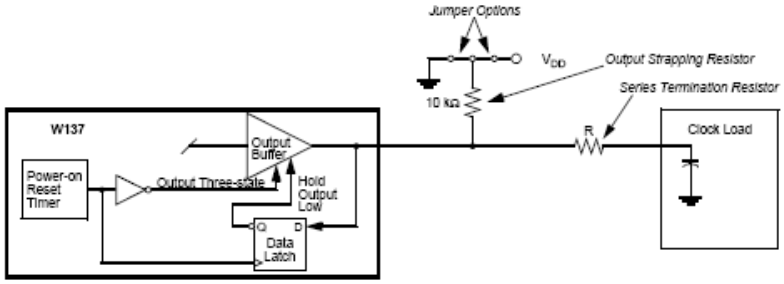

Figure 2. Input Logic Selection Through Jumper Option

Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is –0.5% of the selected frequency. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated through I/O pin #26.

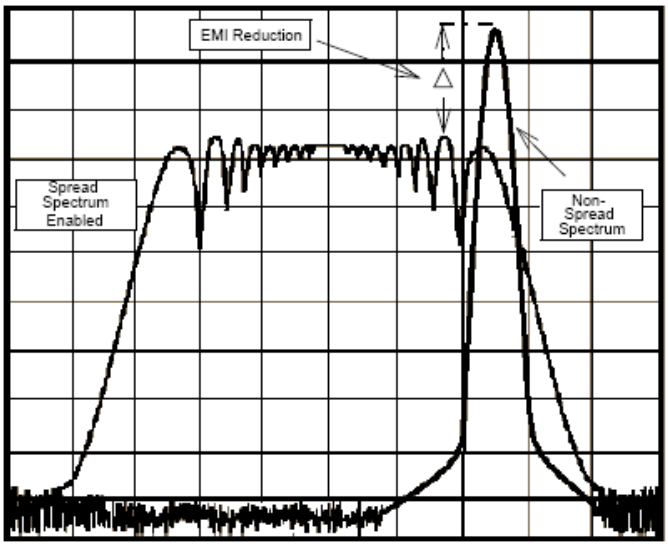

Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

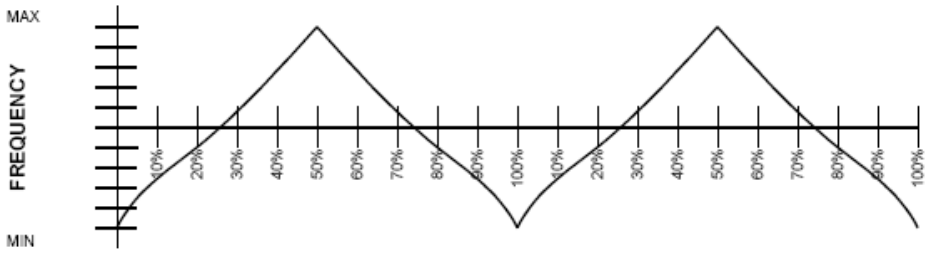

Figure 4. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics:

T_A = 0°C to +70°C; V_{DDQ3} = 3.3V±5%; V_{DDQ2} = 2.5V±5%; CPU0:1 = 66.6/100 MHz

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD3PD}	3.3V Supply Current in Power-down mode		PWR_DWN# = 0		1	5	mA
I_{DD3}	3.3V Supply Current		Outputs Loaded[1]		80	100	mA
I_{DD2}	2.5V Supply Current		Outputs Loaded[1]		30	45	mA
I_{DD2PD}	2.5V Supply Current in Power-down mode		PWR_DWN# = 0		0.2 µA	1	mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[2]					–25	µA
I_{IH}	Input High Current[2]					10	µA
I_{IL}	Input Low Current (SEL100/66#)					–5	µA
I_{IH}	Input High Current (SEL100/66#)					+5	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	PCI_F, PCI1:5, REF0:1	I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU0:1	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current:	CPU0:1	V_{OL} = 1.25V	80	120	180	mA
		PCI_F, PCI1:5	V_{OL} = 1.5V	70	110	140	mA
		REF0:1	V_{OL} = 1.5V	50	70	90	mA
I_{OH}	Output High Current	CPU0:1	V_{OH} = 1.25V	80	120	180	mA
		PCI_F, PCI1:5	V_{OH} = 1.5V	70	110	140	mA
		REF0:1	V_{OH} = 1.5V	50	70	90	mA
Crystal Oscillator							
V_{TH}	X1 Input Threshold Voltage[3]		V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, As Seen by External Crystal[4]				14		pF
$C_{IN,X1}$	X1 Input Capacitance[5]		Pin X2 unconnected		28		pF

Notes:
1. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
2. CPU_STOP#, PCI_STOP#, PWR_DWN#, SPREAD#, and SEL48# logic inputs have internal pull-up resistors (not CMOS level).
3. X1 input threshold voltage (typical) is $V_{DD}/2$.

DC Electrical Characteristics: (continued)

T_A = 0°C to +70°C; V_{DDQ3} = 3.3V±5%; V_{DDQ2} = 2.5V±5%; CPU0:1 = 66.6/100 MHz

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

AC Electrical Characteristics

T_A = 0°C to +70°C; V_{DDQ3} = 3.3V±5%; V_{DDQ2} = 2.5V±5%; f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			200			200	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		13.5			13.5		Ω

Notes:
4. The W137 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

PCI Clock Outputs, PCI1:5 and PCI_F (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12.0			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Offset	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4.0	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

REF0:1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Max.	Typ.	
f	Frequency, Actual	Determined by crystal oscillator frequency	14.318			MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

48 MHz and 24 MHz Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see n/m below)	48.008 24.004			MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48	+167			ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)	57/17, 57/34			
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

Ordering Information

Part Number	Type	Production Flow
W137H	28-pin SSOP	Commercial, 0 to 70°C
W137HT	28-pin SSOP -Tape and Reel	Commercial, 0 to 70°C
Lead-Free		
CYW137OXC	28-pin SSOP	Commercial, 0 to 70°C
CYW137OXCT	28-pin SSOP -Tape and Reel	Commercial, 0 to 70°C

Package Diagrams

28-Lead (5.3 mm) Shrunk Small Outline Package O28