RoHS Compliant

Value Added Compact Flash Series Ⅲ

Specification for Industrial CF

Mar 8, 2011

Version 1.0

Apacer
Access the best

Apacer Technology Inc.
4th Fl., 75 Hsin Tai Wu Rd., Sec.1, Hsichih, New Taipei City, Taiwan 221
Tel: +886-2-2698-2888 Fax: +886-2-2698-2889
www.apacer.com

Features:

- **Compact Flash Association Specification Revision 3.0 Standard Interface**
  - ATA command set compatible
  - ATA mode support for up to:
    PIO Mode-6
    Multiword DMA Mode-4
    Ultra DMA Mode-4
- **Connector Type**
  - 50 pins female
- **Low power consumption (typical)**
  - Supply voltage: 3.3V & 5V
  - Active mode: 80 mA/95 mA (3.3V/5.0V)
  - Sleep mode: 700 µA/900 µA (3.3V/5.0V)
- **Performance****
  - Sustained read: 30 MB/sec
  - Sustained write:
    Standard: 5 MB/sec
    High Speed: 15 MB/sec
- **Capacity**
  - Standard:
    128, 256, 512 MB
    1, 2, 16 GB
  - High Speed:
    256, 512 MB
    1, 2, 4, 8 GB
- **NAND Flash Type: SLC**
- **Temperature ranges**
  - Operation:
    Standard: 0℃ to 70℃
    ET*: -40℃ to 85℃
  - Storage: -40℃ to 100℃
- **Flash management**
  - Intelligent endurance design
    Advanced wear-leveling algorithms
    S.M.A.R.T. Technology
    Built-in Hardware ECC
    Enhanced Data Integrity
  - Intelligent power failure recovery
- **RoHS compliant**

***Extended Temperature**
****Performance varies with flash configurations**

Table of Contents

1. General Description

Apacer's Industrial Compact Flash Card (CFC) offers the most reliable and high performance storage which is compatible with CF Type I and Type II devise. Unlike the ordinary consumer Compact Flash cards, Apacer Industrial Compact Flash card provides solid traceability to ensure all products HW/SW are the same as you qualified.

Apacer's CFC provides complete PCMCIA - ATA functionality and compatibility. Apacer 's Compact Flash technology is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

Featuring technologies as Advanced Wear-leveling algorithms, S.M.A.R.T, Enhanced Data Integrity, Built-in Hardware ECC, and Intelligent Power Failure Recovery, Apacer's Industrial Compact Flash Card assures users of a versatile device on data storage.

1.1 Performance-Optimized Controller

The Compact Flash Card Controller translates standard CF signals into flash media data and control signals.

1.1.1 Power Management Unit (PMU)

The power management unit (PMU) controls the power consumption of the Compact Flash card controller. It reduces the power consumption of the Compact Flash Card Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

1.1.2 SRAM Buffer

The Compact Flash Card Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

2. Functional Block

The Compact Flash Card (CFC) includes a controller and flash media, as well as the Compact Flash standard interface. Figure 2-1 shows the functional block diagram.

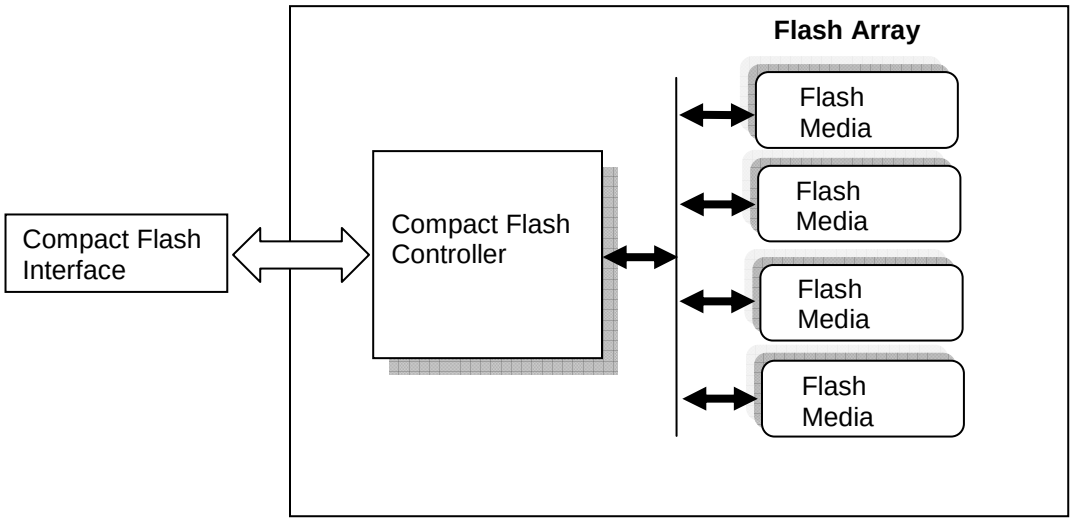


Figure 2-1: Functional block diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A "#" suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin assignments (1 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10[1]	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9[1]	I
11	A8	I	A8	I	A8[1]	I
12	A7	I	A7	I	A7[1]	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6[1]	I
15	A5	I	A5	I	A5[1]	I
16	A4	I	A4	I	A4[1]	I
17	A3	I	A3	I	A3[1]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I

Table 3-1: Pin assignments (2 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ[2]	O
44	#REG	I	#REG	I	DMACK[2]	I
45	BVD2	O	#SPKR	O	#DASP	O
46	BVD1	O	#STSCHG	O	#PDIAG	O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

4. Capacity Specification

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
128 MB	128,450,560	980	8	32	250,880
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1GB	1,024,966,656	1,986	16	63	2,001,888
2GB	2,048,901,120	3,970	16	63	4,001,760
4GB	4,110,188,544	7,964	16	63	8,027,712
8GB	8,195,604,480	15,880	16	63	16,007,040
16GB	16,391,208,960	16,383**	16	63	32,014,080

*Display of total bytes varies from file systems.
**Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

4.1 Performance Specification

Performances of the Standard and High Speed ATA-Flash Disk are listed in Table 4-2 and Table 4-3.

Table 4-2: Standard Performance specifications

Capacity / Performance	128 MB / 256 MB 512 MB / 1 GB	2 GB	16 GB
Sustained read (MB/s)	15	20	20
Sustained write (MB/s)	5	5	5

Table 4-3: High Speed Performance specifications

Capacity / Performance	256 MB	512 MB	1 GB	2 GB	4 GB	8 GB
Sustained read (MB/s)	25	25	25	25	30	30
Sustained write (MB/s)	5	5	5	5	10	15

Note: Performance varies from flash configurations.

4.2 Environmental Specifications

Environmental specification of the Compact Flash Card series (CFC) which follows the MIL-STD-810F standards is available as shown in Table 4-4.

Table 4-4: Environmental specifications

Environment		Specification
Temperature	Operation	0℃ to 70℃ (Standard) ; -40℃ to 85℃ (Extended Temperature)
	Storage	-40℃ to 100℃
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operation)		Sine wave: 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)

5. Flash Management

5.1 Intelligent Endurance Design

5.1.1 Advanced wear-leveling algorithms

The NAND flash devices are limited by a certain number of write cycles. When using a file system, frequent file table updates is mandatory. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole device, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. The scheme is achieved both via buffer management and Apacer-specific advanced wear leveling to ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

5.1.2 S.M.A.R.T. technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

5.1.3 Built-in hardware ECC

The ATA-Disk Module uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data. High performance is fulfilled through hardware-based error detection and correction.

5.1.4 Enhanced data integrity

The properties of NAND flash memory make it ideal for applications that require high integrity while operating in challenging environments. The integrity of data to NAND flash memory is generally maintained through ECC algorithms and bad block management. Flash controllers can support up to 8 bits ECC capability for accuracy of data transactions, and bad block management is a preventive mechanism from loss of data by retiring unusable media blocks and relocating the data to the other blocks, along with the integration of advanced wear leveling algorithms, so that the lifespan of device can be expanded.

5.2 Intelligent Power Failure Recovery

The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected blackout. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

6. Software Interface

6.1 Command Set

Table 6-1 summarizes the command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1: Command set (1 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
Flush-Cache	E7H	-	-	-	-	D	-
Format Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Request-Sense	03H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y[7]	-	-	-	D	-

Table 6-1: Command set (2 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
SMART	B0H	Y	Y	Y	Y	D	
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Translate-Sector	87H	-	Y	Y	Y	Y	Y
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDH	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector-Without-Erase	38H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command
8. For the Drive/Head register:
Y means both the CFC and Head parameters are used
D means only the CFC parameter is valid and not the Head parameter

7. Electrical Specification

Caution: **Absolute Maximum Stress Ratings –** Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

Range	Ambient Temperature	3.3V	5V
Standard	0℃ to +70℃	3.135-3.465V	4.75-5.25V
Extended Temperature	-40℃ to +85℃		

Table 7-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to VDD + 0.5V max.

Table 7-3: Recommended system power-up timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-READY}$[1]	Power-up to Ready Operation	200	1000	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	200	1000	ms

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

7.1 DC Characteristics

Table 7-4: DC Characteristics

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1} V_{IL1}	I1	Input Voltage	2.0V	0.8V	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	μA	V_{IN}=GND to V_{DDQ} V_{DDQ}= V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-110	-1	μA	V_{OUT}=GND, V_{DDQ}= V_{DDQ} Max
V_{T+2} V_{T-2}	I2	Input Voltage Schmitt Trigger	0.8	2.0	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	μA	V_{IN}=GND to V_{DDQ} V_{DDQ}= V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-110	-1	μA	V_{OUT}=GND, V_{DDQ}= V_{DDQ} Max
V_{OH1} V_{OL1}	O1	Output Voltage	2.4	0.4	V	I_{OH1}=I_{OH1} Min I_{OL1}=I_{OL1} Max
I_{OH1}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL1}		Output Current		4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH2} V_{OL2}	O2	Output Voltage	2.4	0.4	V	I_{OH2}=I_{OH2} Min I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-6		mA	V_{DDQ}=3.135V-3.465V
I_{OL2}		Output Current		6	mA	V_{DDQ}=3.135V-3.465V
I_{OH2}		Output Current	-8		mA	V_{DDQ}=4.5V-5.5V
I_{OL2}		Output Current		8	mA	V_{DDQ}=4.5V-5.5V
V_{OH6} V_{OL6}	O6	Output Voltage for DASP# pin	2.4	0.4	V	I_{OH6}=I_{OH6} Min I_{OL6}=I_{OL6} Max
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=3.135V-3.465V
I_{OL6}		Output Current for DASP# pin		8	mA	V_{DDQ}=3.135V-3.465V
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=4.5V-5.5V
I_{OL6}		Output Current for DASP# pin		12	mA	V_{DDQ}=4.5V-5.5V
$I_{DD}^{1,2}$	PWR	Power supply current (T_a = 0℃ to +70℃)		50	mA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max
$I_{DD}^{1,2}$	PWR	Power supply current (T_a= -40℃ to +85℃)		75	mA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_a = 0℃ to +70℃)		75	μA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_a = -40℃ to +85℃)		200	μA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max

7.2 AC Characteristics

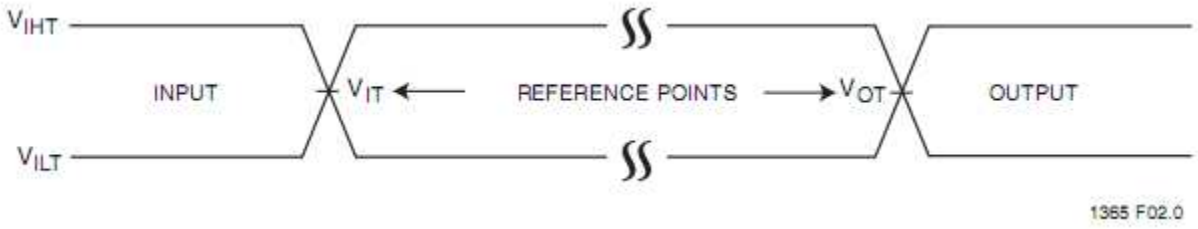


Figure 7-1: AC Input/Output Reference Waveforms

AC test inputs are driven at VIHT (0.9 VDD) for a logic “1” and VILT (0.1 VDD) for a logic “0”. Measurement reference points for inputs and outputs are VIT (0.5 VDD) and VOT (0.5 VDD). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - $V_{INPUT\ HIGH}$ Test
V_{ILT}- $V_{INPUT\ LOW}$ Test

7.2.1 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-5: Attribute Memory Read Timing Specification

Speed Version			100 ns		
Item	**Symbol**	**IEEE Symbol**	**Min***	**Max***	**Units**
Read Cycle Time	$T_{C(R)}$	tAVAV	100		ns
Address Access Time	$T_{A(A)}$	tAVQV		100	ns
Card Enable Access Time	$T_{A(CE)}$	tELQV		100	ns
Output Enable Access Time	$T_{A(OE)}$	tGLQV		50	ns
Output Disable Time from CE#	$T_{DIS(CE)}$	tEHQZ		50	ns
Output Disable Time from OE#	$T_{DIS(OE)}$	tGHQZ		50	ns
Address Setup Time	$T_{SU(A)}$	tAVGL	10		ns
Output Enable Time from CE#	$T_{EN(CE)}$	tELQNZ	5		ns
Output Enable Time from OE#	$T_{EN(OE)}$	tGLQNZ	5		ns
Data Valid from Address Change	$T_{V(A)}$	tAXQZ	0		ns

*D_{OUT} signifies data provided by the Compact Flash card to the system. The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations. All AC specifications are guaranteed by design.

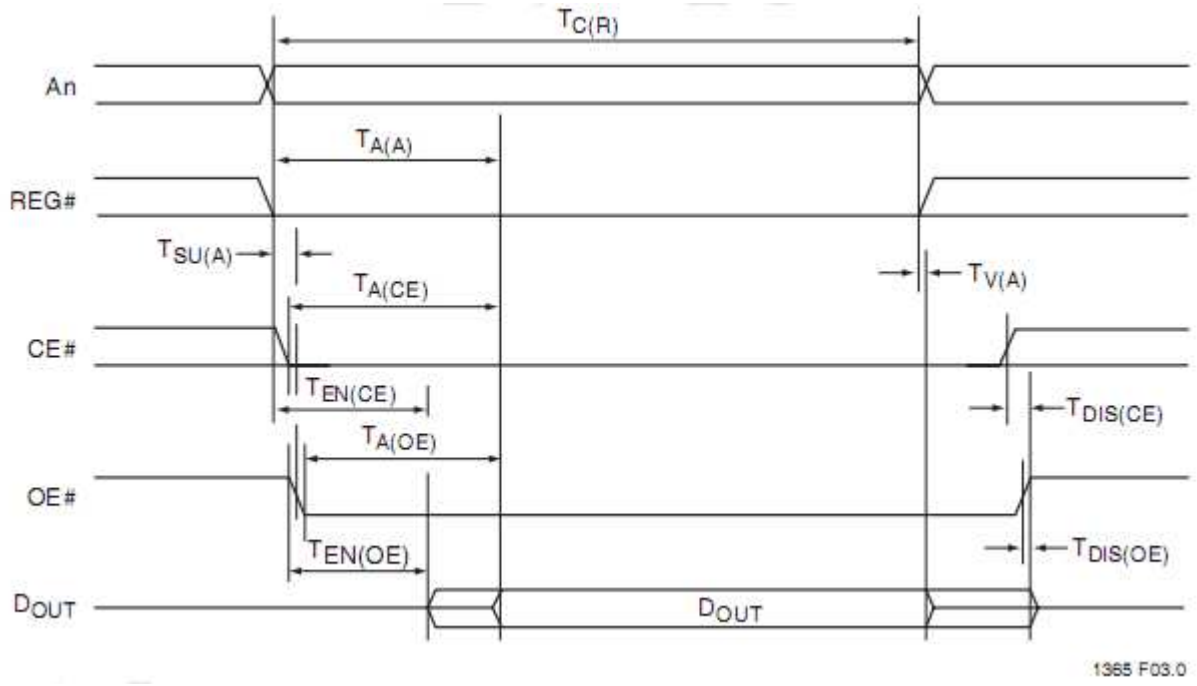


Figure 7-2: Attribute Memory Read Timing Diagram

7.2.2 Configuration Register (Attribute Memory) Write Specification

The card configuration write access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-6: Configuration Register (Attribute Memory) Write Timing

Speed Version			**100 ns**		
Item	**Symbol**	**IEEE Symbol**	**Min***	**Max***	**Units**
Write Cycle Time	$T_{C(W)}$	tAVAV	100		ns
Write Pulse Width	$T_{W(WE)}$	tWLWH	60		ns
Address Setup Time	$T_{SU(A)}$	tAVWL	10		ns
Write Recover Time	$T_{REC(WE)}$	tWMAX	15		ns
Data Setup Time for WE	$T_{SU(DWE\#H)}$	tDVWH	40		ns
Data Hold Time	$T_{H(D)}$	tWMDX	15		ns

*D_{IN} signifies data provided by the system to the Compact Flash card. All AC specifications are guaranteed by design.

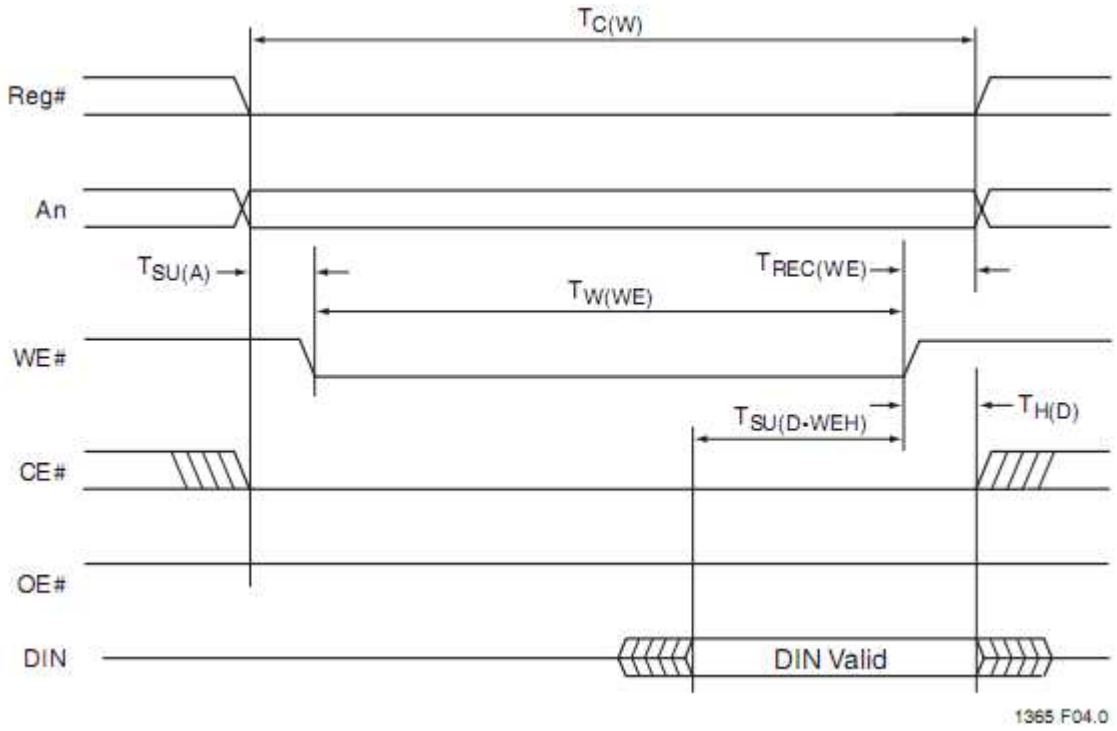


Figure 7-3: Configuration Register (Attribute Memory) Write Timing Diagram

7.2.3 Common Memory Read Timing Specification

Table 7-7: Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min*	Max*	Units
Output Enable Access Time	$T_{A(OE)}$	tGLQV		50	ns
Output Disable Time from OE	$T_{DIS(OE)}$	tGHQZ		50	ns
Address Setup Time	$T_{SU(A)}$	tAVGL	10		ns
Address Hold Time	$T_{REC(WE)}$	tGHAX	15		ns
CE Setup before OE	$T_{SU(CE)}$	tELGL	0		ns
CE Hold following OE	$T_{H(CE)}$	tGHEH	15		ns

*All AC specifications are guaranteed by design.

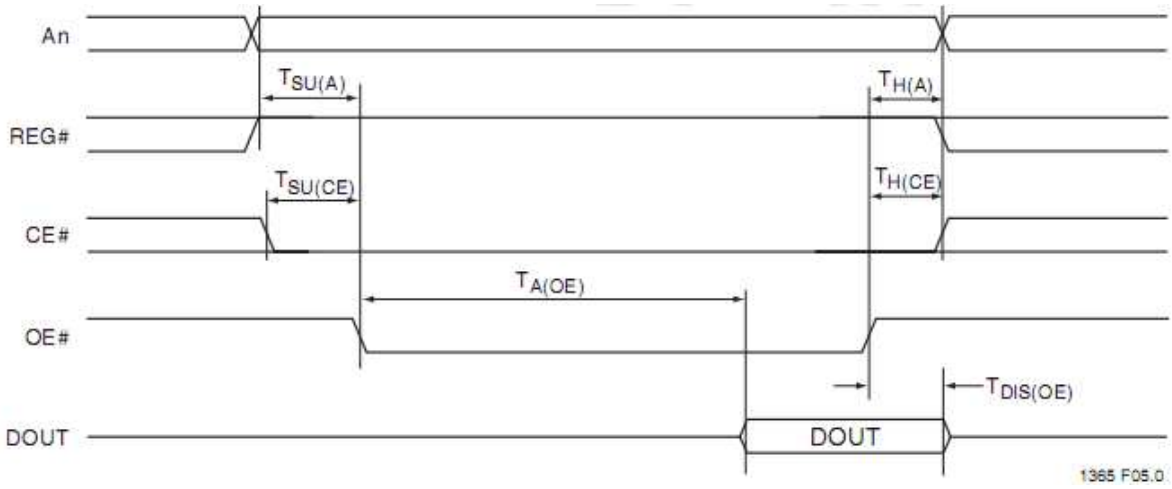


Figure 7-4: Common Memory Read Timing Diagram

7.2.4 Common Memory Write Timing Specification

Table 7-8: Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min*	Max*	Units
Data Setup before WE	$T_{SU(DWE\#H)}$	tDVWH	40		ns
Data Hold following WE	$T_{H(D)}$	tWMDX	15		ns
WE Pulse Width	$T_{W(WE)}$	tWLWH	60		ns
Address Setup Time	$T_{SU(A)}$	tAVWL	10		ns
CE Setup before WE	$T_{SU(CE)}$	tELWL	0		ns
Write Recovery Time	$T_{REC(WE)}$	tWMAX	15		ns
Address Hold Time	$T_{H(A)}$	tGHAX	15		ns
CE Hold following WE	$T_{H(CE)}$	tGHEH	15		ns

*All AC specifications are guaranteed by design.

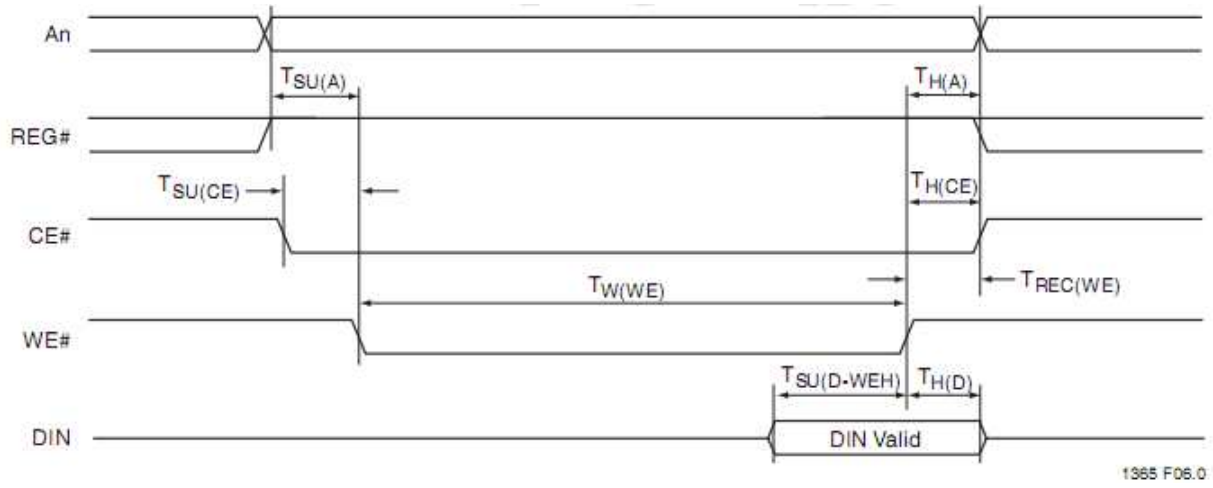


Figure 7-5: Common Memory Write Timing Diagram

7.2.5 I/O Input (Read) Timing Specification

Table 7-9: I/O Read Timing

Item	Symbol	IEEE Symbol	Min*	Max*	Units
Data Delay after IORD	$T_{D(IORD)}$	tIGLQV		100	ns
Data Hold following IORD	$T_{H(IORD)}$	tIGHQX	0		ns
IORD Width Time	$T_{W(IORD)}$	tIGLIGH	165		ns
Address Setup before IORD	$T_{SUA(IORD)}$	tAVIGL	70		ns
Address Hold following IORD	$T_{HA(IORD)}$	tIGHAX	20		ns
CE Setup before IORD	$T_{SUCE(IORD)}$	tELIGL	5		ns
CE Hold following IORD	$T_{HCE(IORD)}$	tIGHEH	20		ns
REG Setup before IORD	$T_{SUREG(IORD)}$	tRGLIGL	5		ns
REG Hold following IORD	$T_{HREG(IORD)}$	tIGHRGH	0		ns
INPACK Delay Falling from IORD	$T_{DFINPACK(IORD)}$	tIGLIAL	0	45	ns
INPACK Delay Rising from IORD	$T_{DRINPACK(IORD)}$	tIGHIAH		45	ns
IOIS16 Delay Falling from Address	$T_{DFIOIS16(ARD)}$	tAVISL		35	ns
IOIS16 Delay Rising from Address	$T_{DRIOIS16(ADR)}$	tAVISH		35	ns

*All AC specifications are guaranteed by design.
Note: The maximum load on –INPACK and IOIS16# is 1 LSTTL with 50pF total load.

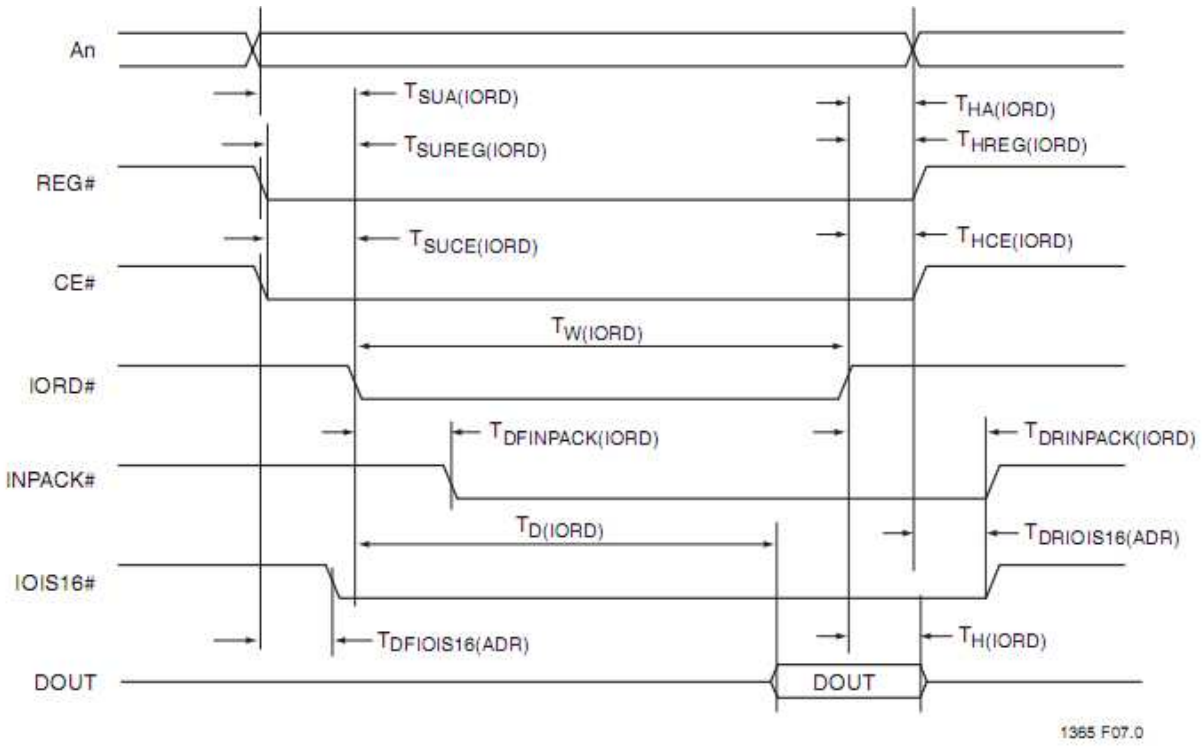


Figure 7-6: I/O Read Timing Diagram

7.2.6 I/O Output (Write) Timing Specification

Table 7-10: I/O Write Timing

Item	Symbol	IEEE Symbol	Min*	Max*	Units
Data Setup before IOWR	$T_{SU(IOWR)}$	tDVIWH	60		ns
Data Hold following IOWR	$T_{H(IOWR)}$	tIWHDX	30		ns
IOWR Width Time	$T_{W(IOWR)}$	tIWLIWH	165		ns
Address Setup before IOWR	$T_{SUA(IOWR)}$	tAVIWL	70		ns
Address Hold following IOWR	$T_{HA(IOWR)}$	tIWHAX	20		ns
CE Setup before IOWR	$T_{SUCE(IOWR)}$	tELIWL	5		ns
CE Hold following IOWR	$T_{HCE(IOWR)}$	tIWHEH	20		ns
REG Setup before IOWR	$T_{SUREG(IOWR)}$	tRGLIWL	5		ns
REG Hold following IOWR	$T_{HREG(IOWR)}$	tIWHRGH	0		ns
IOIS16 Delay Falling from Address	$T_{DFIOIS16(ARD)}$	tAVISL		35	ns
IOIS16 Delay Rising from Address	$T_{DRIOIS16(ADR)}$	tAVISH		35	ns

*All AC specifications are guaranteed by design.
Note: The maximum load on –INPACK and IOIS16# is 1 LSTTL with 50pF total load.

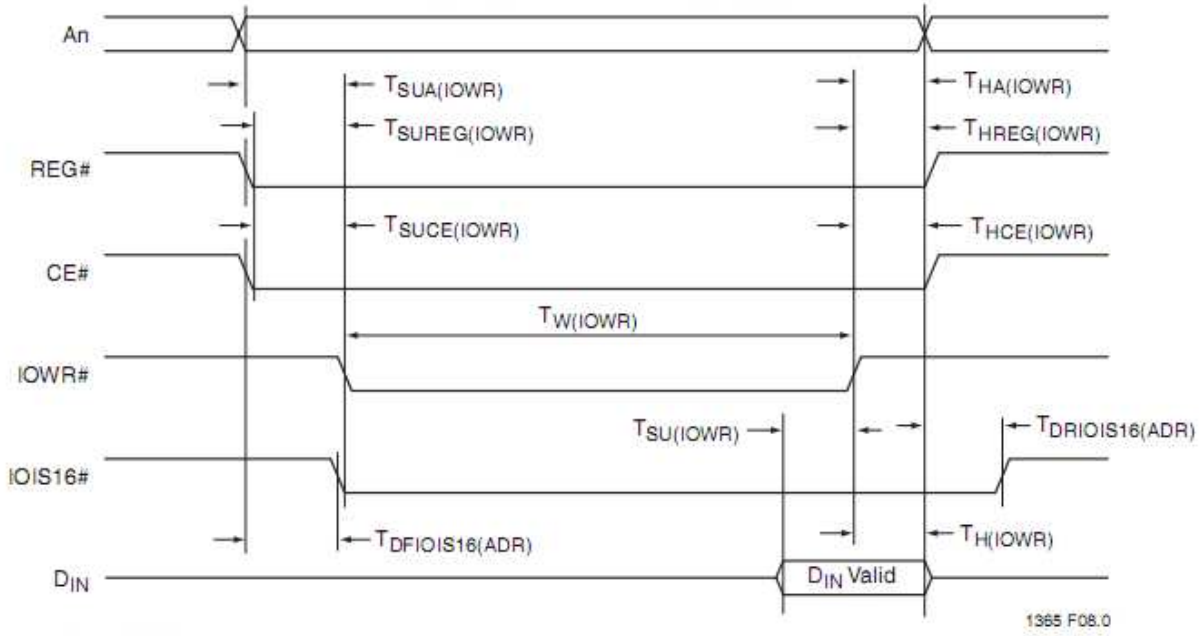


Figure 7-7: I/O Write Timing Diagram

7.2.7 Ultra DMA Mode Data Transfer Input/Output (Read/Write) Timing

Table 7-11: Ultra DMA Data Burst Timing Specifications[1]

Name	Descriptions	Mode 4		Unit	Measurement Location[2]
		Min	Max		
$T_{2CYCTYP}$	Typical sustained average two cycle time	60		ns	Sender
T_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	25		ns	Note[3]
T_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	57		ns	Sender
T_{DS}	Data setup time at recipient (from data valid until STROBE edge)[4,5]	5.0		ns	Recipient
T_{DH}	Data hold time at Recipient (from STROBE edge until data becomes invalid)[1,2]	5.0		ns	Recipient
T_{DVS}	Data valid setup time for Sender (from data valid until STROBE edge)[6]	6.0		ns	Sender
T_{DVH}	Data valid hold time at Sender (from STROBE edge until data becomes invalid)[3]	6.0		ns	Sender
T_{CS}	CRC word setup time at device[1]	5.0		ns	Device
T_{CH}	CRC word hold time at device[1]	5.0		ns	Device
T_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK negation)[3]	6.7		ns	Host
T_{CVH}	CRC word valid hold time at Sender (from DMACK negation until CRC becomes invalid)[3]	6.2		ns	Host
T_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	0		ns	Device
T_{DZFS}	Time from data output released-to-driving until the first transition of critical timing	6.7		ns	Sender
T_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)		120	ns	Device
T_{LI}	Limited interlock time[7]	0	100	ns	Note[8]
T_{MLI}	Interlock time with minimum[4]	20		ns	Host
T_{UI}	Unlimited interlock time[4]	0		ns	Host
T_{AZ}	Maximum time allowed for output drivers to release (from asserted to negated)		10	ns	Note[9]
T_{ZAH}	Minimum delay time required for output	20		ns	Host
T_{ZAD}	Drivers to assert or negate (from released)	0		ns	Device
T_{ENV}	Envelope time (from DMACK# to STOP and HDMARDY# during data in burst initiation and from DMACK to STOP during data our burst initiation)	20	55	ns	Host
T_{RFS}	Ready-to-final STROBE time (no STROBE edge are sent this long after negation of DMARDY)		60	ns	Sender
T_{RP}	Ready-to-pause time (Recipient waits to pause until after negating DMARDY)	100		ns	Recipient
T_{IORDYZ}	Maximum time before releasing IORDY		20	ns	Device
T_{ZIORDY}	Minimum time before driving IORDY[10]	0		ns	Device
T_{ACK}		20		ns	Host
T_{SS}		50		ns	Sender

1. All timing measurement switching points (low-to-high and high-to-low) are taken at 1.5V.
2. All signal transitions for a timing parameter are measured at the connector specified in the measurement location column. For example, in the case of TRFS, both STROBE and DMARDY Transitions are measured at the Sender connector.
3. The parameter TCYC is measured at the recipient's connector farthest from the Sender.
4. 80-Conductor cabling is required in order to meet sup (TDS, TCS) and hold (TDH, TCH) times in modes greater than two.
5. The parameters TDS and TDH for Mode 5 are defined for a Recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for TDS and TDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.
6. Timing for TDVS, TDVH, TCVS, and TCVH are met for lumped capacitive loads of 15 and 50 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
7. The parameters TUI, TMLI, and TLI indicate Sender-to-Recipient or Recipient-to-Sender interlocks. For example, one agent (either Sender or Recipient) is waiting for the other agent to respond with a signal before proceeding; TUI is an unlimited interlock that has no maximum time value, TMLI is a limited time-out that has a defined minimum, and TLI is a limited time-out that has a defined maximum.
8. The parameter TLI is measured at the connector of the Sender or Recipient that is responding to an incoming transition from the Recipient or Sender respectively. Both the incoming signal and the outgoing response are measured at the same connector.
9. The parameter TAZ is measured at the connector of the Sender or Recipient that is driving the bus but must release the bus that allow for a bus turnaround.
10. For all modes the parameter TZIORDY may be greater than TENV because the host has a pull-on IORDY giving it a known state when released.

Table 7-12: Ultra DMA Sender and Recipient IC Timing Specifications[1]

Name	Descriptions	Mode 4		Unit
		Min	Max	
T_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge)[2]	4.8		ns
T_{DHIC}	Recipient IC data hold time (from STROBE edge until data becomes invalid)[1]	4.8		ns
T_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge)[3]	9.5		ns
T_{DVHIC}		9.0		ns

1. All timing measurement switching point (low-to-high and high-to-low)
2. The correct data value is captured by the Recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at TDSIC and TDHIC timing (as measured through 1.5 V).
3. The parameters TDVSIC and TDVHIC are met for lumped capacitive loads of 15 and 40 pf at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

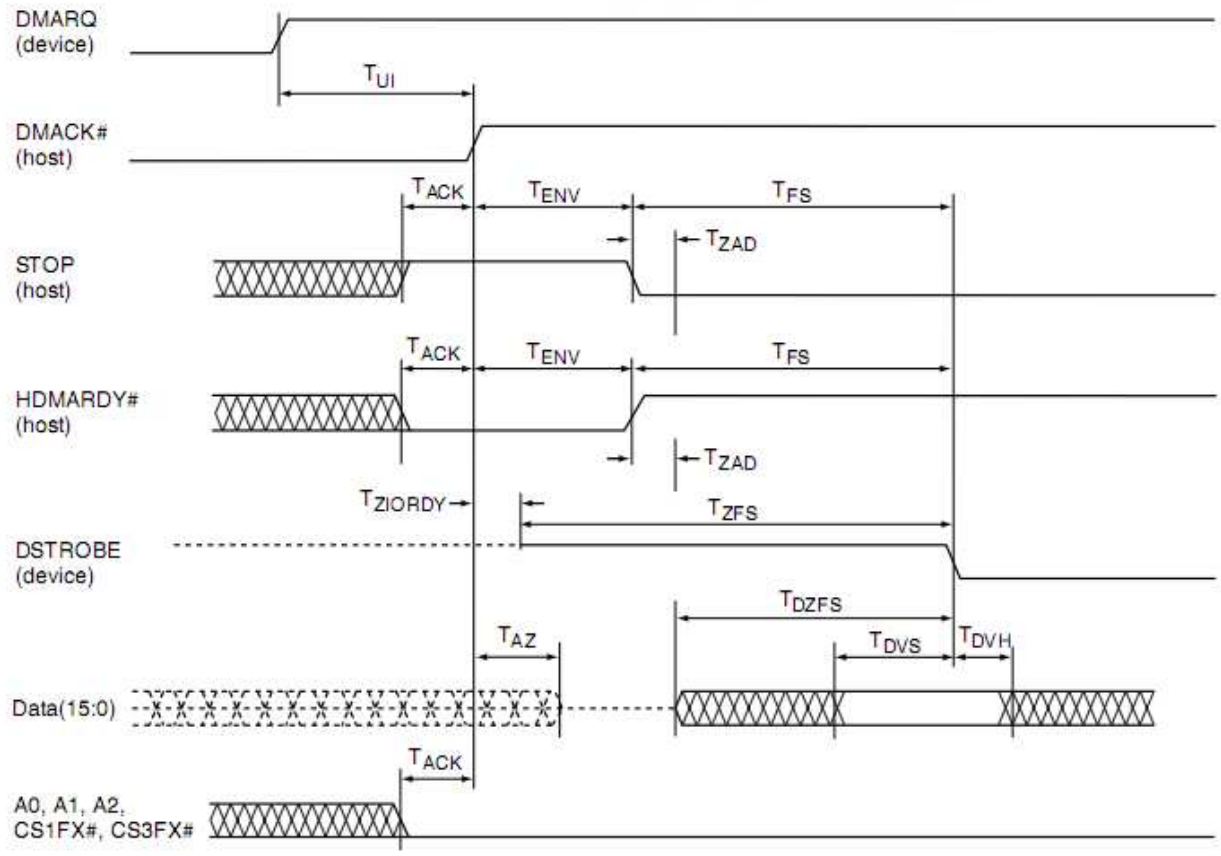


Figure 7-8: Initiating an Ultra DMA Data-In Burst

Notes:
1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDRARDY-: DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

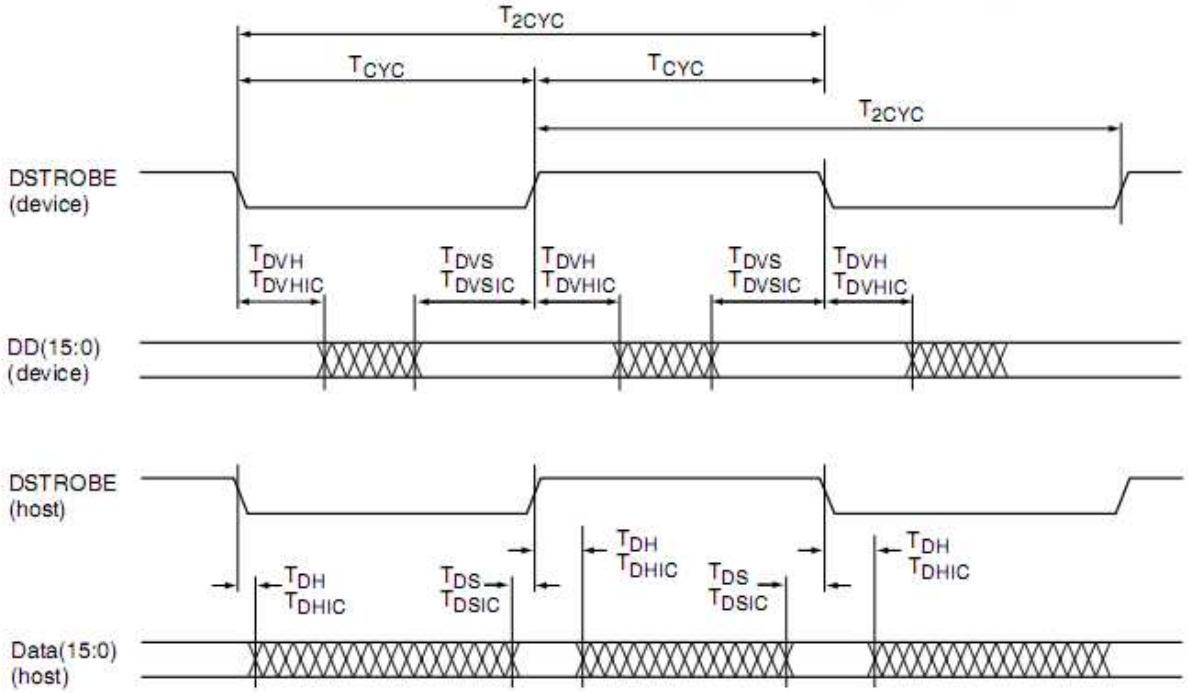


Figure 7-9: Sustained Ultra DMA Data-In Burst

Notes:

1. DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the device.

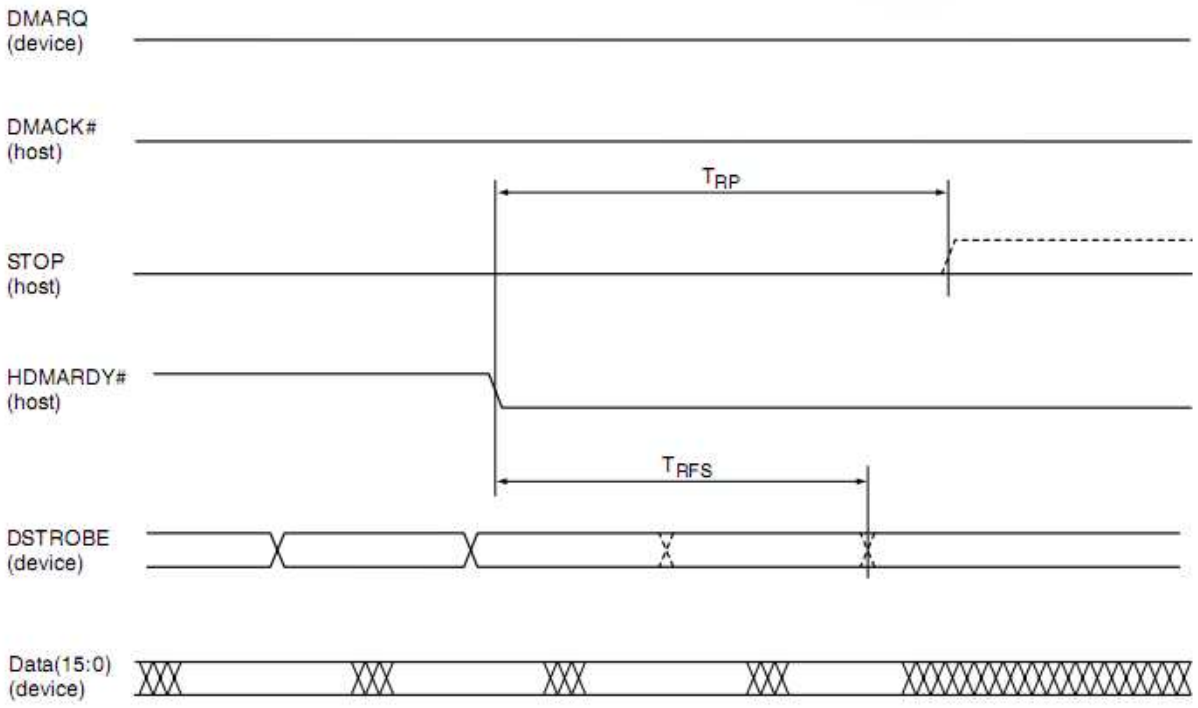


Figure 7-10: Sustained Ultra DMA Data-In Burst

Notes:
1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than TRP after HDMARDY# is negated.
2. After negating HDMARDY#, the host may receive zero, one, two, or three more data words from the device.

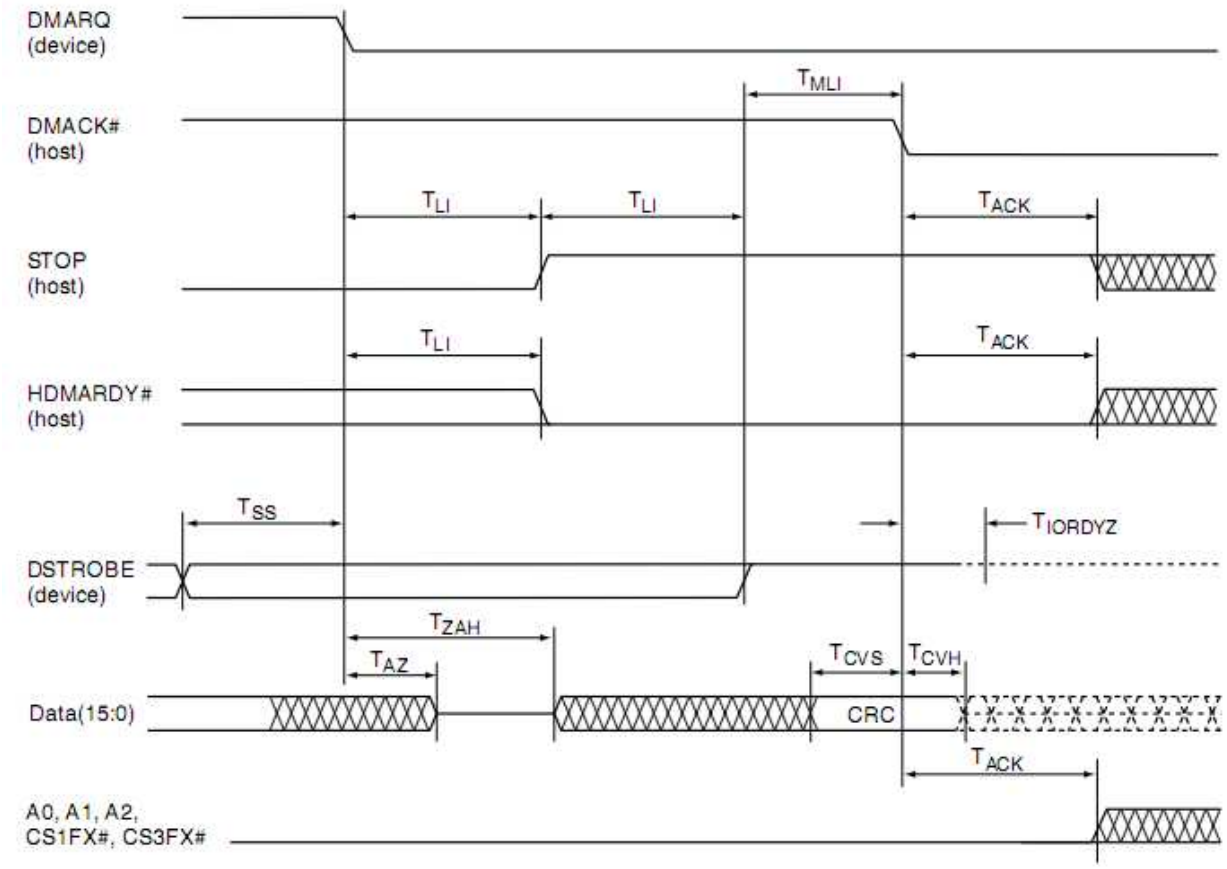


Figure 7-11: Device Terminating and Ultra DMA Data-In Burst

Notes:
1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

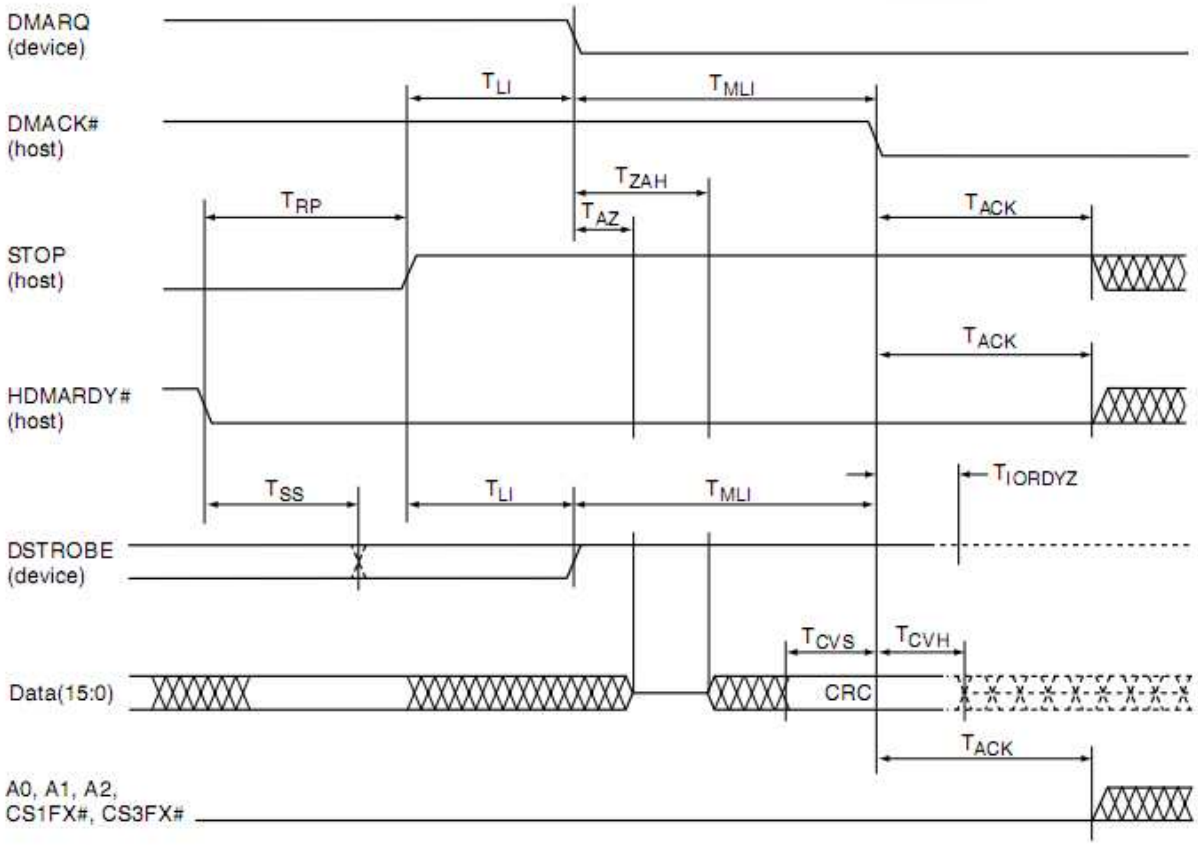


Figure 7-12: Host Terminating and Ultra DMA Data-In Burst

Notes:
1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

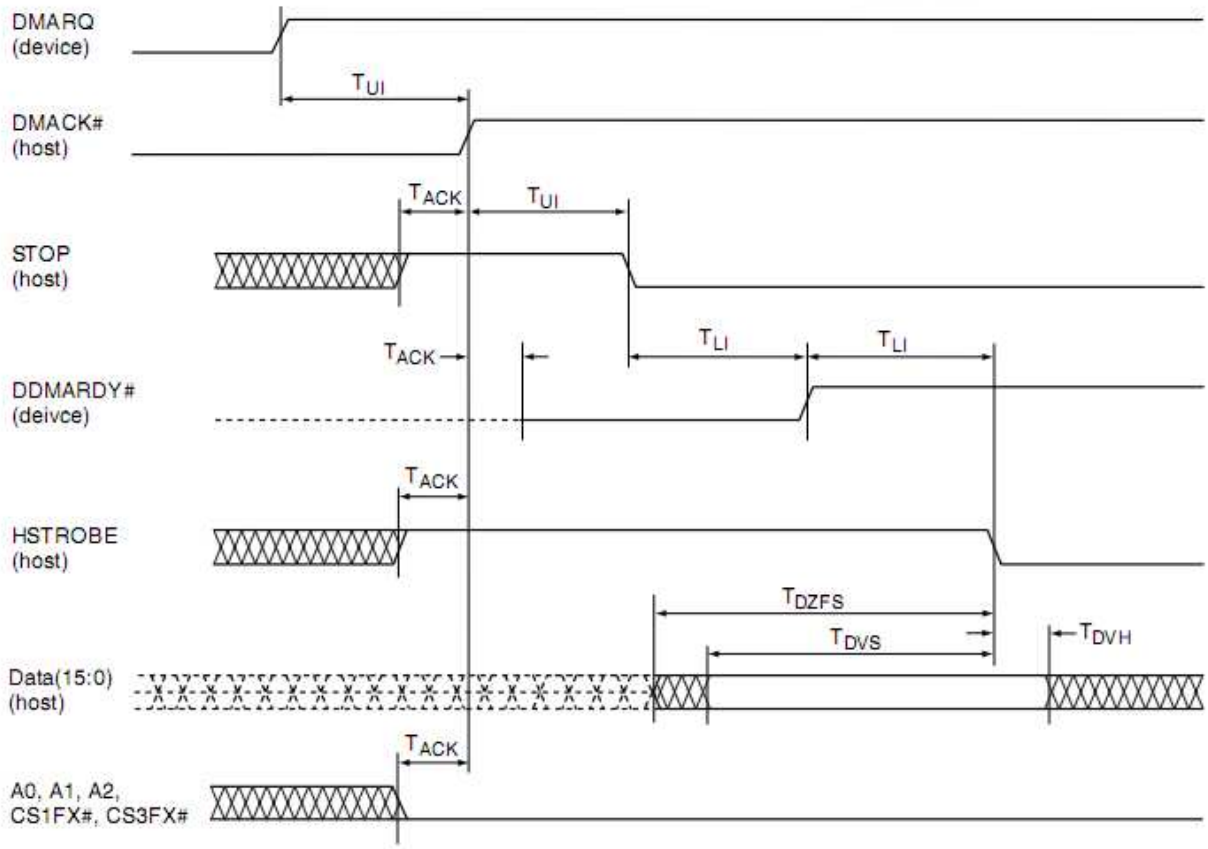


Figure 7-13: Initiating an Ultra DMA Data-Out Burst

Notes:
1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

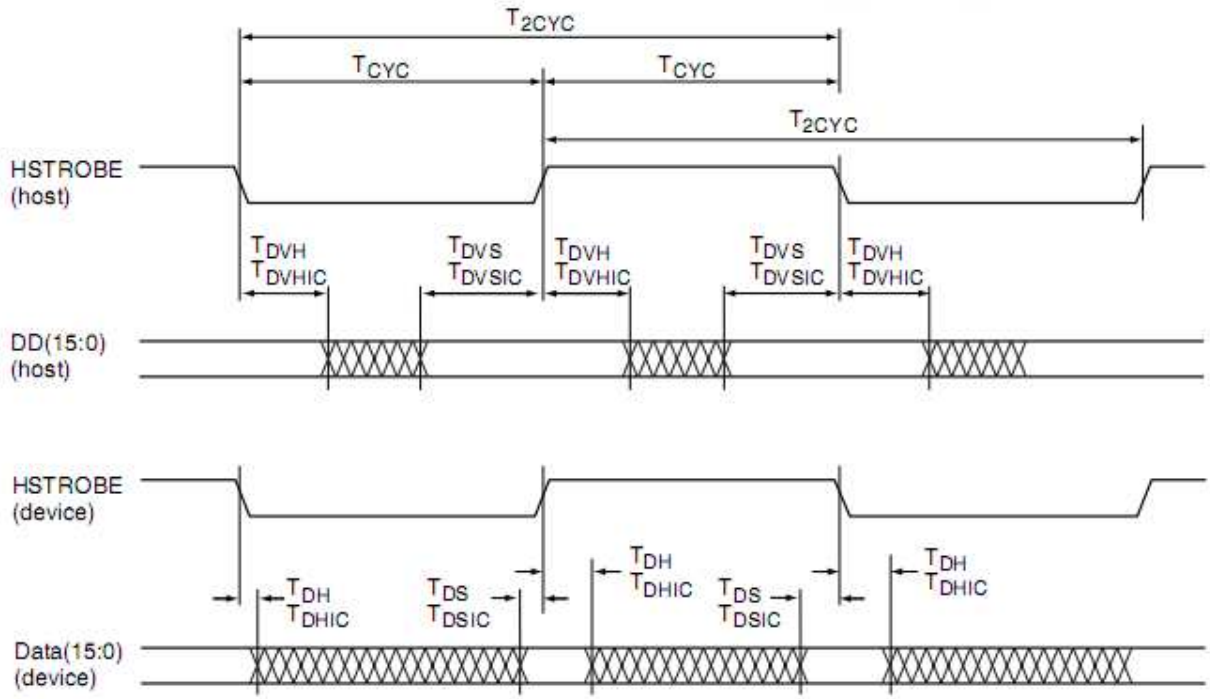


Figure 7-14: Sustained Ultra DMA Data-Out Burst

Notes:

1. DD(15:0) and HSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the host.

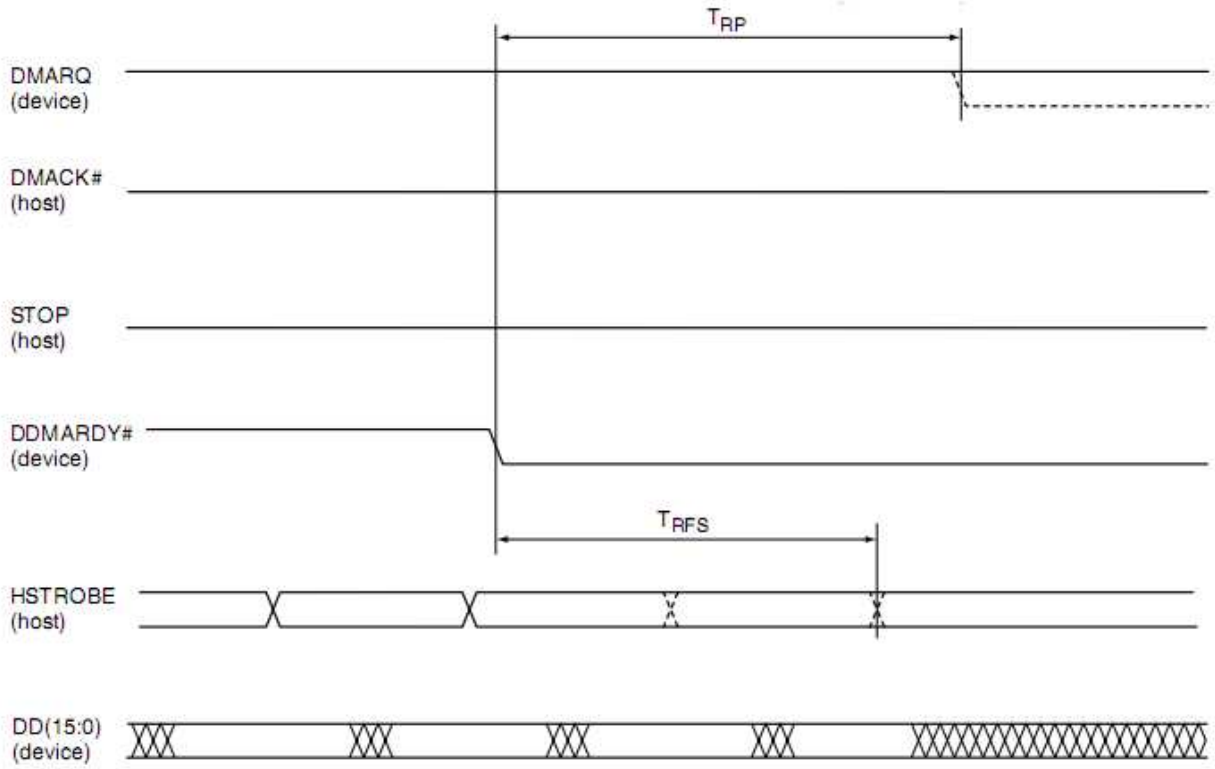


Figure 7-15: Device Pausing and Ultra DMA Data-Out Burst

Notes:
1. The host may negate DMARQ to request termination of the Ultra DMA burst no sooner than TRP after DDMARDY# is negated.
2. After negating DDMARDY#, the host may receive zero, one, two, or three more data words from the host.

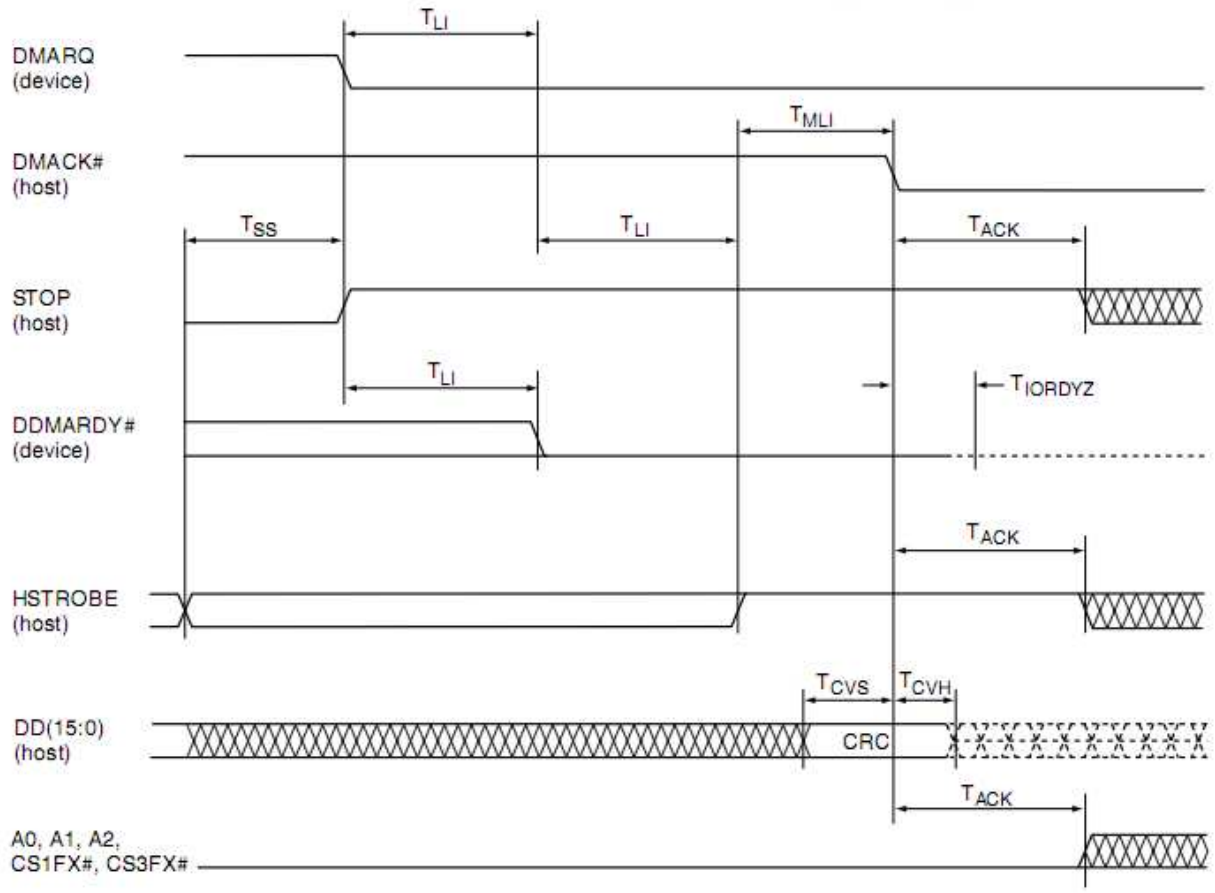


Figure 7-16: Host Terminating and Ultra DMA Data-Out Burst

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

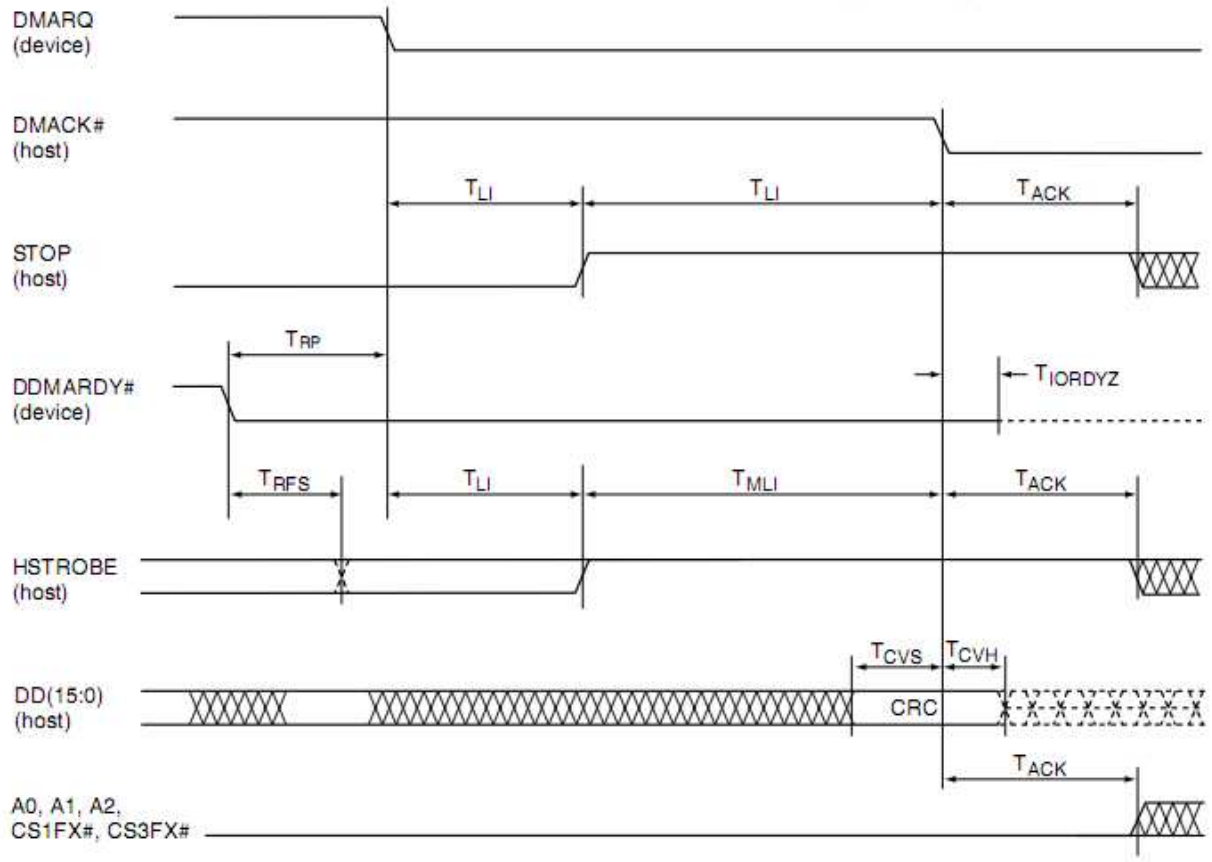


Figure 7-17: Device Terminating and Ultra DMA Data-Out Burst

Notes:
1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

7.2.8 Media Side Interface I/O Timing Specifications

Table 7-13: Timing Parameter

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	20	-	ns
T_{CLH}	FCLE Hold Time	40	-	ns
T_{CS}	FCE# Setup Time	40	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	40	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{WP}	FWE# Pulse Width	20	-	ns
T_{WH}	FWE# High Hold Time	20	-	ns
T_{WC}	Write Cycle Time	40	-	ns
T_{ALS}	FALE Setup Time	20	-	ns
T_{ALH}	FALE Hold Time	40	-	ns
T_{DS}	FAD[15:0] Setup Time	20	-	ns
T_{DH}	FAD[15:0] Hold Time	20	-	ns
T_{RP}	FRE# Pulse Width	20	-	ns
T_{RR}	Ready to FRE# Low	40	-	ns
T_{RES}	FRE# Data Setup Access Time	20	-	ns
T_{RC}	Read Cycle Time	40	-	ns
T_{REH}	FRE# High Hold Time	20	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	5	-	ns

Note: All AC specifications are guaranteed by design.

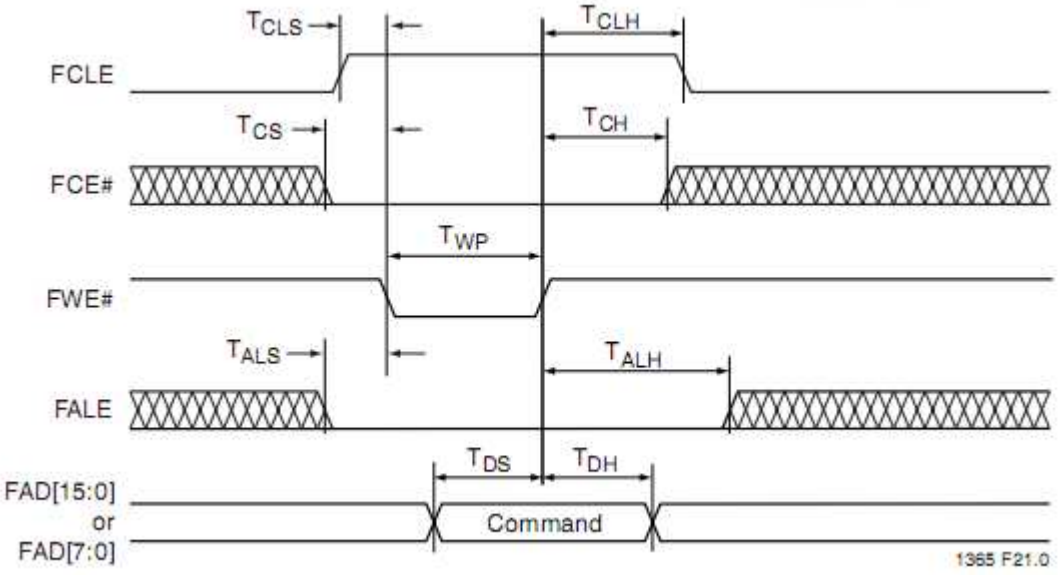


Figure 7-18: Media Command Latch Cycle

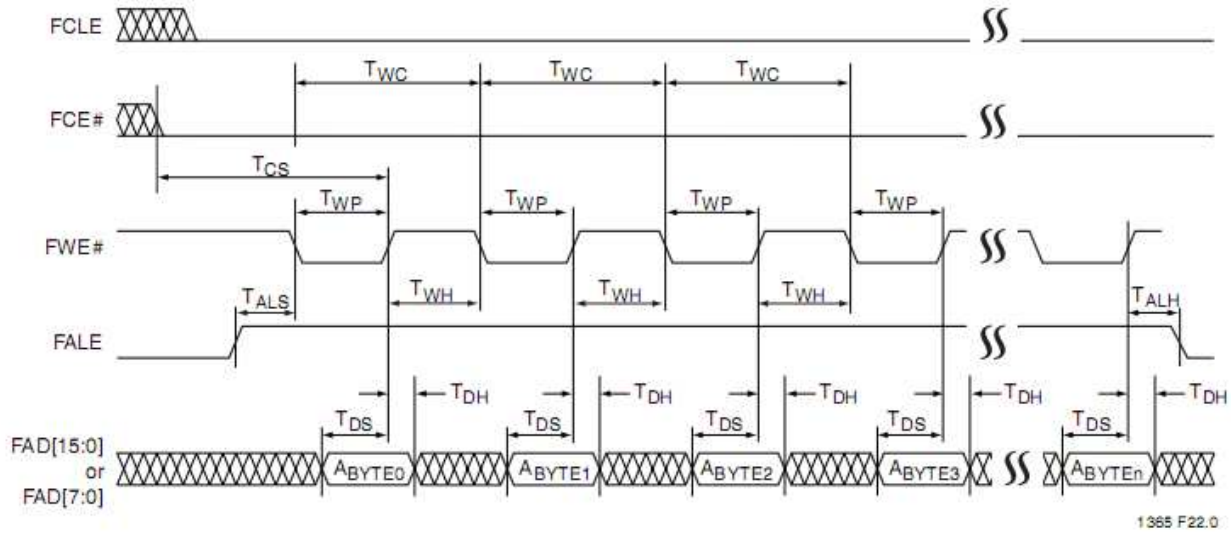


Figure 7-19: Media Access Latch Cycle

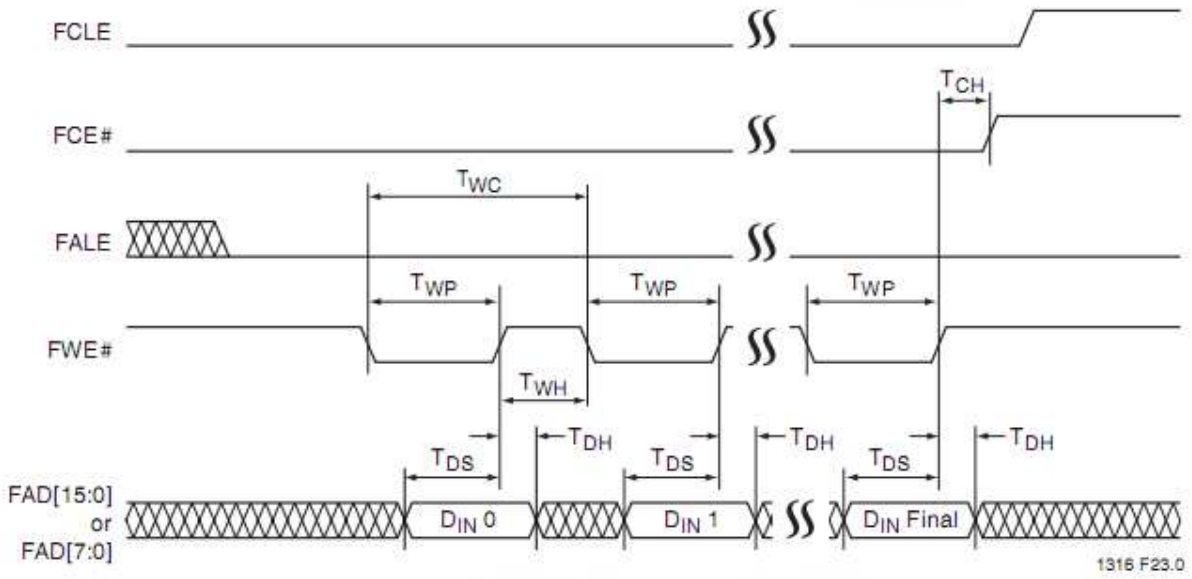


Figure 7-20: Media Data Loading Latch Cycle

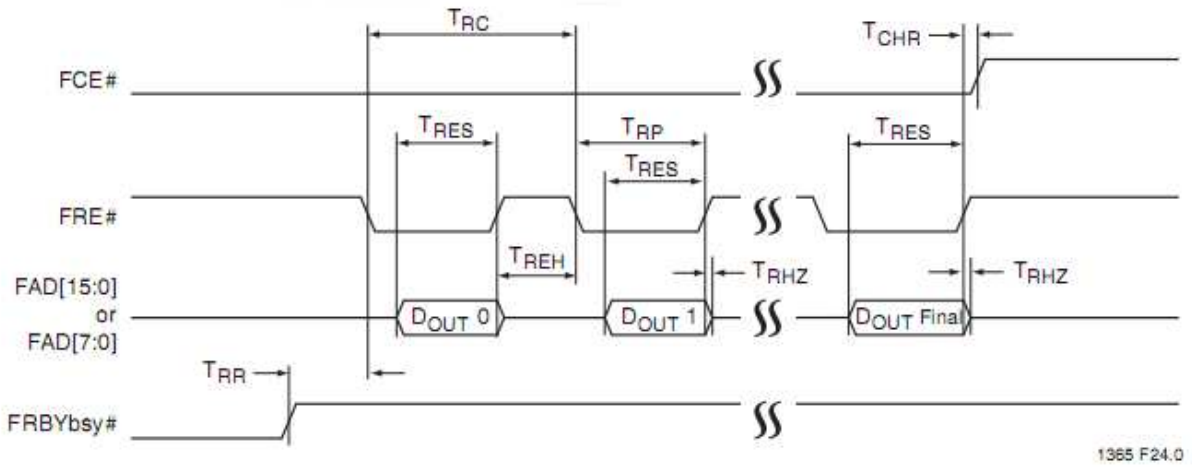


Figure 7-21: Media Data Read Cycle

8. Physical Characteristics

8.1 Dimension

TABLE 8-1: Type I CFC physical specification

Length:	36.40 +/- 0.15mm (1.433+/- 0.06 in.)
Width:	42.80 +/- 0.10mm (1.685+/- 0.04 in.)
Thickness (Including Label Area):	3.3mm+/-0.10mm (0.130+/-0.04in.)

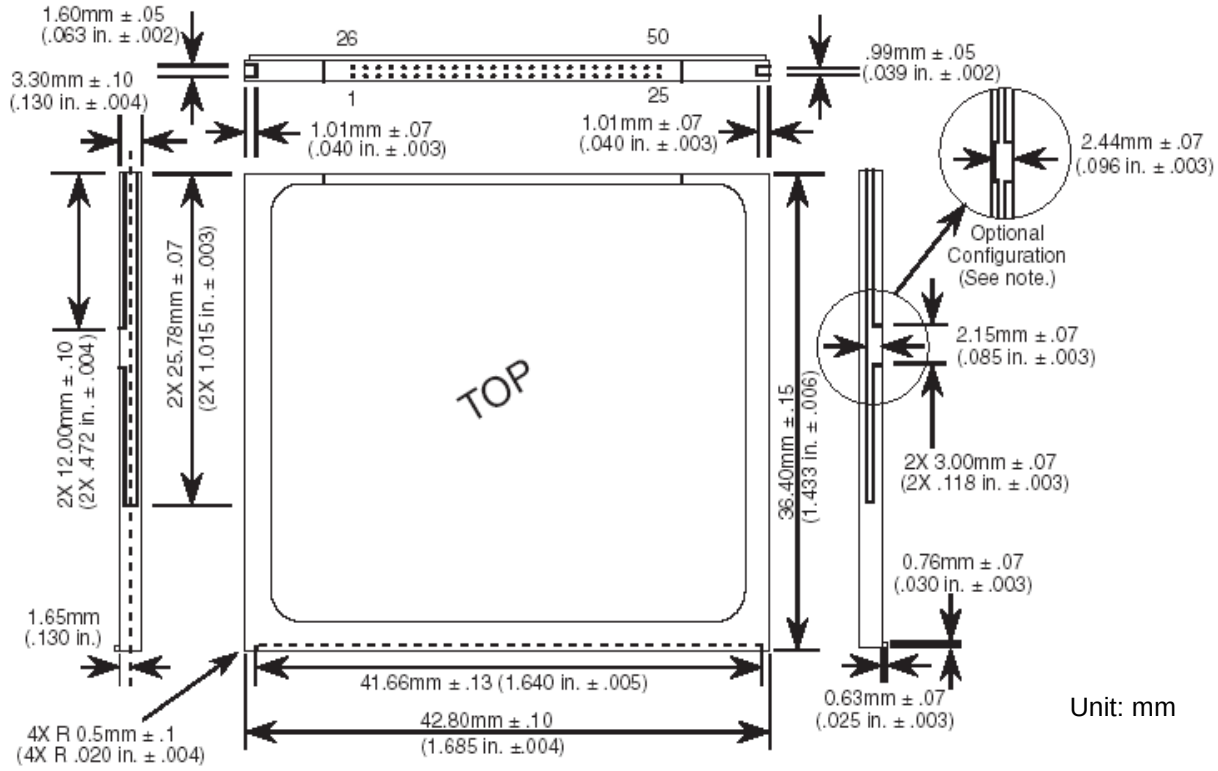
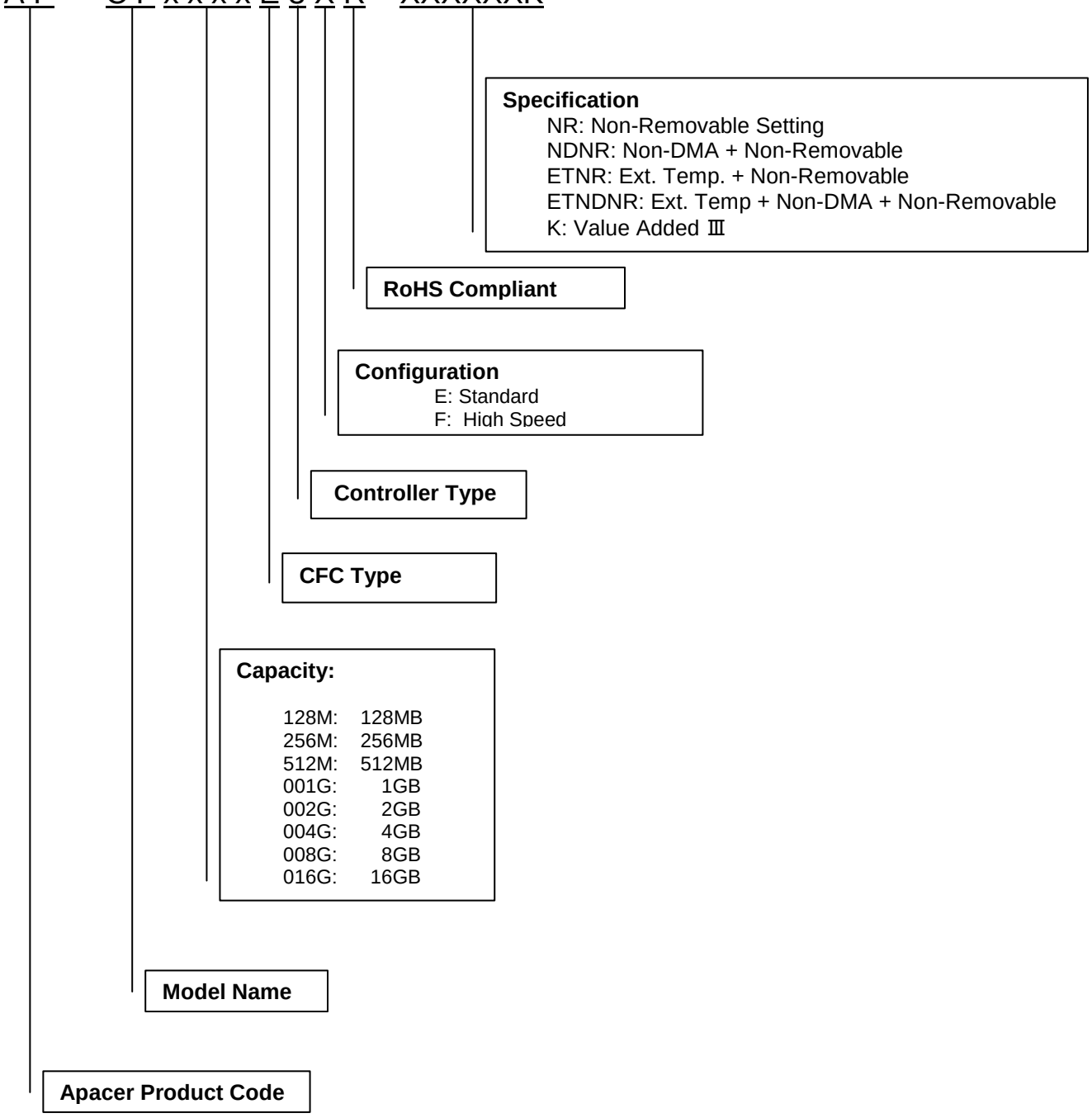


FIGURE 8-1: Physical dimension

9. Product Ordering Information

9.1 Product Code Designations

A P – C F x x x x E 3 X R – XXXXXXK



9.2 Valid Combinations

Standard Temperature

Non-Removable

Standard **High Speed**

Capacity	Model Number	Capacity	Model Number
128MB	AP-CF128ME3ER-NRK	256MB	AP-CF256ME3FR-NRK
256MB	AP-CF256ME3ER-NRK	512MB	AP-CF512ME3FR-NRK
512MB	AP-CF512ME3ER-NRK	1GB	AP-CF001GE3FR-NRK
1GB	AP-CF001GE3ER-NRK	2GB	AP-CF002GE3FR-NRK
2GB	AP-CF002GE3ER-NRK	4GB	AP-CF004GE3FR-NRK
16GB	AP-CF016GE3ER-NRK	8GB	AP-CF008GE3FR-NRK

Non-DMA & Non-Removable

Standard **High Speed**

Capacity	Model Number	Capacity	Model Number
128MB	AP-CF128ME3ER-NDNRK	256MB	AP-CF256ME3FR-NDNRK
256MB	AP-CF256ME3ER-NDNRK	512MB	AP-CF512ME3FR-NDNRK
512MB	AP-CF512ME3ER-NDNRK	1GB	AP-CF001GE3FR-NDNRK
1GB	AP-CF001GE3ER-NDNRK	2GB	AP-CF002GE3FR-NDNRK
2GB	AP-CF002GE3ER-NDNRK	4GB	AP-CF004GE3FR-NDNRK
16GB	AP-CF016GE3ER-NDNRK	8GB	AP-CF008GE3FR-NDNRK

Extended Temperature

Non-Removable

Standard

Capacity	Model Number
128MB	AP-CF128ME3ER-ETNRK
256MB	AP-CF256ME3ER-ETNRK
512MB	AP-CF512ME3ER-ETNRK
1GB	AP-CF001GE3ER-ETNRK
2GB	AP-CF002GE3ER-ETNRK
16GB	AP-CF016GE3ER-ETNRK

High Speed

Capacity	Model Number
256MB	AP-CF256ME3FR-ETNRK
512MB	AP-CF512ME3FR-ETNRK
1GB	AP-CF001GE3FR-ETNRK
2GB	AP-CF002GE3FR-ETNRK
4GB	AP-CF004GE3FR-ETNRK
8GB	AP-CF008GE3FR-ETNRK

Non-DMA & Non-Removable

Standard

Capacity	Model Number
128MB	AP-CF128ME3ER-ETNDNRK
256MB	AP-CF256ME3ER-ETNDNRK
512MB	AP-CF512ME3ER-ETNDNRK
1GB	AP-CF001GE3ER-ETNDNRK
2GB	AP-CF002GE3ER-ETNDNRK
16GB	AP-CF016GE3ER-ETNDNRK

High Speed

Capacity	Model Number
256MB	AP-CF256ME3FR-ETNDNRK
512MB	AP-CF512ME3FR-ETNDNRK
1GB	AP-CF001GE3FR-ETNDNRK
2GB	AP-CF002GE3FR-ETNDNRK
4GB	AP-CF004GE3FR-ETNDNRK
8GB	AP-CF008GE3FR-ETNDNRK

Revision History

Revision	Description	Date
1.0	Official release	Mar 8, 2011

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.
4th Fl, 75 Xintai 5th Rd., Sec.1
Hsichih, New Taipei City
Taiwan 221
R.O.C.
Tel: +886-2-2698-2888
Fax: +886-2-2698-2889
amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.
386 Fairview Way, Suite102,
Milpitas, CA 95035
Tel: 1-408-518-8699
Fax: 1-408-935-9611
sa@apacerus.com

Japan

Apacer Technology Corp.
5F, Matsura Bldg., Shiba, Minato-Ku
Tokyo, 105-0014, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe

Apacer Technology B.V.
Aziëlaan 22,
5232 BA 's-Hertogenbosch,
The Netherlands
Tel: 31-73-645-9620
Fax: 31-73-645-9629
sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd
1301, No.251,Xiaomuqiao Road, Shanghai,
200032, China
Tel: 86-21-5529-0222
Fax: 86-21-5206-6939
sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd,
#1064, 1st Floor, 7th 'A' Main,
3rd Block Koramangala, Bangalore – 560 034
Tel: +91 80 4152 9061/62/63
Fax: +91 80 4170 0215
sales_india@apacer.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Apacer:

AP-CF001GE3FR-ETNDNRK AP-CF001GE3FR-ETNRK AP-CF001GE3FR-NDNRK AP-CF001GH4FR-ETNDNRK AP-CF001GH4FR-ETNRK AP-CF001GH4FR-NDNRK AP-CF001GH4FR-NRK AP-CF002GE3FR-ETNDNRK AP-CF002GE3FR-NDNRK AP-CF002GE3FR-NRK AP-CF002GH4FR-ETNDNRK AP-CF002GH4FR-ETNRK AP-CF002GH4FR-NDNRK AP-CF002GH4FR-NRK AP-CF004GE3FR-ETNDNRK AP-CF004GE3FR-NDNRK AP-CF004GH4FR-ETNDNRK AP-CF004GH4FR-ETNRK AP-CF004GH4FR-NDNRK AP-CF004GH4FR-NRK AP-CF008GE3FR-ETNDNRK AP-CF008GE3FR-ETNRK AP-CF008GE3FR-NDNRK AP-CF008GH4FR-ETNDNRK AP-CF008GH4FR-ETNRK AP-CF008GH4FR-NDNRK AP-CF128ME3ER-ETNDNRK AP-CF128ME3ER-ETNRK AP-CF128ME3ER-NDNRK AP-CF128MH4ER-ETNDNRK AP-CF128MH4ER-ETNRK AP-CF128MH4ER-NDNRK AP-CF128MH4ER-NRK AP-CF256ME3FR-NDNRK AP-CF256ME3FR-NRK AP-CF256MH4FR-ETNDNRK AP-CF256MH4FR-ETNRK AP-CF256MH4FR-NDNRK AP-CF256MH4FR-NRK AP-CF512ME3FR-ETNDNRK AP-CF512ME3FR-ETNRK AP-CF512ME3FR-NDNRK AP-CF512ME3FR-NRK AP-CF512MH4FR-ETNDNRK AP-CF512MH4FR-ETNRK AP-CF512MH4FR-NDNRK AP-CF512MH4FR-NRK

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Apacer:

AP-CF256ME3ER-ETNDNRK AP-CF256ME3ER-ETNRK