# 54S/74S112 011007
# 54LS/74LS112 611006

## DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

**DESCRIPTION** — The '112 features individual J, K, Clock and asynchronous Set and Clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may change when the clock is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

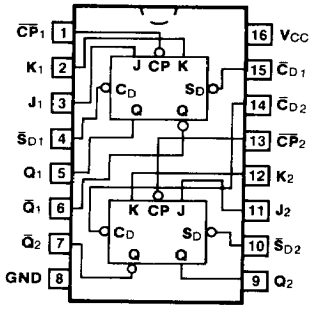
**TRUTH TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| @ $t_n$ | | @ $t_{n+1}$ |
| J | K | Q |
| L | L | $Q_n$ |
| L | H | L |
| H | L | H |
| H | H | $\overline{Q}_n$ |

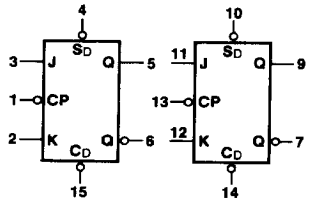
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

$t_n$ = Bit time before clock pulse.
$t_{n+1}$ = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

**CONNECTION DIAGRAM**
PINOUT A




**LOGIC SYMBOL**




$V_{CC}$ = Pin 16
GND = Pin 8

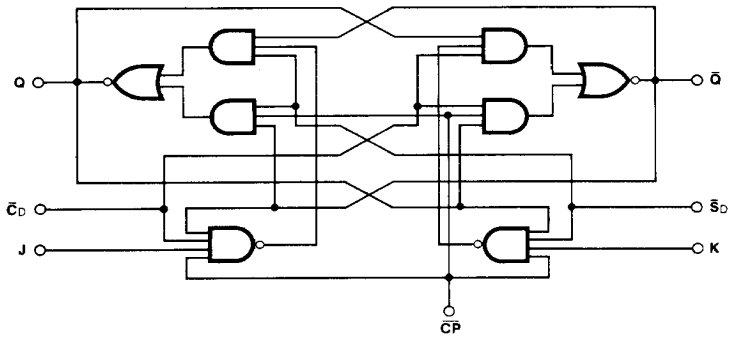
**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE: $V_{CC}$ = +5.0 V ±5%, $T_A$ = 0°C to +70°C | MILITARY GRADE: $V_{CC}$ = +5.0 V ±10%, $T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74S112PC, 74LS112PC | | 9B |
| Ceramic DIP (D) | A | 74S112DC, 74LS112DC | 54S112DM, 54LS112DM | 6B |
| Flatpak (F) | A | 74S112FC, 74LS112FC | 54S112FM, 54LS112FM | 4L |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74S (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|---|
| $J_1$, $J_2$, $K_1$, $K_2$ | Data Inputs | 1.25/1.0 | 0.5/0.25 |
| $\overline{CP}_1$, $\overline{CP}_2$ | Clock Pulse Inputs (Active Falling Edge) | 2.5/2.5 | 2.0/0.5 |
| $\overline{C}_{D1}$, $\overline{C}_{D2}$ | Direct Clear Inputs (Active LOW) | 2.5/4.375 | 1.5/0.5 |
| $\overline{S}_{D1}$, $\overline{S}_{D2}$ | Direct Set Inputs (Active LOW) | 2.5/4.375 | 1.5/0.5 |
| $Q_1$, $Q_2$, $\overline{Q}_1$, $\overline{Q}_2$ | Outputs | 25/12.5 | 10/5.0 (2.5) |

**LOGIC DIAGRAM** (one half shown)




**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | 54/74S | | 54/74LS | | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $I_{CC}$ | Power Supply Current | | 50 | | 8.0 | mA | $V_{CC}$ = Max, $V_{CP}$ = 0 V |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25° C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74S | | 54/74LS | | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | $C_L$ = 15 pF | | | |
| | | Min | Max | Min | Max | | |
| $f_{max}$ | Maximum Clock Frequency | 80 | | 30 | | MHz | Figs. 3-1, 3-9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{CP}_n$ to $Q_n$ or $\overline{Q}_n$ | | 7.0<br>7.0 | | 16<br>24 | ns | Figs. 3-1, 3-9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | | 7.0<br>7.0 | | 16<br>24 | ns | Figs. 3-1, 3-10 |

**AC OPERATING REQUIREMENTS:** $V_{CC}$ = +5.0 V, $T_A$ = +25° C

| SYMBOL | PARAMETER | 54/74S | | 54/74LS | | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_s$ (H)<br>$t_s$ (L) | Setup Time<br>$J_n$ or $K_n$ to $\overline{CP}_n$ | 7.0<br>7.0 | | 20<br>15 | | ns | Fig. 3-7 |
| $t_h$ (H)<br>$t_h$ (L) | Hold Time<br>$J_n$ or $K_n$ to $\overline{CP}_n$ | 0<br>0 | | 0<br>0 | | ns | |
| $t_w$ (H)<br>$t_w$ (L) | $\overline{CP}_n$ Pulse Width | 6.0<br>6.5 | | 20<br>15 | | ns | Fig. 3-9 |
| $t_w$ (L) | $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW | 8.0 | | 15 | | ns | Fig. 3-10 |