

M66310P/FP

16-Bit LED Driver with Shift Register and Latch

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Description

M66310P/FP is a LED array driver having a 16 bit serial-input and parallel output shift-register function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24 mA which is sufficient for cathode common LED drive, capable of flowing 16 bits continuously at the same time.

Parallel output is open drain output.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin layout ensures the realization of an easy printed circuit.

Features

- Cathode common LED drive
- High output current
all parallel output $I_{OH} = -24$ mA
simultaneous lighting available
- Low power dissipation: 100 μ W/package (max)
($V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$, quiescent state)
- High noise margin
schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output (except serial data output)
- Wide operating temperature range: $T_a = -40$ to $+85^\circ\text{C}$
- Pin layout facilitates printed circuit wiring. (This layout facilitates cascade connection and LED connection.)

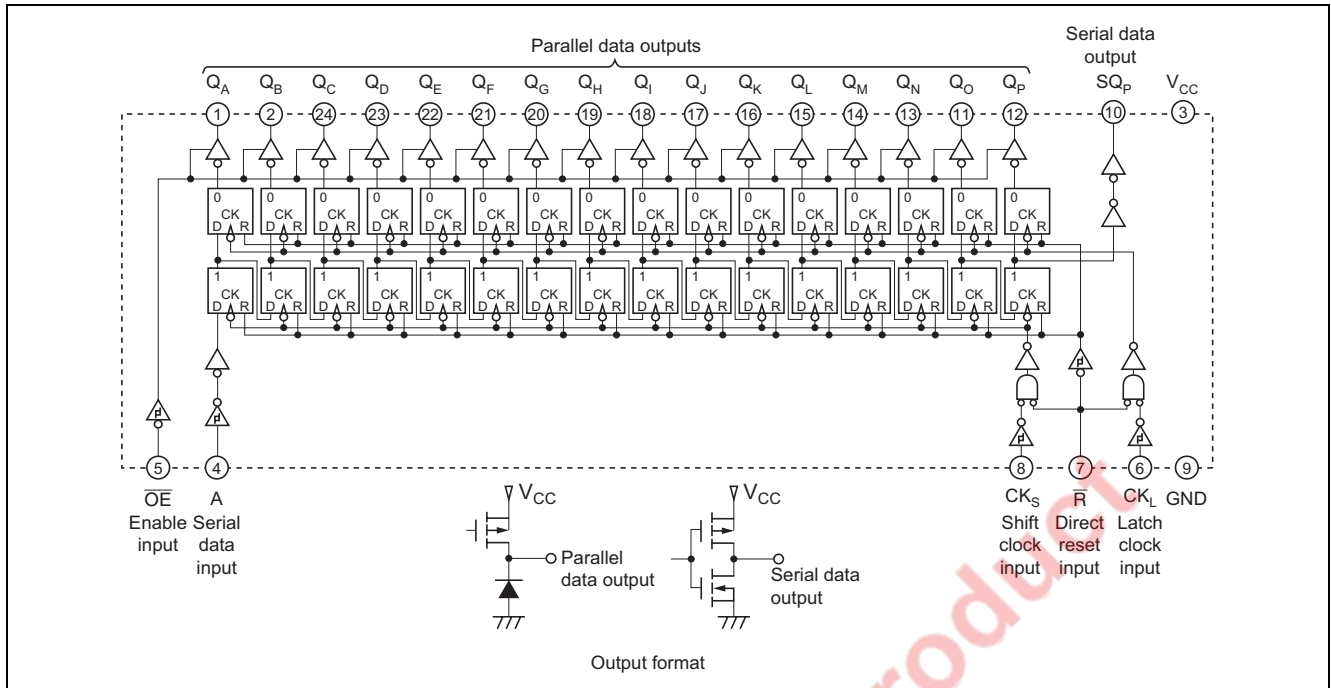
Application

LED array drive of BUTTON TELEPHONE

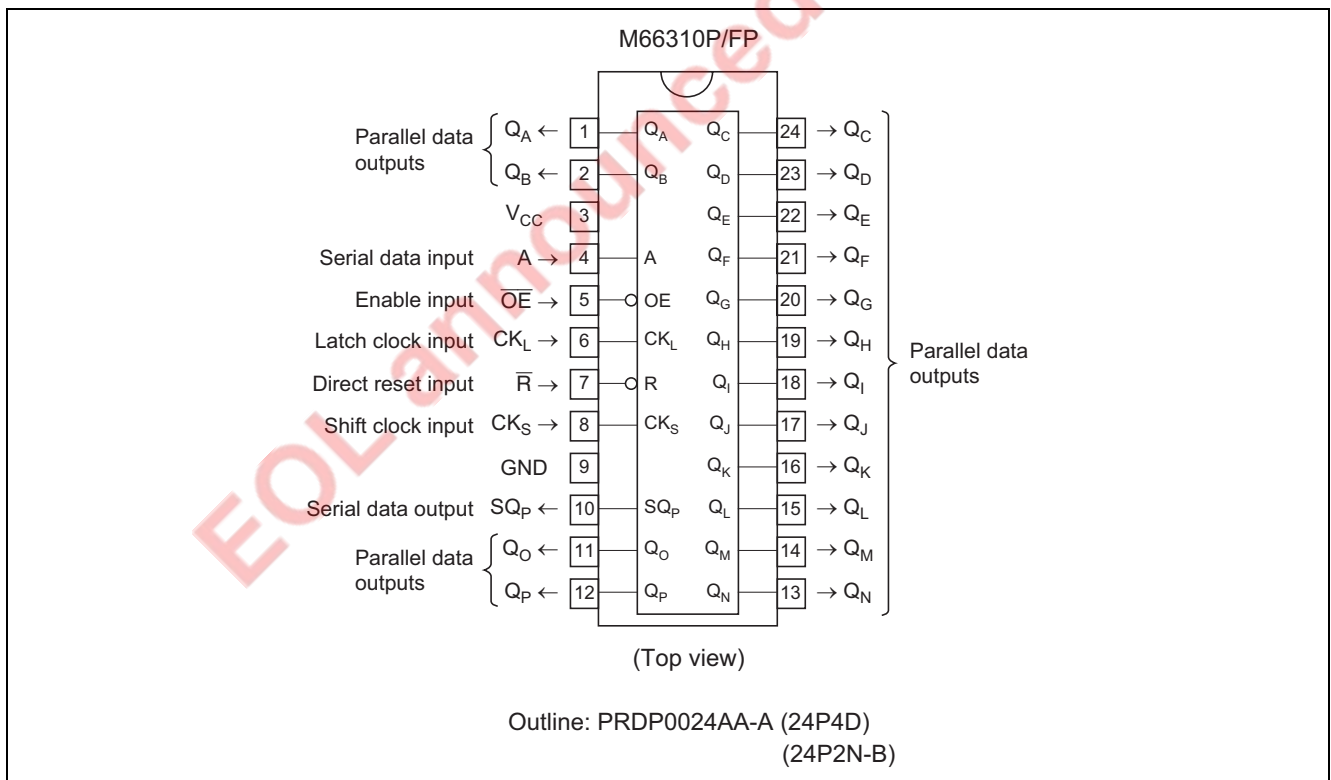
LED array drive of ERASER of a PPC copier

Other various LED modules

Logic Diagram



Pin Arrangement



Functional Description

As M66310P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shift-register consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shift-register and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S . When A is "L", the signal of "L" shifts.

When the pulse is impressed to CK_L , the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from Q_A to Q_P .

Outputs from Q_A to Q_P are open drain outputs.

To extend the number of bits, use the serial data output SQ_P which shows the output of the shifting register of the 16th bit.

If CK_S and CK_L are connected, the state of the shifting register with one clock delay is outputted to Q_A to Q_P .

When reset input \bar{R} is changed to "L", Q_A to Q_P and SQ_P are reset. In this case, shifting and latching registers are reset.

If "H" is impressed to output enable input \overline{OE} , Q_A to Q_P reaches the high impedance state, but SQ_P does not reach the high impedance state. Furthermore, change in \overline{OE} does not affect shift operation.

Function Table (Note)

Operation Mode		Input					Parallel Data Output																	Serial Data Output SQ _P	Remarks
		R̄	CK _S	CK _L	A	OĒ	Q _A	Q _B	Q _C	Q _D	Q _E	Q _F	Q _G	Q _H	Q _I	Q _J	Q _K	Q _L	Q _M	Q _N	Q _O	Q _P			
Reset		L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	–	
Shift latch operation	Shift t1	H	↑	X	H	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	Q _I ⁰	Q _J ⁰	Q _K ⁰	Q _L ⁰	Q _M ⁰	Q _N ⁰	Q _O ⁰	Q _P ⁰	q _O ⁰	Output lighting "H"	
	Latch t2	H	X	↑	X	L	H	q _A ⁰	q _B ⁰	q _C ⁰	q _D ⁰	q _E ⁰	q _F ⁰	q _G ⁰	q _H ⁰	q _I ⁰	q _J ⁰	q _K ⁰	q _L ⁰	q _M ⁰	q _N ⁰	q _O ⁰	q _P ⁰		
	Shift t1	H	↑	X	L	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	Q _I ⁰	Q _J ⁰	Q _K ⁰	Q _L ⁰	Q _M ⁰	Q _N ⁰	Q _O ⁰	Q _P ⁰	q _O ⁰	Output lights-out "L"	
	Latch t2	H	X	↑	X	L	Z	q _A ⁰	q _B ⁰	q _C ⁰	q _D ⁰	q _E ⁰	q _F ⁰	q _G ⁰	q _H ⁰	q _I ⁰	q _J ⁰	q _K ⁰	q _L ⁰	q _M ⁰	q _N ⁰	q _O ⁰	q _P ⁰		
Output disable		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q _P	–	

Note ↑: Change from low-level to high-level
 Q^0 : Output state Q before CK_L changed
 X: Irrelevant
 q^0 : Contents of shift register before CK_S changed
 q: Contents of shift register
 t_1, t_2 : t_2 is set after t_1 is set
 Z: High impedance

Absolute Maximum Ratings

(Ta = -40 to +85°C, unless otherwise noted)

Item		Symbol	Ratings	Unit	Conditions
Supply voltage		V _{CC}	-0.5 to +7.0	V	
Input voltage		V _I	-0.5 to V _{CC} + 0.5	V	
Output voltage		V _O	-0.5 to V _{CC} + 0.5	V	
Input protection diode current		I _{IK}	-20	mA	V _I < 0 V
			20		V _I > V _{CC}
Output parasitic diode current		I _{OK}	-20	mA	V _O < 0 V
			20		V _O > V _{CC}
Output current per output pin	Q _A to Q _P	I _O	-50	mA	
	SQ _P		±25		
Supply/GND current		I _{CC}	-410, +20	mA	V _{CC} , GND
Power dissipation		P _d	500	mW	(Note)
Storage temperature range		T _{stg}	-65 to +150	°C	

Note: M66310FP; Ta = -40 to +70°C, Ta = 70 to 85°C are derated at -6 mW/°C.

Recommended Operating Conditions

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V _{CC}	4.5	5	5.5	V
Input voltage	V _I	0	—	V _{CC}	V
Output voltage	V _O	0	—	V _{CC}	V
Operating temperature range	Topr	-40	—	+85	°C

Electrical Characteristics

(V_{CC} = 4.5 to 5.5 V, unless otherwise noted)

Item	Symbol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = –40 to +85°C				
		Min	Typ	Max	Min	Max			
Positive-going threshold voltage	V _{T+}	0.35×V _{CC}	—	0.7×V _{CC}	0.35×V _{CC}	0.7×V _{CC}	V	V _O = 0.1V, V _{CC} –0.1V I _O = 20 μA	
Negative-going threshold voltage	V _{T–}	0.2×V _{CC}	—	0.55×V _{CC}	0.2×V _{CC}	0.55×V _{CC}	V	V _O = 0.1V, V _{CC} –0.1V I _O = 20 μA	
High-level output voltage Q _A to Q _P	V _{OH}	V _{CC} –0.1	—	—	V _{CC} –0.1	—	V	V _I = V _{T+} , V _{T–} V _{CC} = 4.5 V	I _{OH} = –20 μA
		3.83	—	—	3.66	—			I _{OH} = –24 mA
		3.50	—	—	3.25	—			I _{OH} = –40 mA ^(Note)
High-level output voltage SQ _P	V _{OH}	V _{CC} –0.1	—	—	V _{CC} –0.1	—	V	V _I = V _{T+} , V _{T–} V _{CC} = 4.5 V	I _{OH} = –20 μA
		3.83	—	—	3.66	—			I _{OH} = –4 mA
Low-level output voltage SQ _P	V _{OL}	—	—	0.1	—	0.1	V	V _I = V _{T+} , V _{T–} V _{CC} = 4.5 V	I _{OL} = 20 μA
		—	—	0.44	—	0.53			I _{OL} = 4 mA
High-level input current	I _{IH}	—	—	0.5	—	5.0	μA	V _I = V _{CC} , V _{CC} = 5.5 V	
Low-level input current	I _{IL}	—	—	–0.5	—	–5.0	μA	V _I = GND, V _{CC} = 5.5 V	
Maximum output leakage current Q _A to Q _P	I _O	—	—	1.0	—	10.0	μA	V _I = V _{T+} , V _{T–} V _{CC} = 5.5 V	V _O = V _{CC}
		—	—	–1.0	—	–10.0			V _O = GND
Quiescent supply current	I _{CC}	—	—	20.0	—	200.0	μA	V _I = V _{CC} , GND, V _{CC} = 5.5 V	

Note: M66310 is used under the condition of an output current I_{OH} = –40 mA, the number of simultaneous drive outputs are restricted as shown in the Duty Cycle-I_{OH} of Standard characteristics.

Switching Characteristics

(V_{CC} = 5V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = -40 to +85°C			
		Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	5	—	—	4	—	MHz	C _L = 50 pF R _L = 1 kΩ (Note 2)
Low-level to high-level and high-level to low-level output propagation time (CK _S -SQ _P)	t _{PLH}	—	—	100	—	130	ns	
	t _{PHL}	—	—	100	—	130	ns	
High-level to low-level output propagation time (R̄-SQ _P)	t _{PHL}	—	—	100	—	130	ns	
High-level to low-level output propagation time (R̄-Q _A to Q _P)	t _{PHZ}	—	—	150	—	200	ns	
Low-level to high-level and high-level to low-level output propagation time (CK _L -Q _A to Q _P)	t _{PZH}	—	—	100	—	130	ns	
	t _{PHZ}	—	—	150	—	200	ns	
Output enable time to low-level and high-level (OE-Q _A to Q _P)	t _{PZH}	—	—	100	—	130	ns	
	t _{PHZ}	—	—	150	—	200	ns	
Input Capacitance	C _I	—	—	10	—	10	pF	
Output Capacitance	C _O	—	—	15	—	15	pF	OE = V _{CC}
Power dissipation Capacitance (Note 1)	C _{PO}	—	11	—	—	—	pF	

Note: 1. C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)

The power dissipated during operation under no-load conditions is calculated using the following formula:

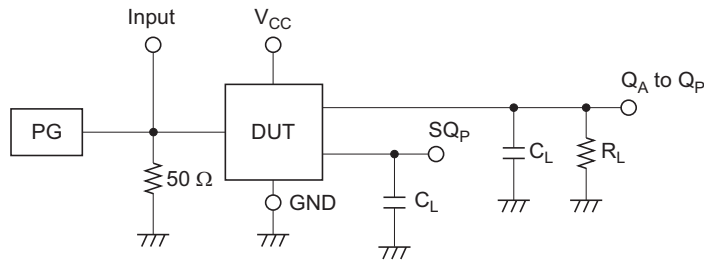
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$

Timing Requirements

(V_{CC} = 5 V)

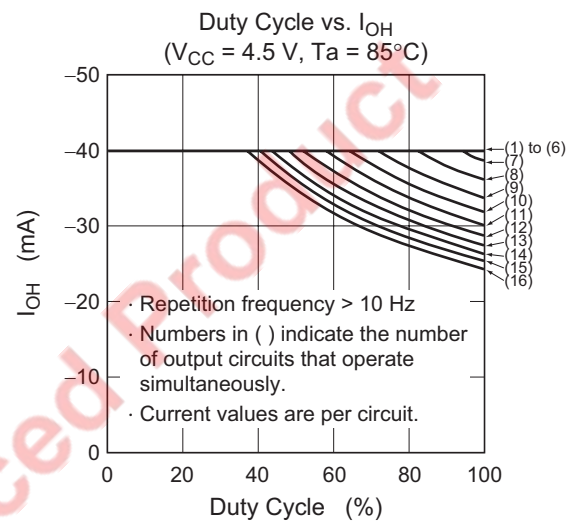
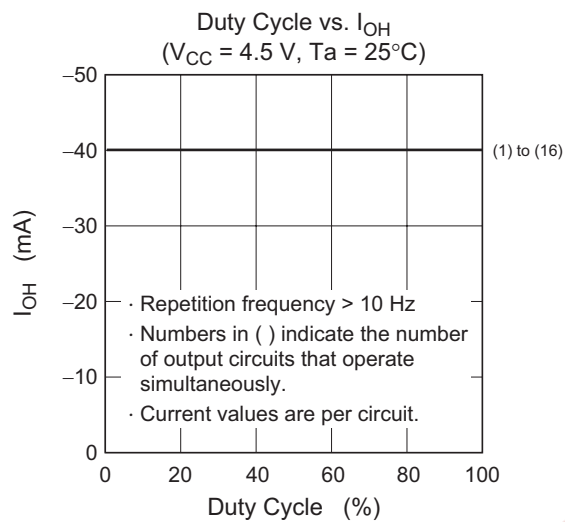
Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = −40 to +85°C			
		Min	Typ	Max	Min	Max		
CK _S , CK _L , \overline{R} pulse width	t _w	100	—	—	130	—	ns	(Note 2)
A setup time with respect to CK _S	t _{su}	100	—	—	130	—	ns	
CK _S setup time with respect to CK _L	t _{su}	100	—	—	130	—	ns	
A hold time with respect to CK _S	t _h	10	—	—	15	—	ns	
\overline{R} , recovery time with respect to CK _S , CK _L	t _{rec}	50	—	—	70	—	ns	

Note: 2. Test Circuit

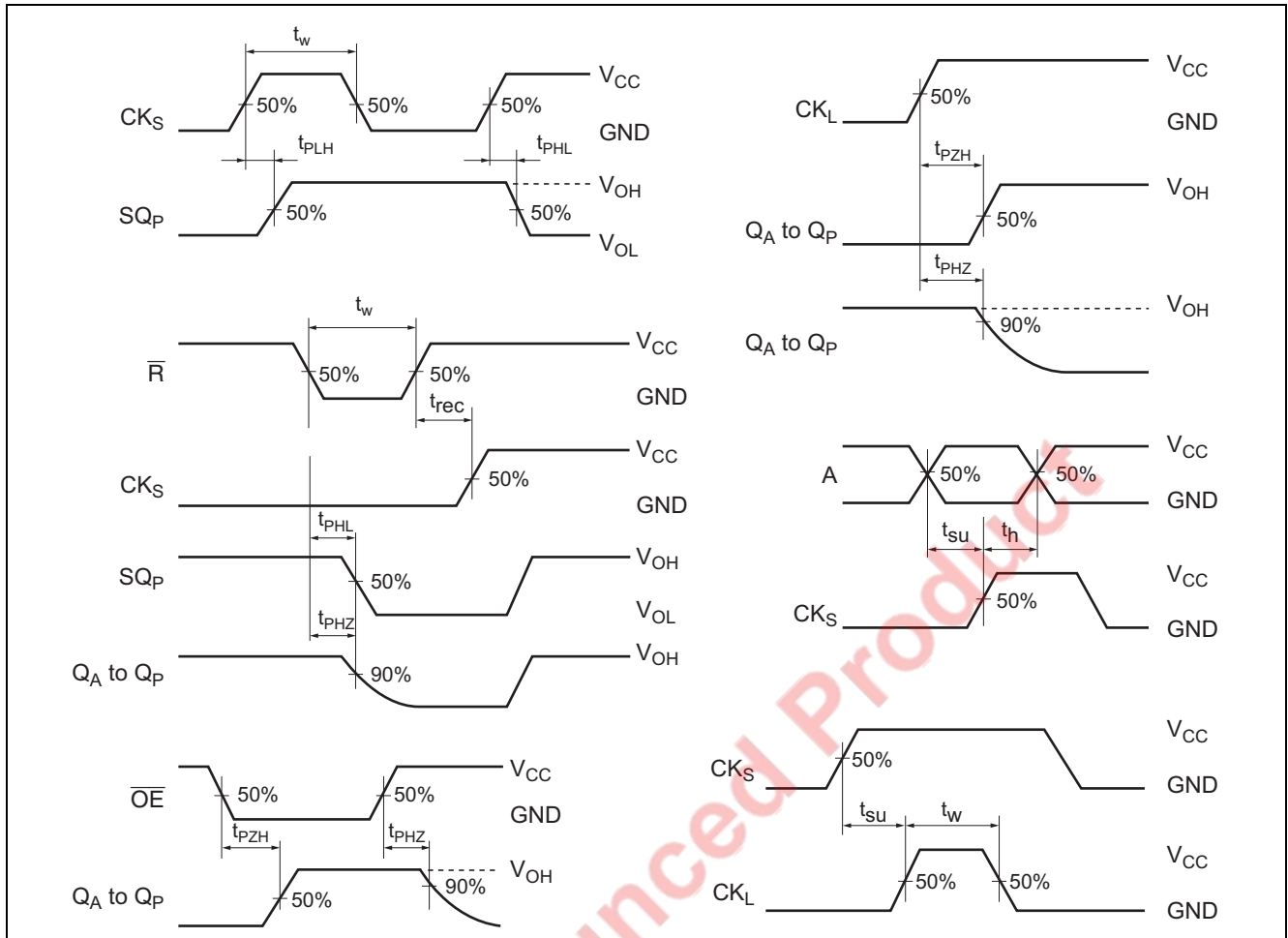


- (1) The pulse generator (PG) has the following characteristics (10% to 90%): $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

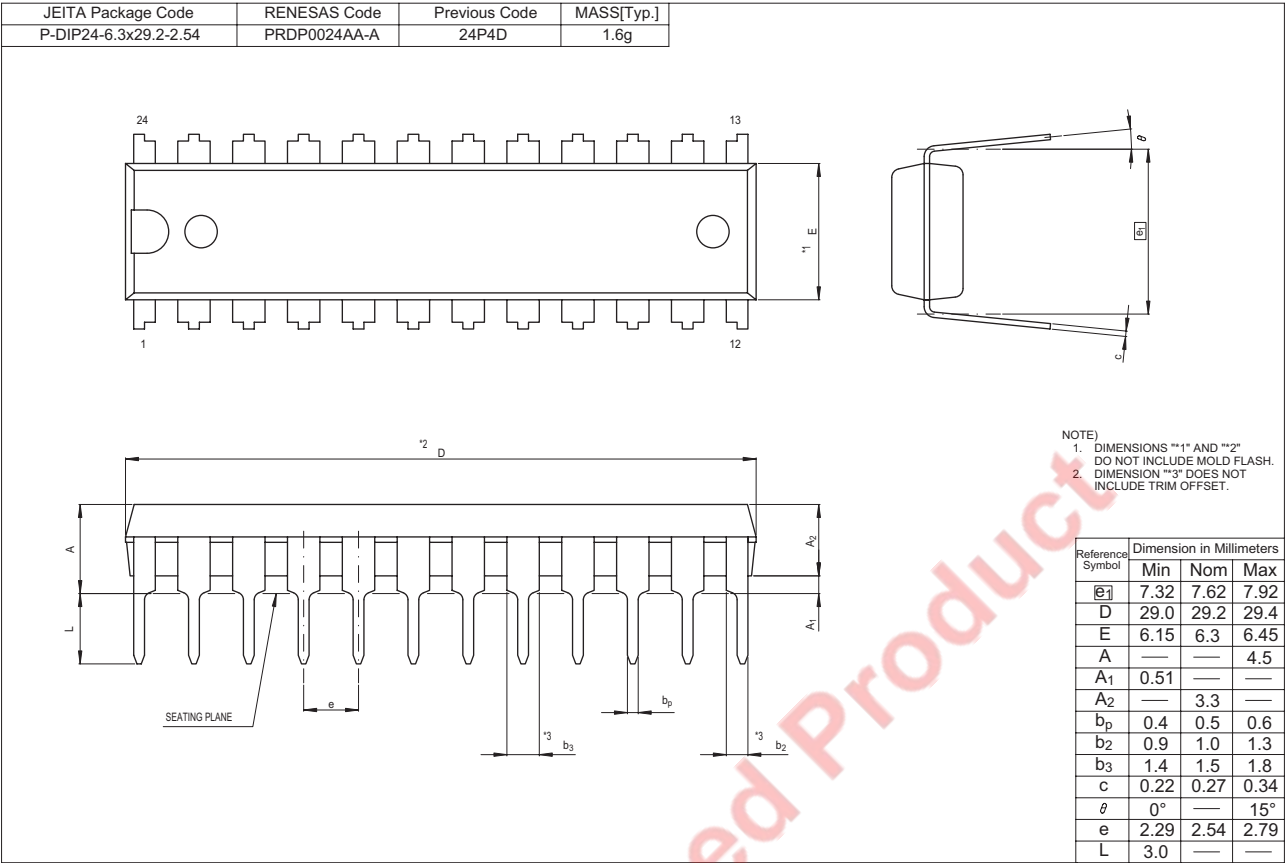
Typical Characteristics



Timing Chart

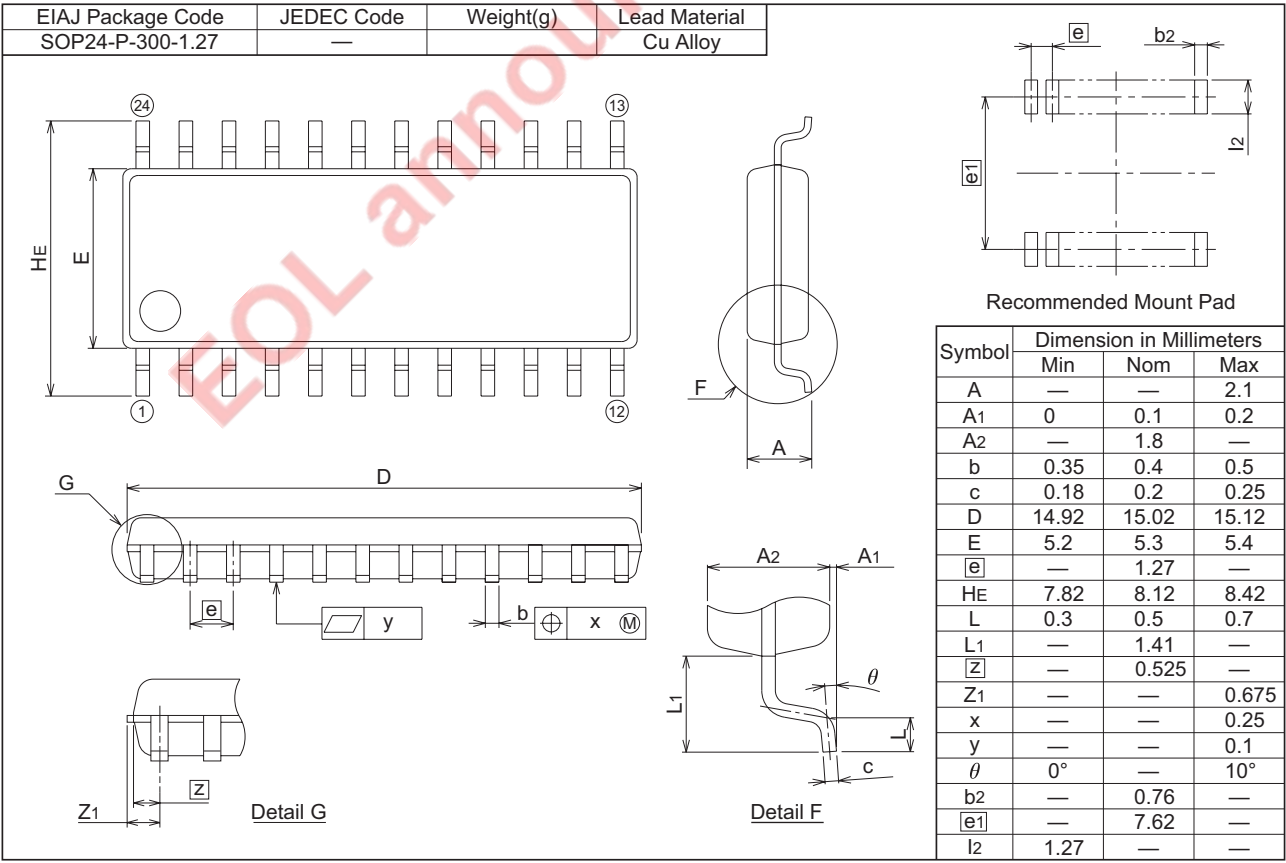


Package Dimensions



24P2N-B

Plastic 24pin 300mil SOP



Notes:

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