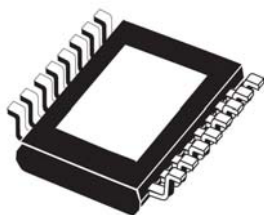


Quad channel high-side driver with CurrentSense analog feedback for automotive applications


PowerSSO-16

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	100 m Ω
Current limitation (typ)	I_{LIMH}	15 A
Stand-by current (max)	I_{STBY}	0.5 μ A
Minimum cranking supply Voltage (V_{CC} decreasing)	$V_{USD_cranking}$	2.85 V

- AEC-Q100 qualified 
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
 - Quad channel smart high-side driver with CurrentSense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
 - Analog feedback of load current with high precision proportional current mirror
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Configurable latch-off on overtemperature or power limitation
 - Loss of ground and loss of V_{CC}
 - Reverse battery with external components
 - Electrostatic discharge protection

Product status	
VNQ7E100AJ	
Product summary	
Order code	VNQ7E100AJTR
Package	PowerSSO-16
Packing	Tape and reel

Applications

- Automotive resistive, inductive and capacitive loads
- Protected supply for ADAS systems: radars and sensors
- Automotive lamps

Description

The device is a quad channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in a PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

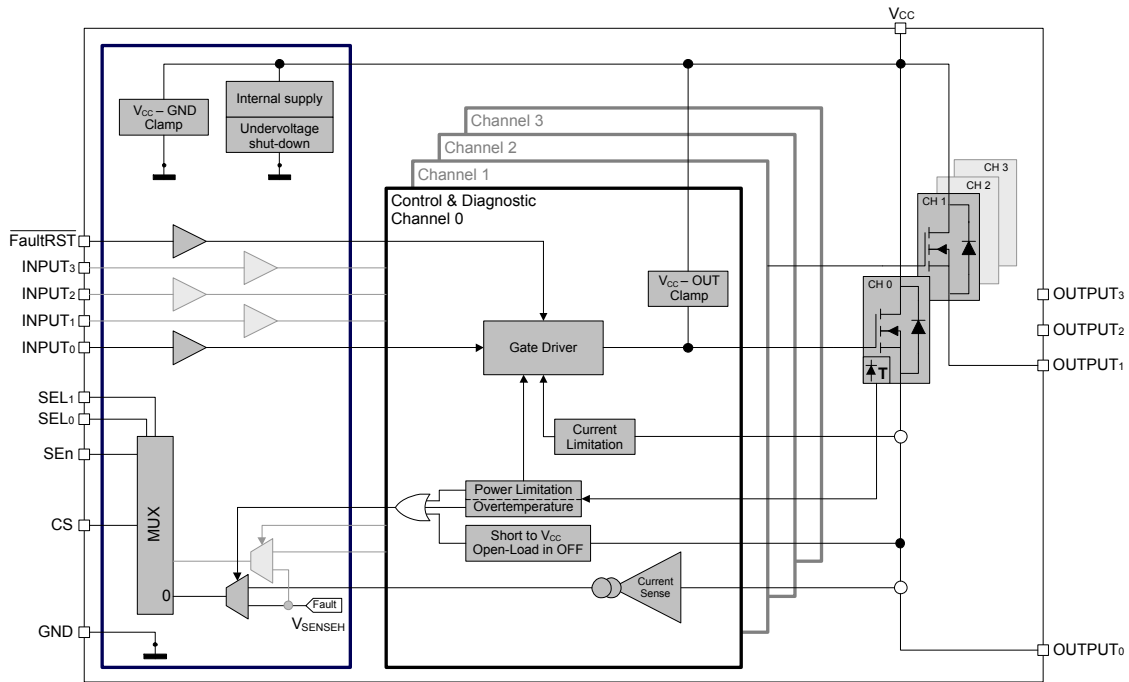
The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A multiplexed current sense pin delivers high precision proportional load current sense in addition to the detection of overload and short circuit to ground, short to V_{CC} and off-state openload.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

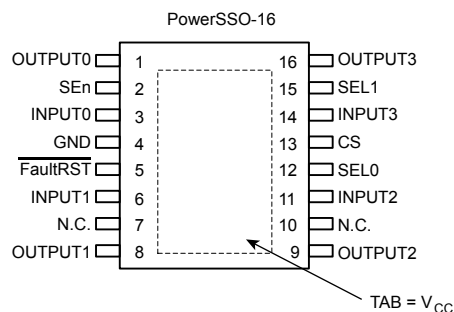
1 Block diagram and pin description

Figure 1. Block diagram


GADG1003171112PS

Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT _{0,1,2,3}	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT _{0,1,2,3}	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
CS	Analog current sense output pin delivers a current proportional to the load current.
SEn	Active high, compatible with 3 V and 5 V CMOS outputs input pin; it enables the CS diagnostic pin.
SEL _{0,1}	Active high, compatible with 3 V and 5 V CMOS outputs input pin; They address the CS multiplexer.
FaultRST	Active low, compatible with 3 V and 5 V CMOS outputs input pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)


GAPGCFT00632

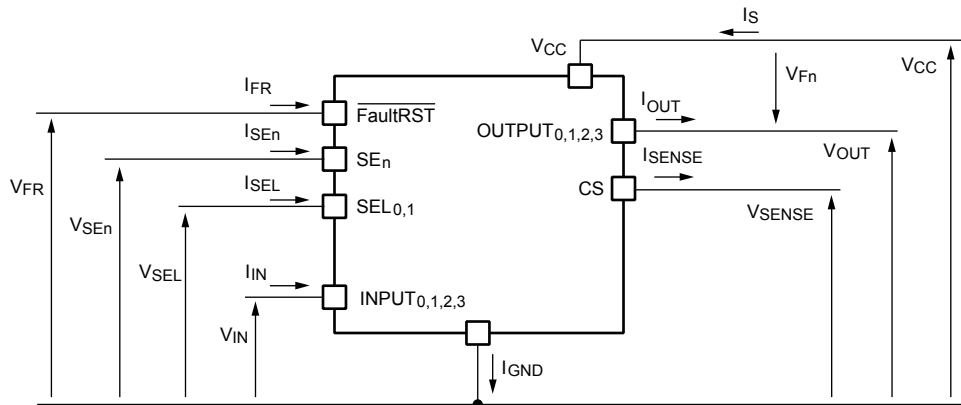
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CS	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 k Ω resistor	X	Not allowed	Through 15 k Ω resistor	Through 15 k Ω resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



GADG0704171646PS

Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3. Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4 \Omega$)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT _{0,1,2,3} DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	7.5	
I_{IN}	INPUT _{0,1,2,3} DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	SEL _{0,1} DC input current		
I_{FR}	FaultRST DC input current	-1 to 1.5	mA
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)	-20	

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4 \text{ ms}$; $T_{jstart} = 150^\circ\text{C}$)	10	mJ
V_{ESD}	JEDEC standard (Electrostatic discharge)	JEDEC 22A-114F	
	INPUT _{0,1,2,3}	4000	V
	CS, SEn	2000	
	SEL _{0,1} , $\overline{\text{FaultRST}}$	4000	
	OUTPUT _{0,1,2,3}	4000	
	V _{CC}	4000	
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) ⁽¹⁾⁽²⁾	7.7	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽¹⁾⁽³⁾	60.3	
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾	27.1	
$R_{thj-top}$	Thermal resistance junction-top (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾	13.5	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB.
3. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace.

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. Electrical characteristics during cranking

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{USD_Cracking}	Minimum cranking supply voltage (V _{CC} decreasing)				2.85	V
R _{ON}	On-state resistance ⁽¹⁾	I _{OUT} = 0.2 A; V _{CC} = 2.85 V; V _{CC} decreasing			300	mΩ
T _{TSD} ⁽²⁾	Shutdown temperature (V _{CC} decreasing)	V _{CC} = 2.85 V	140			°C

1. For each channel.

2. Parameter guaranteed by design and characterization; not subject to production test.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		4	13	28	V
V _{USD}	Undervoltage shutdown				2.85	
V _{USDReset}	Undervoltage shutdown reset				5	
V _{USDhyst}	Undervoltage shutdown hysteresis			0.3		
R _{ON}	On-state resistance ⁽¹⁾	I _{OUT} = 1 A; T _j = 25°C		100		mΩ
		I _{OUT} = 1 A; T _j = 150°C			210	
		I _{OUT} = 1 A; V _{CC} = 4 V; T _j = 25°C ⁽²⁾			160	
V _{clamp}	Clamp voltage	I _S = 20 mA; 25°C < T _j < 150°C	41	46	52	V
		I _S = 20 mA; T _j = -40°C	38			
I _{STBY}	Supply current in Standby at V _{CC} = 13 V ⁽³⁾	V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEn} = 0 V; V _{SEL0,1} = 0 V; T _j = 25°C			0.5	μA
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEn} = 0 V; V _{SEL0,1} = 0 V; T _j = 85°C ⁽⁴⁾			0.5	μA
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEn} = 0 V; V _{SEL0,1} = 0 V; T _j = 125°C			3	μA
t _{D_STBY}	Standby mode blanking time	V _{CC} = 13 V V _{IN} = V _{OUT} = V _{FR} = V _{SEL0,1} = 0 V; V _{SEn} = 5 V to 0 V	60	300	550	μs
I _{S(ON)}	Supply current	V _{CC} = 13 V; V _{SEn} = V _{FR} = V _{SEL0,1} = 0 V; V _{IN0,1,2,3} = 5 V; I _{OUT0,1,2,3} = 0 A		10	16	mA
I _{GND(ON)}	Control stage current consumption in ON state. All channels active.	V _{CC} = 13 V; V _{SEn} = 5 V; V _{FR} = V _{SEL0,1} = 0 V; V _{IN0,1,2,3} = 5 V; I _{OUT0,1,2,3} = 1 A			20	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off)}$	Off-state output current at $V_{CC} = 13\text{ V}$ ⁽¹⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25^\circ\text{C}$	0	0.01	0.5	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125^\circ\text{C}$	0		3	
V_F	Output - V_{CC} diode voltage at $T_j = 150^\circ\text{C}$	$I_{OUT} = -1\text{ A}$; $T_j = 150^\circ\text{C}$			0.7	V

1. For each channel.
2. Parameter guaranteed only at $V_{CC} = 4\text{ V}$ and $T_j = 25^\circ\text{C}$
3. PowerMOS leakage included.
4. Parameter specified by design; not subject to production test.

Table 7. Switching

$V_{CC} = 13\text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ ⁽¹⁾	Turn-on delay time at $T_j = 25^\circ\text{C}$	$R_L = 13\ \Omega$	10	50	120	μs
$t_{d(off)}$ ⁽¹⁾	Turn-off delay time at $T_j = 25^\circ\text{C}$		10	35	100	
$(dV_{OUT}/dt)_{on}$ ⁽¹⁾	Turn-on voltage slope at $T_j = 25^\circ\text{C}$	$R_L = 13\ \Omega$	0.1	0.3	0.7	V/ μs
$(dV_{OUT}/dt)_{off}$ ⁽¹⁾	Turn-off voltage slope at $T_j = 25^\circ\text{C}$		0.1	0.4	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	$R_L = 13\ \Omega$	—	0.15	0.5 ⁽²⁾	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	$R_L = 13\ \Omega$	—	0.1	0.5 ⁽²⁾	mJ
t_{SKEW} ⁽¹⁾	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 13\ \Omega$	-65	-15	35	μs

1. See [Figure 6. Switching times and Pulse skew](#).
2. Parameter guaranteed by design and characterization, not subject to production test

Table 8. Logic Inputs

7 V < V _{CC} < 28 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT _{0,1,2,3} characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
FaultRST characteristics						
V _{FRL}	Input low level voltage				0.9	V

7 V < V _{CC} < 28 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{FRL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{FRH}	Input high level voltage		2.1			V
I _{FRH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{FR(hyst)}	Input hysteresis voltage		0.2			V
V _{FRCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		
SEL _{0,1} characteristics (7 V < V _{CC} < 18 V)						
V _{SELL}	Input low level voltage				0.9	V
I _{SELL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SELH}	Input high level voltage		2.1			V
I _{SELH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V _{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		

Table 9. Protections

7 V < V _{CC} < 28 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH}	DC short circuit current	V _{CC} = 13 V	11	15	22	A
		4 V < V _{CC} < 18 V ⁽¹⁾			22	
I _{LIML}	Short circuit current during thermal cycling	V _{CC} = 13 V; T _R < T _j < T _{TSD}		6		
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽¹⁾		T _{RS} + 1	T _{RS} + 7		
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V;	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R) ⁽¹⁾			7		
ΔT _{J_SD}	Dynamic temperature	T _j = -40°C; V _{CC} = 13 V		60		K

7 V < V _{CC} < 28 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{LATCH_RST}	Fault reset time for output unlatch ⁽¹⁾	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V • E.g. Ch ₀ V _{IN0} = 5 V; V _{SEL0,1} = 0 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 1 A; L = 6 mH; T _j = -40°C	V _{CC} - 38			V
		I _{OUT} = 1 A; L = 6 mH; T _j = 25°C to 150°C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V

1. Parameter guaranteed by design and characterization; not subject to production test.

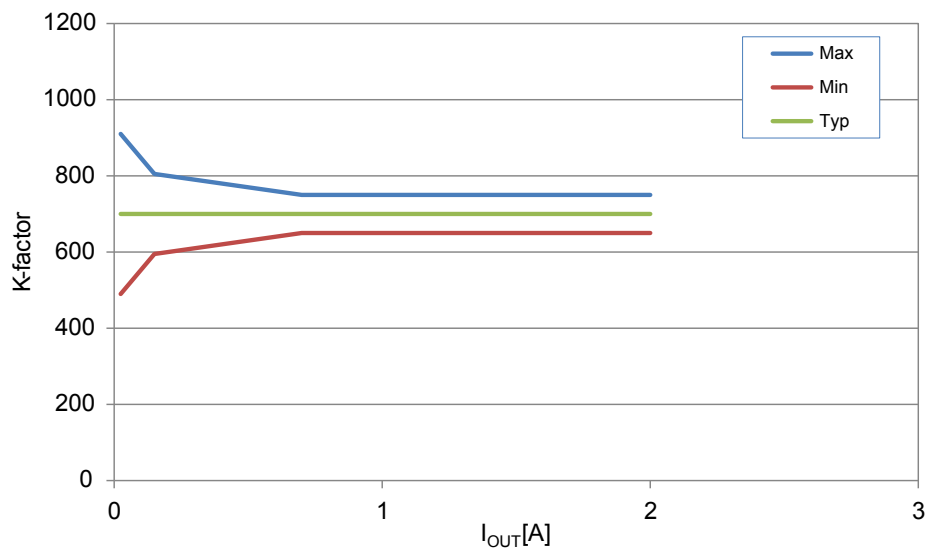
Table 10. CurrentSense

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	Current sense clamp voltage	V _{SEn} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{SEn} = 0 V; I _{SENSE} = -1 mA		7		
Current Sense characteristics						
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-30%	710	+30%	
dK ₀ /K ₀ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-20		+20	%
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-15%	710	+15%	
dK ₁ /K ₁ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-10		+10	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-7%	710	+7%	
dK ₂ /K ₂ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-6		+6	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-7%	710	+7%	
dK ₃ /K ₃ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-6		+6	%
I _{SENSE_OL}	CS current for OL detection	I _{OUT} = 0.01 A; V _{SENSE} = 4 V; V _{SEn} = 5 V			24	μA
I _{SENSE0}	Current sense leakage current	Current sense disabled: V _{SEn} = 0 V;	0		0.5	μA
		Current sense disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾	-0.5		0.5	
		Current sense enabled: V _{SEn} = 5 V All channels ON; I _{OUTX} = 0 A; Ch _X diagnostic selected: • E.g. Ch ₀ : V _{IN0,1,2,3} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT0} = 0 A; I _{OUT1,2,3} = 1 A	0		10	
		Current sense enabled: V _{SEn} = 5 V; Ch _X OFF; Ch _X diagnostic selected: • E.g. Ch ₀ : V _{IN0} = 0 V; V _{IN1,2,3} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT1,2,3} = 1 A	0		2	

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{OUT_MSD} ⁽¹⁾	Output Voltage for Current sense shutdown	V _{SEn} = 5 V; R _{SENSE} = 2.7 kΩ • E.g. Ch ₀ : V _{IN0} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT0} = 1 A		5		V
V _{SENSE_SAT}	CS saturation voltage	V _{CC} = 7 V; R _{SENSE} = 2.7 kΩ; V _{SEn} = 5 V; V _{IN0} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 2 A; T _j = -40 °C	4.8			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; T _j = 150 °C	4			mA
I _{OUT_SAT} ⁽¹⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; T _j = 150 °C	3.1			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{SEn} = 5 V; Ch _X OFF; Ch _X diagnostic selected • E.g. Ch ₀ V _{IN0} = 0 V; V _{SEL0,1} = 0 V	2	3	4	V
I _{L(off2)} ⁽³⁾	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40°C to 125°C	-100		-15	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 8. T _{DSKON})	V _{SEn} = 5 V; Ch _X ON to OFF transition; Ch _X diagnostic selected: • E.g. Ch ₀ V _{IN0} = 5 V to 0 V; V _{SEL0,1} = 0 V; V _{OUT0} = 4 V; I _{OUT0} = 0 A	100	350	700	μs
t _{D_OL_V}	Settling time for valid OFF-state open-load diagnostic indication from rising edge of SE _n	V _{IN0,1,2,3} = 0 V; V _{FR} = 0 V; V _{SEL0,1} = 0 V; V _{OUT0} = 4 V; V _{SEn} = 0 V to 5 V			60	μs
t _{D_VOL}	OFF-state diagnostic delay time from rising edge of V _{OUT}	V _{SEn} = 5 V; Ch _X OFF; Ch _X diagnostic selected: • E.g. Ch ₀ V _{IN0} = 0 V; V _{SEL0,1} = 0 V; V _{OUT0} = 0 V to 4 V		5	30	μs
Fault diagnostic feedback (see Table 11. Truth table)						
V _{SENSEH}	Current sense output voltage in fault condition	V _{CC} = 13 V; R _{SENSE} = 1 kΩ • E.g. Ch ₀ in open load V _{IN0} = 0 V; V _{SEn} = 5 V; V _{SEL0,1} = 0 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	5		6.6	V
I _{SENSEH}	Current sense output current in fault condition	V _{CC} = 13 V; V _{SENSE} = 5 V	7	20	30	mA
Current sense timings (current sense mode - see Figure 7. Current sense timings (current sense mode))⁽⁴⁾						
t _{DSSENSE1H}	Current sense settling time from rising edge of SE _n	V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω			60	μs
t _{DSSENSE1L}	Current sense disable delay time from falling edge of SE _n	V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω		5	20	μs

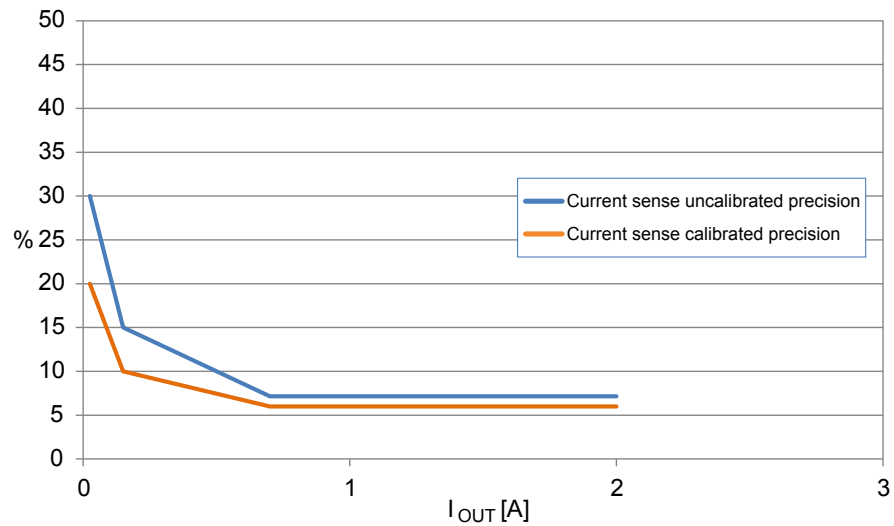
7 V < V _{CC} < 18 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω		100	250	μs
Δt _{DSENSE2H}	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 6.5 Ω			100	μs
t _{DSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω		50	250	μs
Current sense timings (Multiplexer transition times) ⁽⁴⁾						
t _{D_XtoY}	Current sense transition delay from Ch _X to Ch _Y	V _{IN0} = 5 V; V _{IN1} = 5 V; V _{SEn} = 5 V; V _{SEL1} = 0 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 0 A; I _{OUT1} = 1 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CS to VSENSEH}	Current sense transition delay from stable current sense on Ch _X to V _{SENSEH} on Ch _Y	V _{IN0} = 5 V; V _{IN1} = 0 V; V _{SEn} = 5 V; V _{SEL1} = 0 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 1 A; V _{OUT1} = 4 V; R _{SENSE} = 1 kΩ			20	μs

1. Parameter defined by design. Not subject to production test.
2. All values refer to V_{CC} = 13 V; T_J = 25°C, unless otherwise specified.
3. Parameter granted at -40 °C < T_J < 125 °C"
4. Transition delay are measured up to +/- 10% of final conditions.

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}


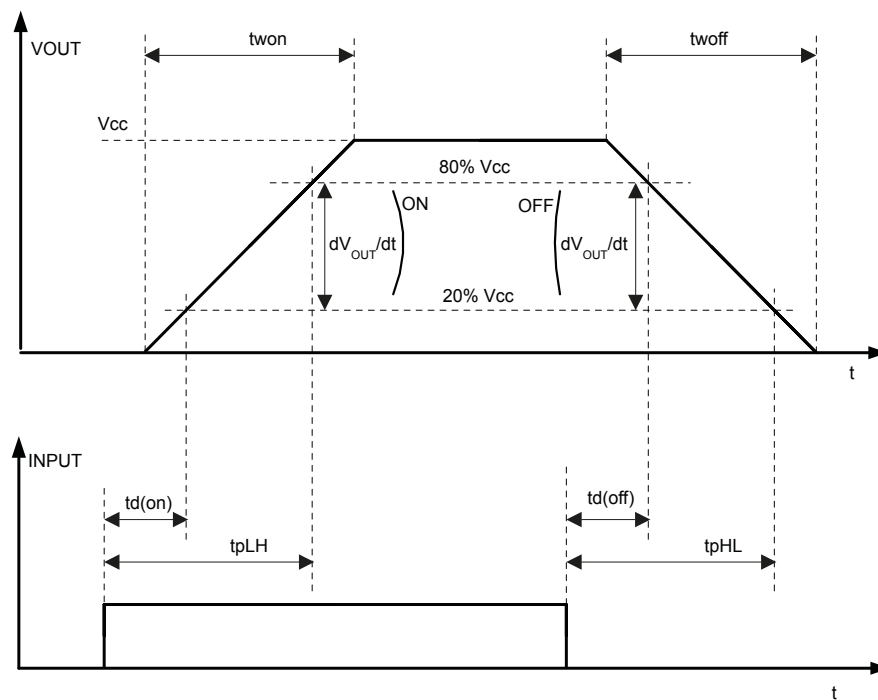
GADG0903171157PS

Figure 5. Current sense accuracy versus I_{OUT}



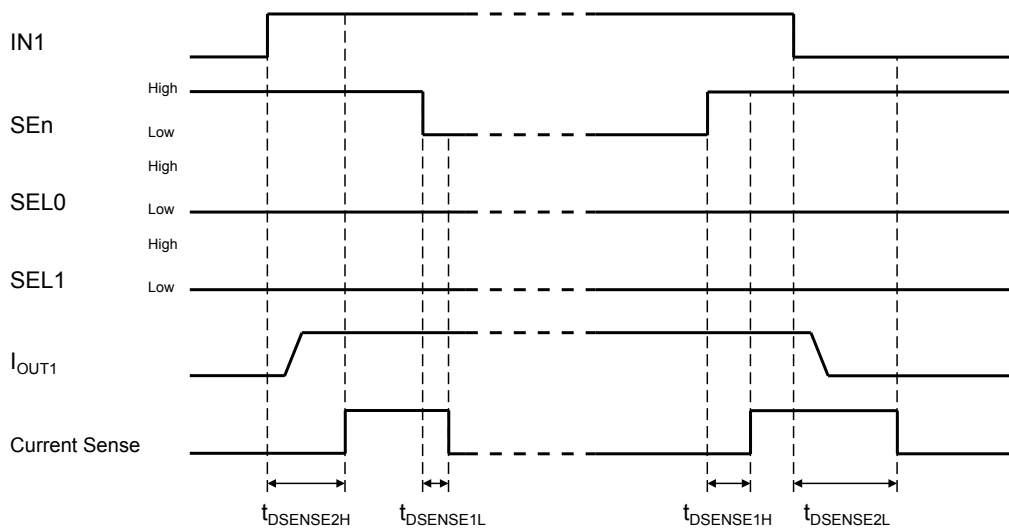
GADG0903171216PS

Figure 6. Switching times and Pulse skew



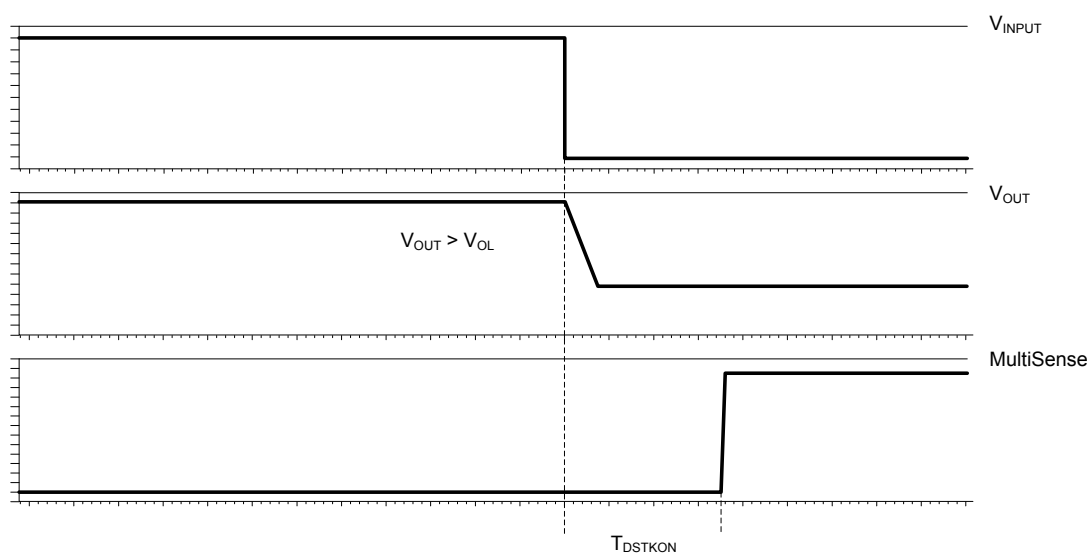
GAPGCFT00797

Figure 7. Current sense timings (current sense mode)



GADG0704171311PS

Figure 8. T_{DSKON}



GAPG2609141140CFT

Table 11. Truth table

Mode	Conditions	IN _X	FR	SEn	SEL _X	OUT _X	Current sense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T _j < 150°C	L	X	See ⁽¹⁾		L	See ⁽¹⁾	
		H	L			H	See ⁽¹⁾	Outputs configured for auto-restart
		H	H			H	See ⁽¹⁾	Outputs configured for Latch-off
Overload	Overload or short to GND causing: T _j > T _{TSD} or ΔT _j > ΔT _{j,SD}	L	X	See ⁽¹⁾		L	See ⁽¹⁾	
		H	L			H	See ⁽¹⁾	Output cycles with temperature hysteresis
		H	H			L	See ⁽¹⁾	Output latches-off
Under-voltage	V _{CC} < V _{USD} (falling)	X	X	X	X	L	Hi-Z	Re-start when V _{CC} > V _{USD} + V _{USDhyst} (rising)
						L	Hi-Z	
OFF-state diagnostics	Short to V _{CC}	L	X	See ⁽¹⁾		H	See ⁽¹⁾	
	Open-load	L	X			H	See ⁽¹⁾	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See ⁽¹⁾		< 0 V	See ⁽¹⁾	

1. Refer to Table 12. Current sense multiplexer addressing

Table 12. Current sense multiplexer addressing

SEn	SEL ₁	SEL ₀	MUX channel	Current sense output			
				Nomal mode	Overload	OFF-state diag. ^{(1) (2) (3)}	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	I _{SENSE} = 1/ K * I _{OUT0}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	L	H	Channel 1 diagnostic	I _{SENSE} = 1/ K * I _{OUT1}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	H	L	Channel 2 diagnostic	I _{SENSE} = 1/ K * I _{OUT2}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	H	H	Channel 3 diagnostic	I _{SENSE} = 1/ K * I _{OUT3}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z

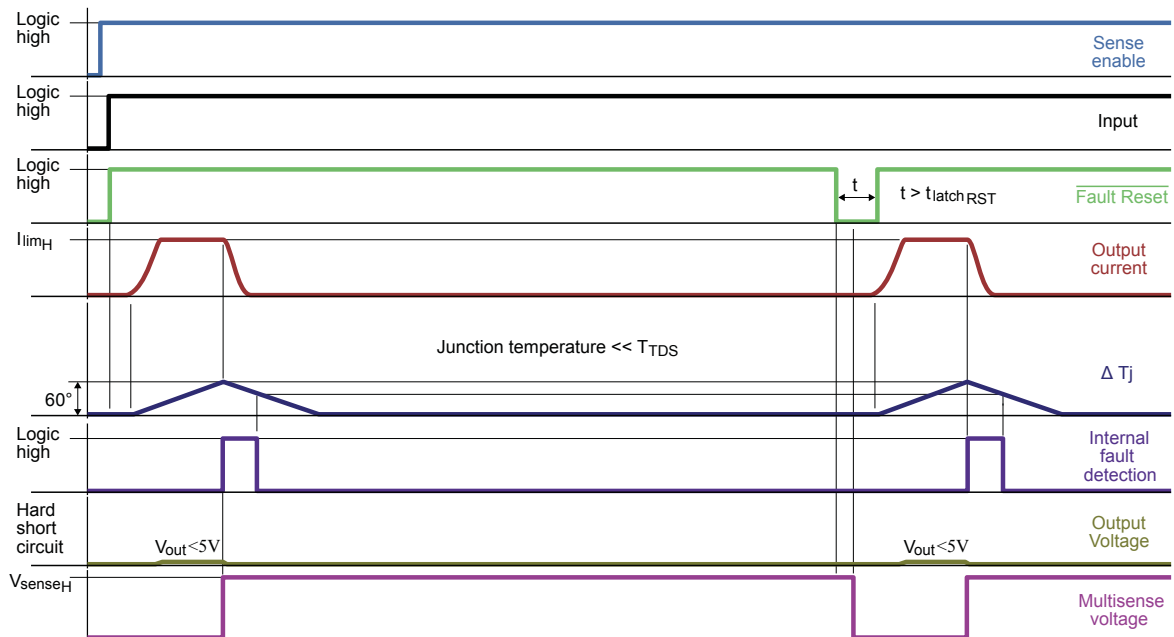
1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, CS pin delivers feedback according to OFF-State diagnostic.

2. Example 1: FR = 1; IN₀ = 0; OUT₀ = L (latched); MUX channel = channel 0 diagnostic; CS = 0

3. Example 2: FR = 1; IN₀ = 0; OUT₀ = latched, V_{OUT0} > V_{OL}; MUX channel = channel 0 diagnostic; CS = V_{SENSEH}

2.4 Waveforms

Figure 9. Latch functionality - behavior in hard short-circuit condition ($T_{AMB} \ll T_{TSD}$)



GADG1703171451PS

Figure 10. Latch functionality - behavior in hard short-circuit condition

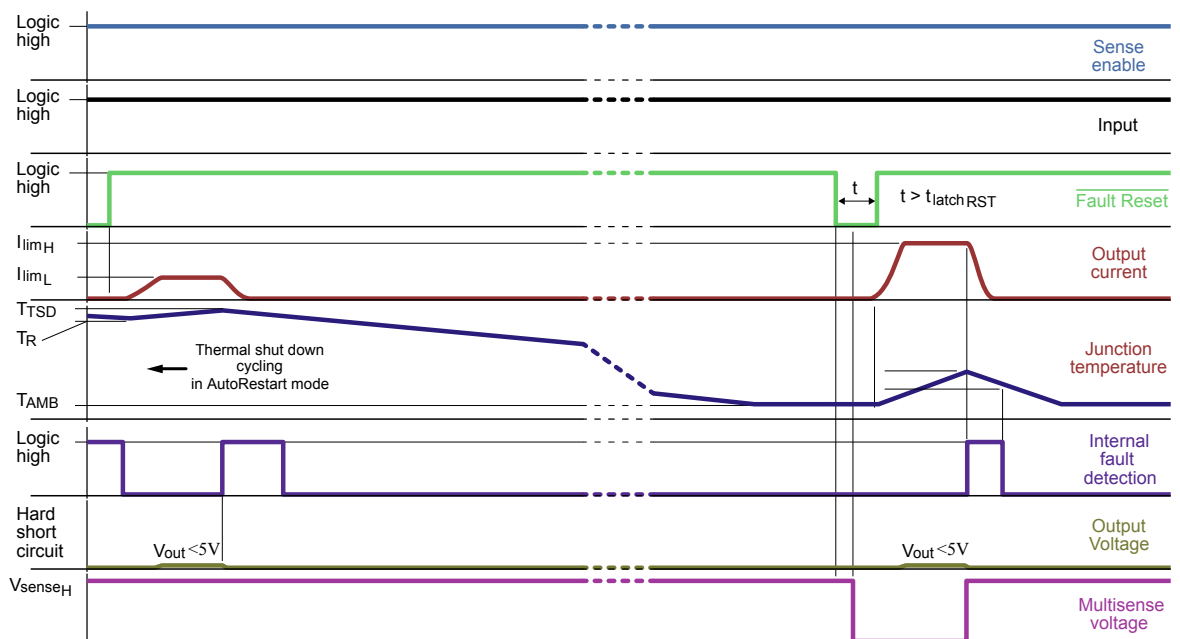
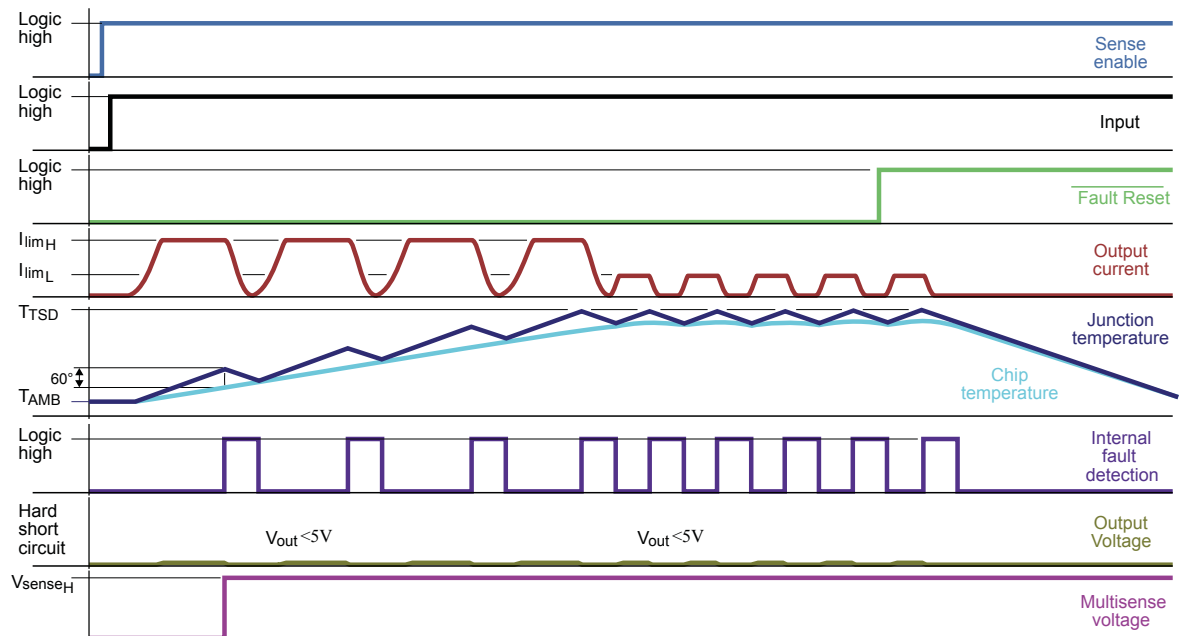
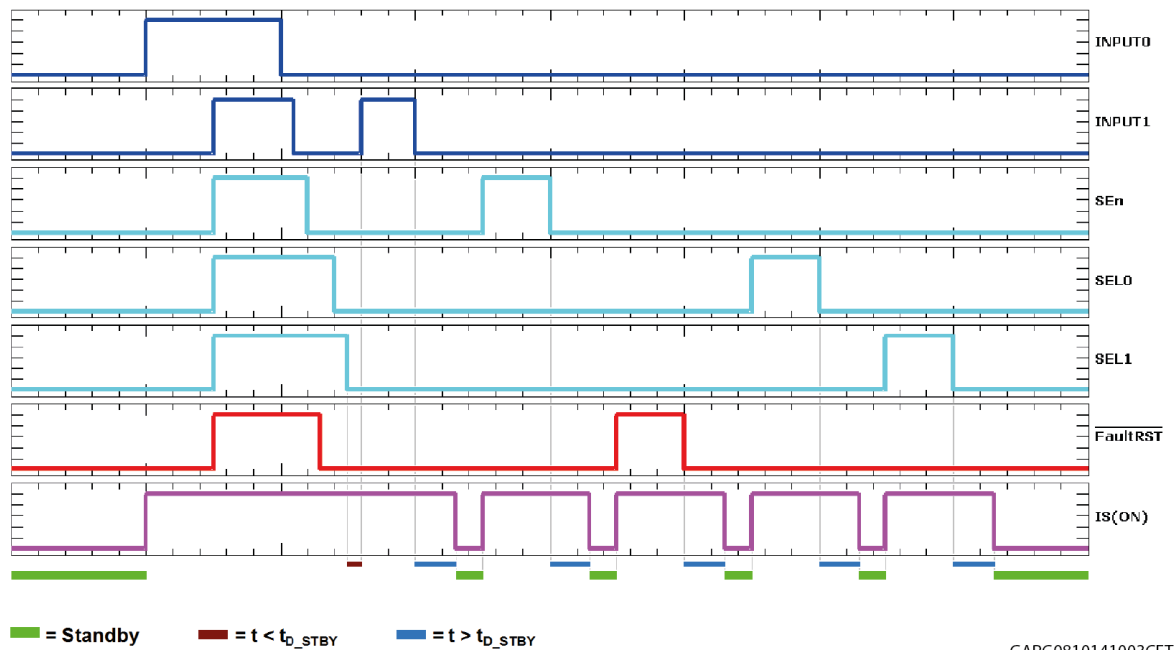


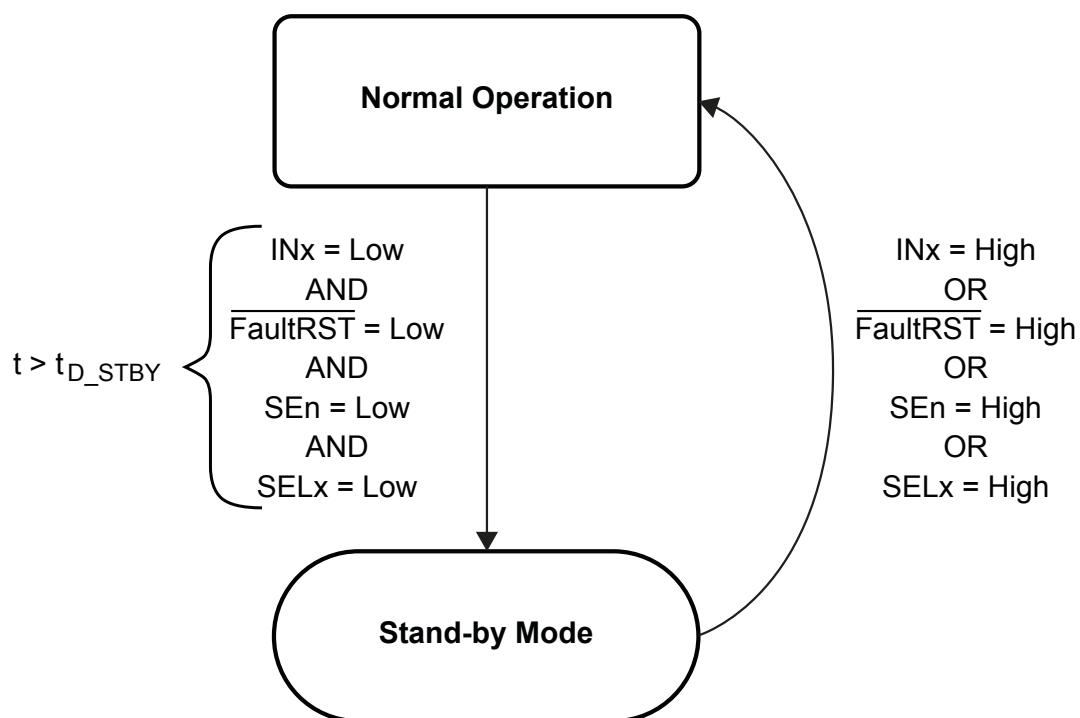
Figure 11. Latch functionality - behavior in hard short-circuit condition (autorestart mode + latch off)


GADG2103171742PS

Figure 12. Standby mode activation


GAPG0810141003CFT

Figure 13. Standby state diagram



GAPGCFT00598

2.5 Electrical characteristics curves

Figure 14. OFF-state output current

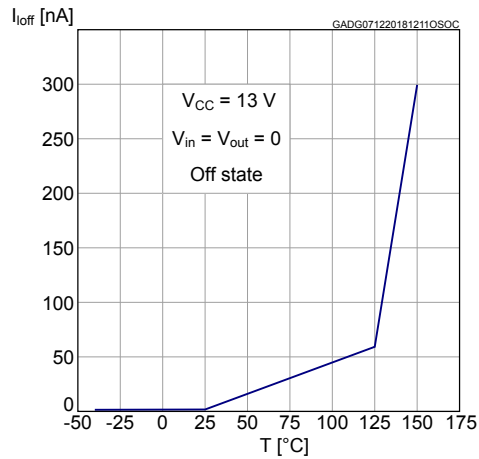


Figure 15. Standby current

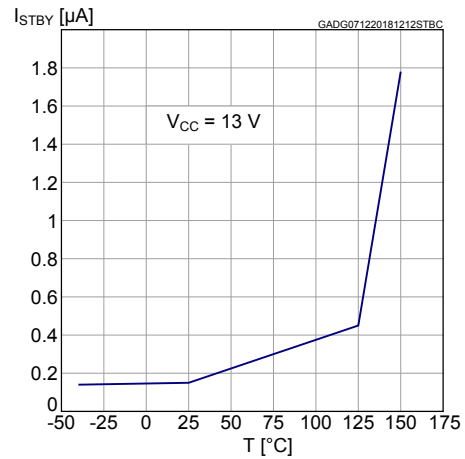


Figure 16. $I_{GND(ON)}$ vs. I_{out}

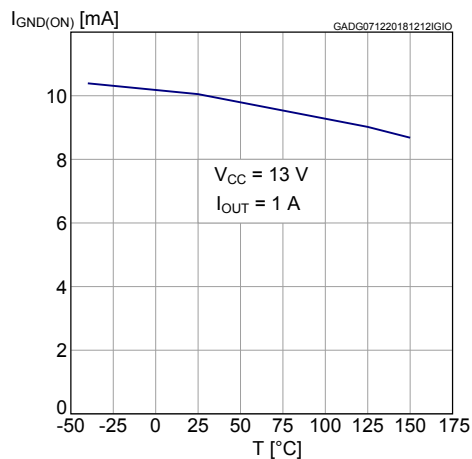


Figure 17. Logic input high level voltage

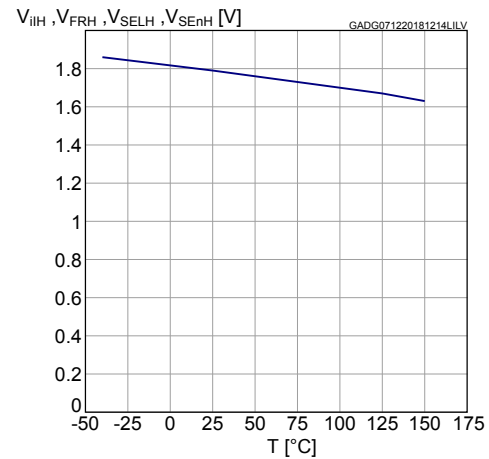


Figure 18. Logic input low level voltage

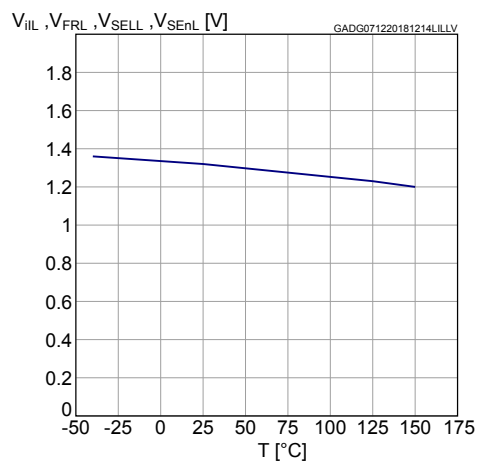


Figure 19. High level logic input current

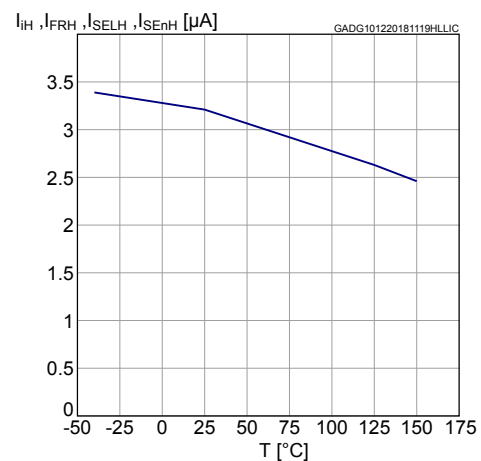


Figure 20. Low level logic input current

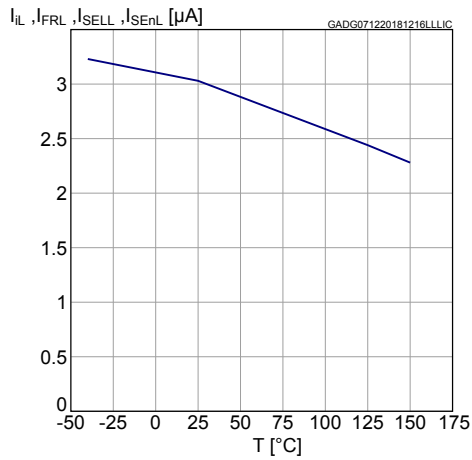


Figure 21. Logic input hysteresis voltage

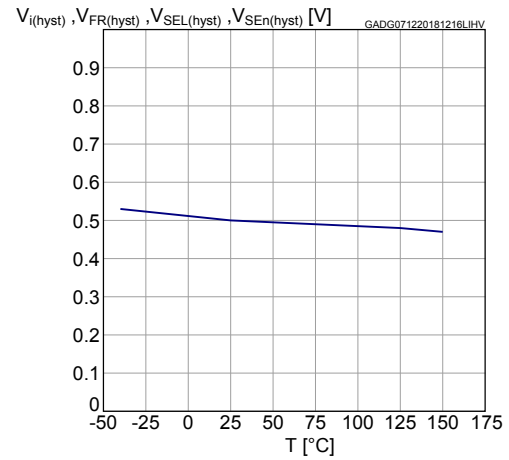


Figure 22. FaultRST Input clamp voltage

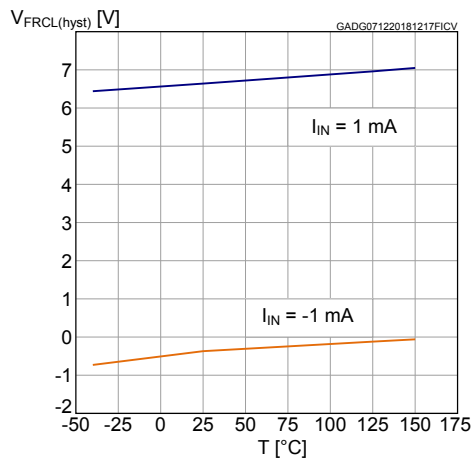


Figure 23. Undervoltage shutdown

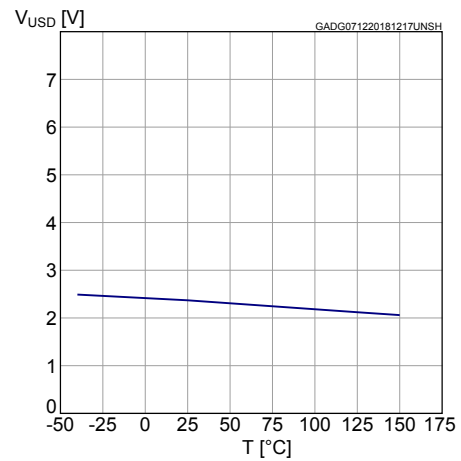


Figure 24. On-state resistance vs. T_{case}

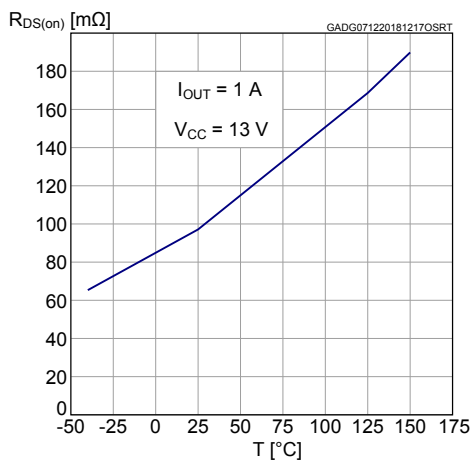


Figure 25. On-state resistance vs. V_{CC}

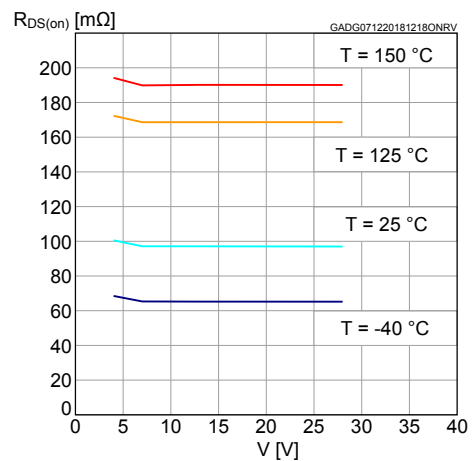


Figure 26. Turn-on voltage slope

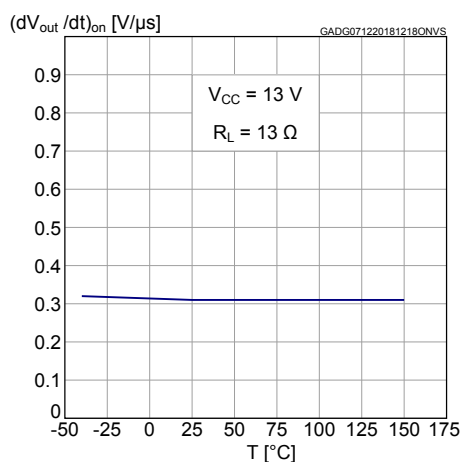


Figure 27. Turn-off voltage slope

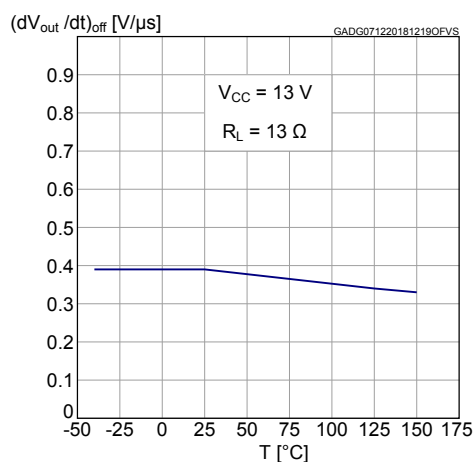


Figure 28. W_{on} vs. T_{case}

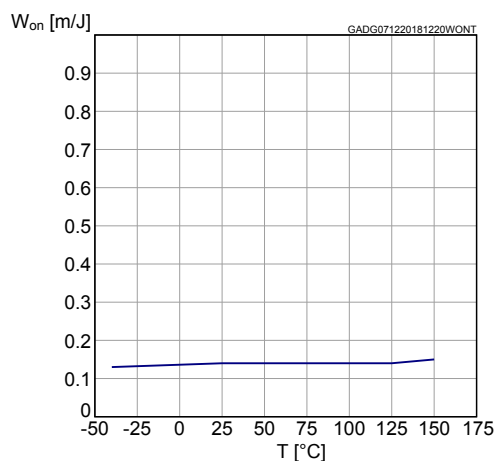


Figure 29. W_{off} vs. T_{case}

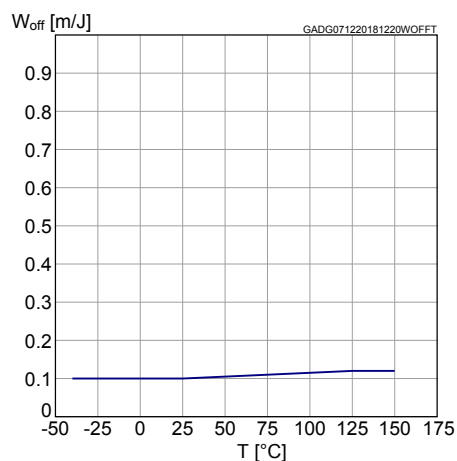


Figure 30. OFF-state open-load voltage detection threshold

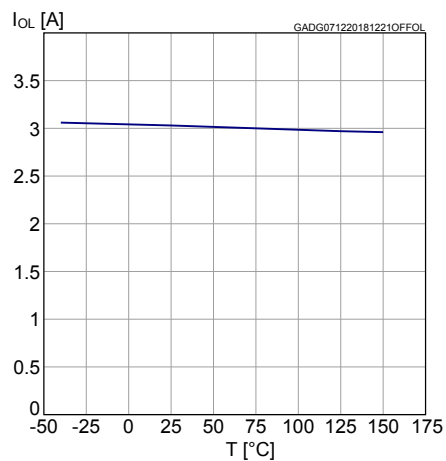


Figure 31. V_{SENSE_CL} vs. T_{case}

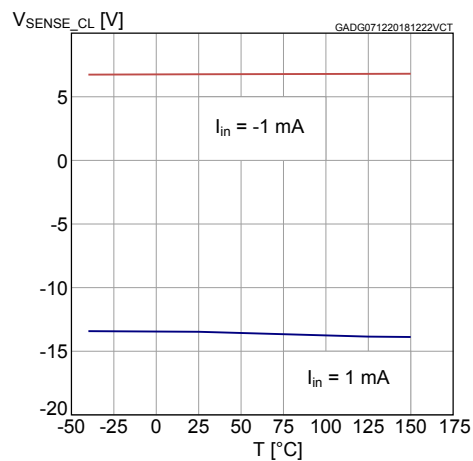
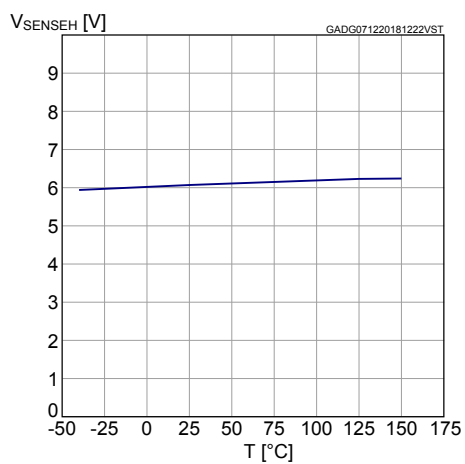


Figure 32. V_{SENSEH} vs. T_{case}



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($\overline{\text{FaultRST}} = \text{Low}$) or remains off ($\overline{\text{FaultRST}} = \text{High}$). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($\overline{\text{FaultRST}} = \text{Low}$) or remains off ($\overline{\text{FaultRST}} = \text{High}$).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

4 Application information

Figure 33. Application diagram

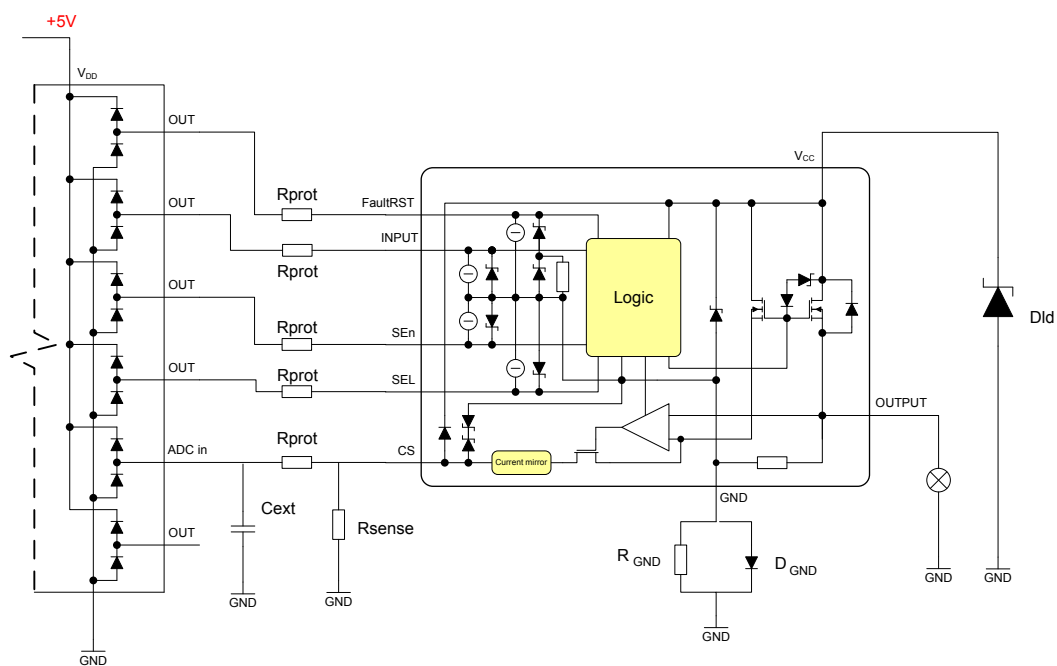


Table 13. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_S^{(1)}$		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a ⁽³⁾	III	+55 V	500 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4 ⁽²⁾	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		40 V	5 pulse	1 min		400 ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 40 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

4.3

MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$V_{CC\text{peak}}/I_{\text{latchup}} \leq R_{\text{prot}} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IH\text{max}}$$

Calculation example:

For $V_{CC\text{peak}} = -150\text{ V}$; $I_{\text{latchup}} \geq 20\text{ mA}$; $V_{OH\mu C} \geq 4.5\text{ V}$

$$7.5\text{ k}\Omega \leq R_{\text{prot}} \leq 140\text{ k}\Omega.$$

Recommended values: $R_{\text{prot}} = 15\text{ k}\Omega$

4.4

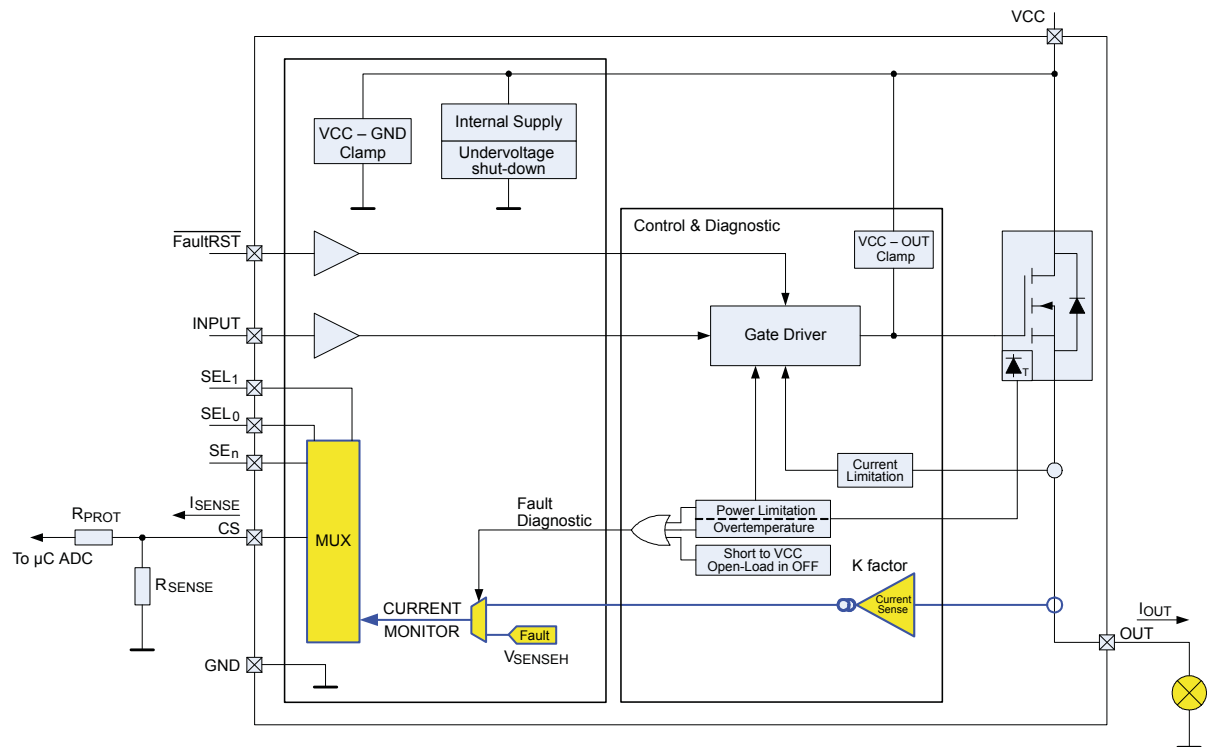
CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

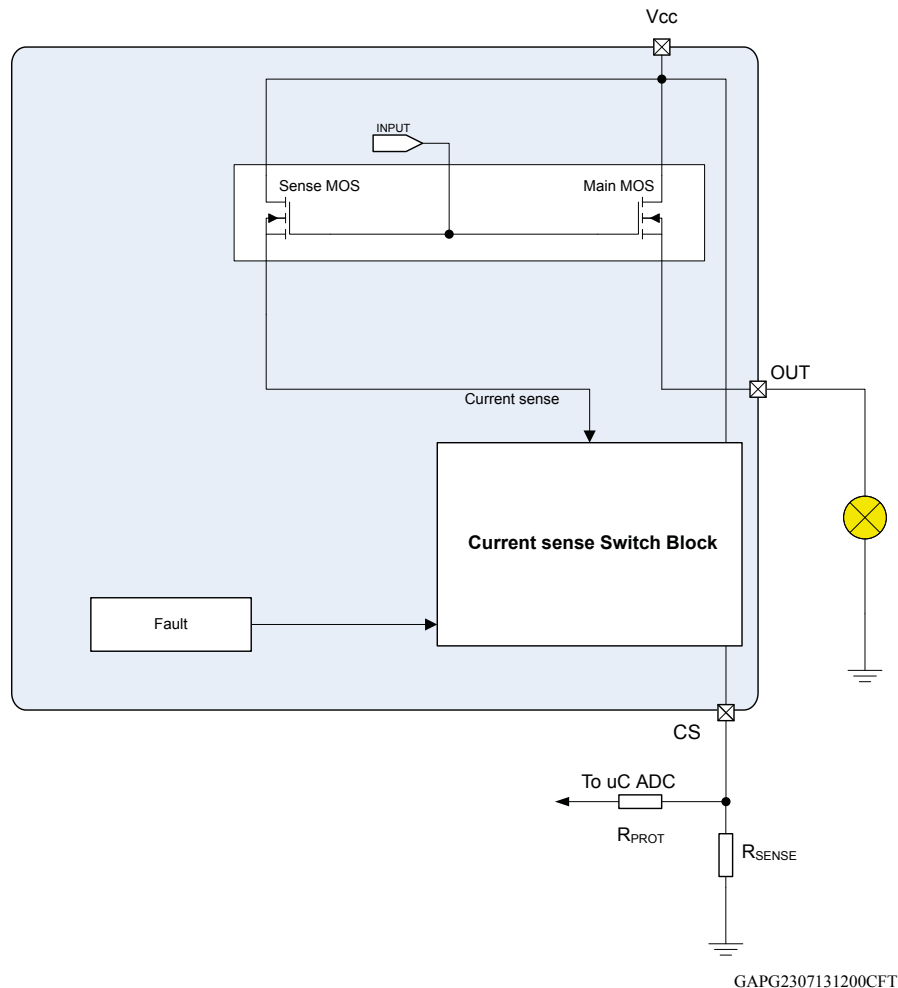
Figure 35. CurrentSense and diagnostic – block diagram



GADG2004171456PS

4.4.1 Principle of CurrentSense signal generation

Figure 36. CurrentSense block diagram



Current sense

The output is able to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CS output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor

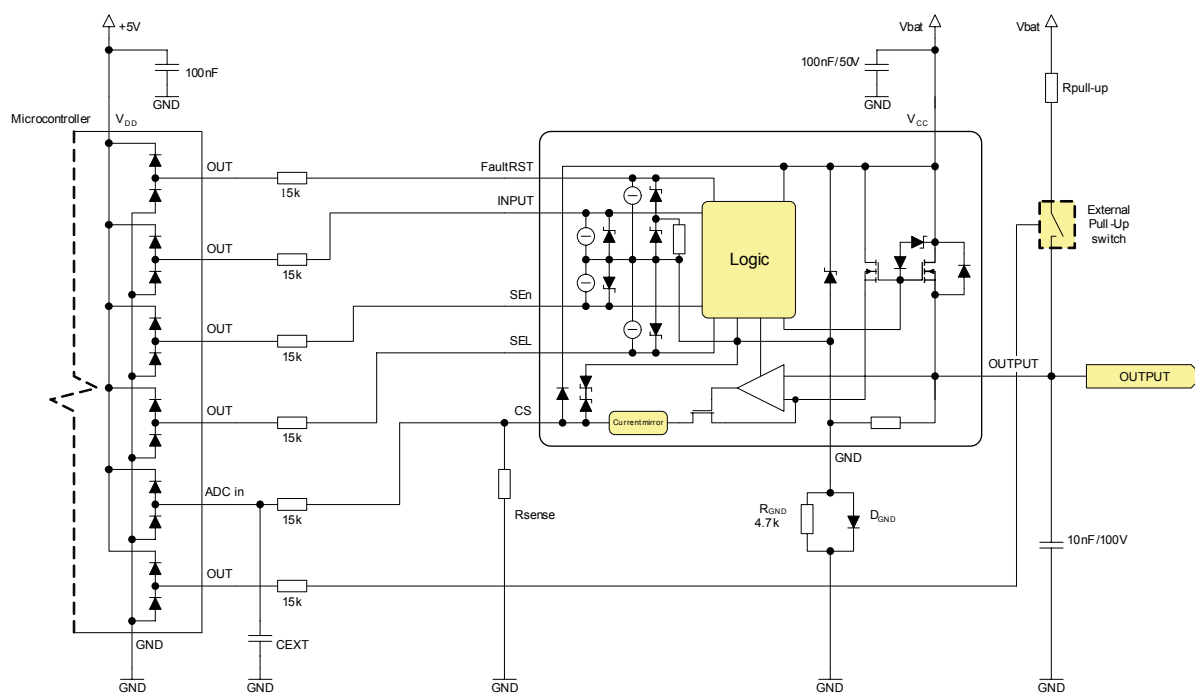
- I_{SENSE} is the current provided from CS pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of the overall circuitry, specifying the ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source, V_{SENSEH} .

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH} .

Figure 37. Analog HSD – open-load detection in off-state



GAPG1201151432CFT

Figure 38. Open-load / short to V_{CC} condition

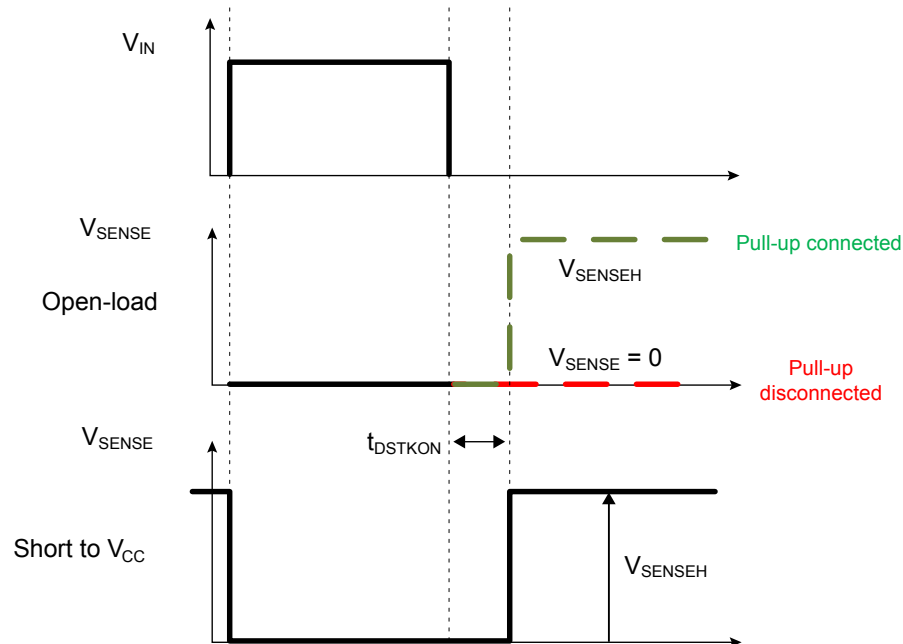


Table 14. CurrentSense pin levels in off-state

Condition	Output	CS	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

5 Maximum demagnetization energy ($V_{CC} = 16\text{ V}$)

Figure 40. Maximum turn off current versus inductance

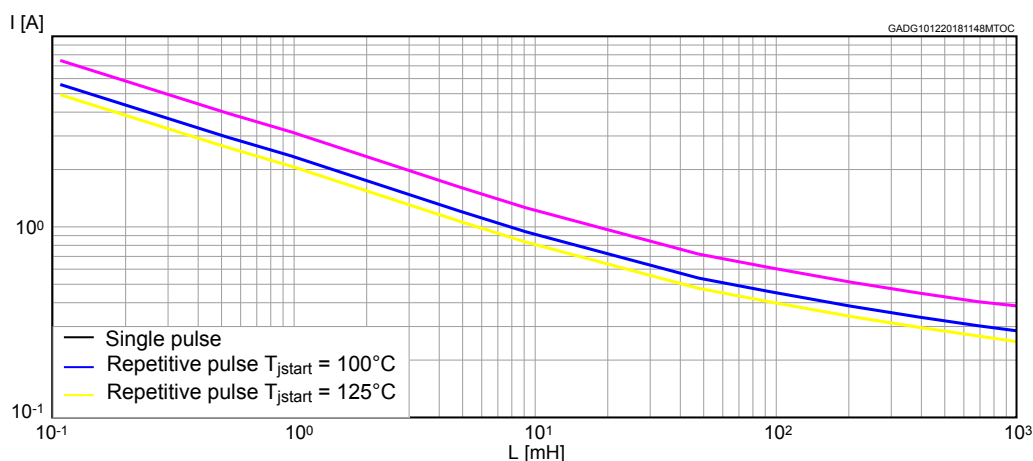
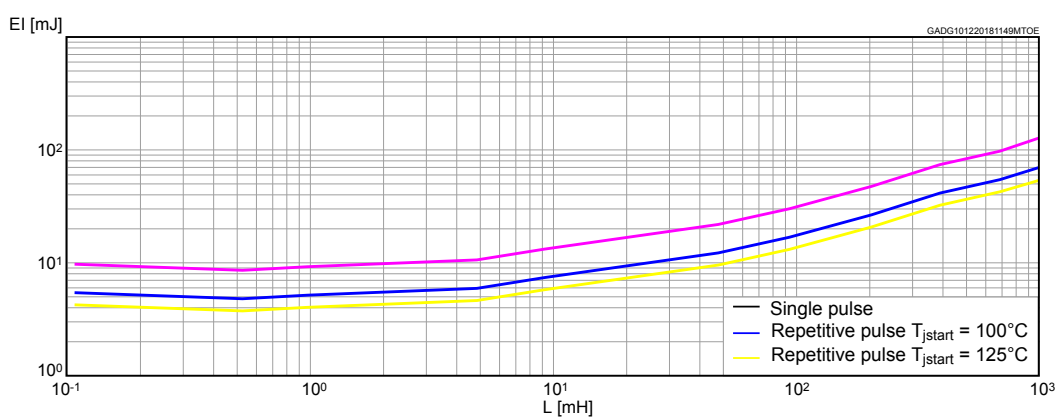


Figure 41. Maximum turn off energy versus inductance



Note: Values are generated with $R_L = 0\ \Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 42. PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)

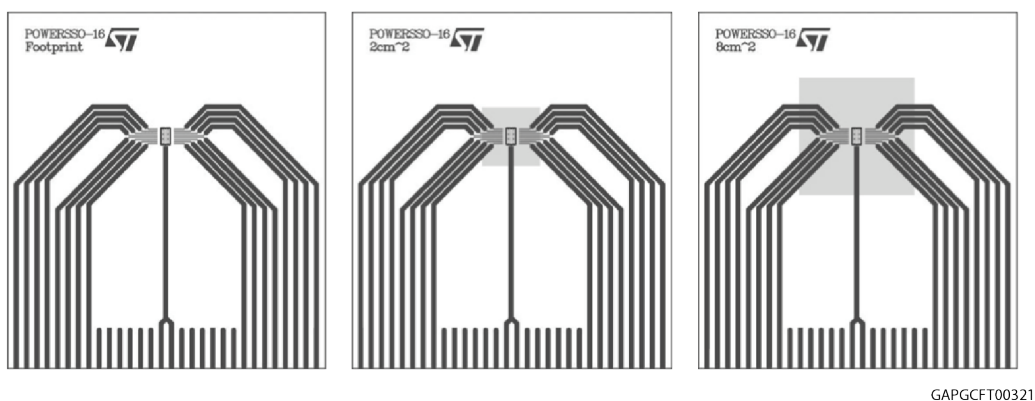


Figure 43. PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)

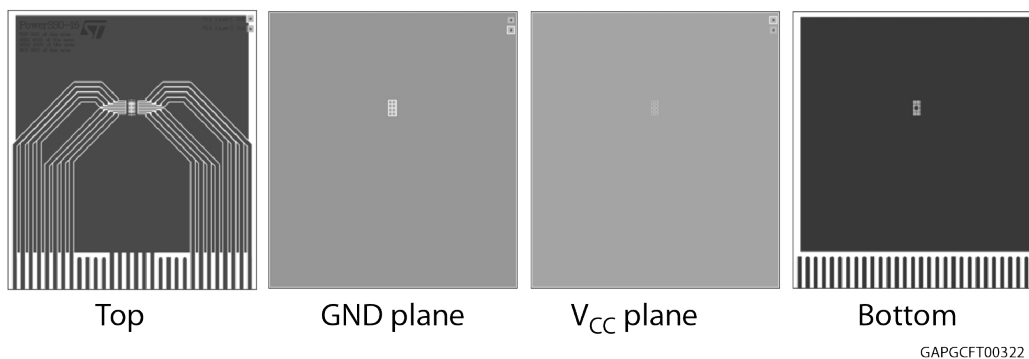
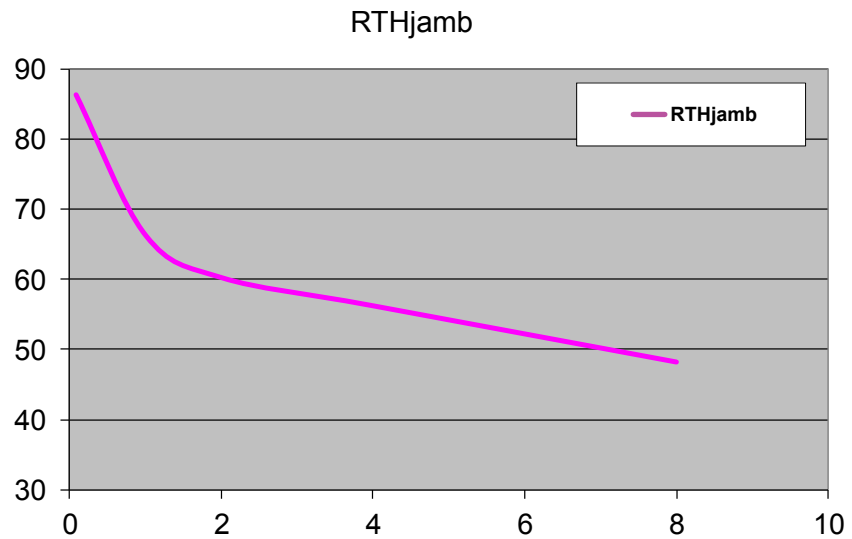


Table 15. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm

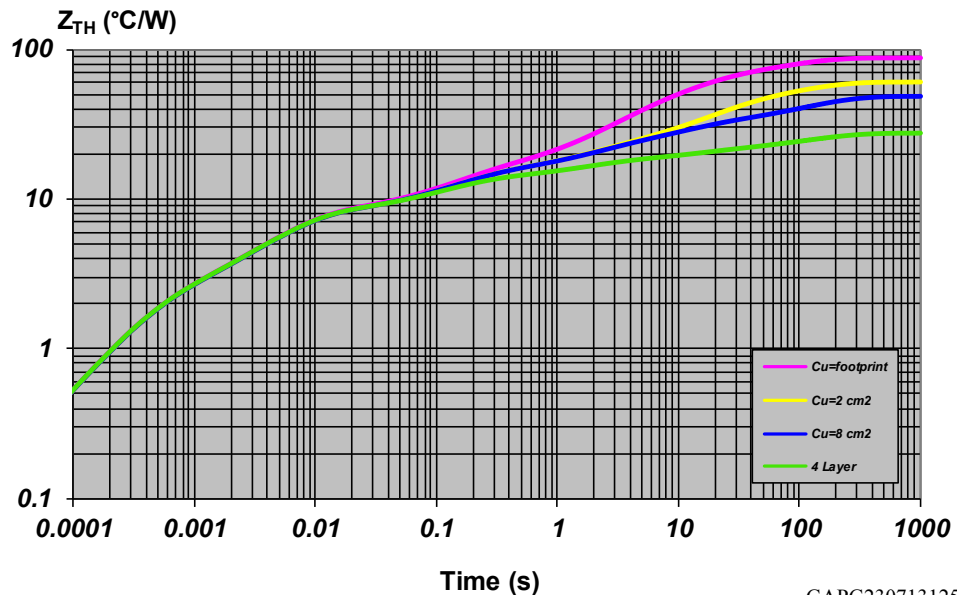
Dimension	Value
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

Figure 44. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)



GAPG2307131254CFT

Figure 45. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)

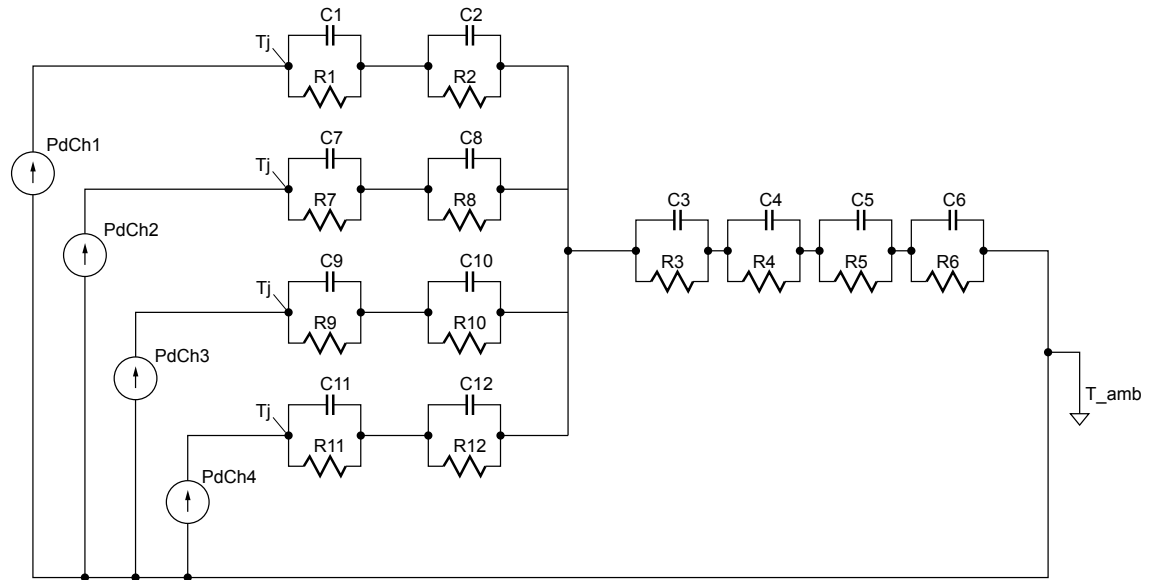


GAPG2307131257CFT

Equation: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 46. Thermal fitting model of a double-channel HSD in PowerSSO-16


GADG2203171318PS

Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. Thermal parameters

Area/island (cm ²)	Footprint	2	8	4L
R1, R7 (°C/W)	1.75			
R2, R8 (°C/W)	6			
R3 (°C/W)	6.6	6.6	6.6	5.4
R4 (°C/W)	16	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1, C7 (W.s/°C)	0.0002			
C2, C8 (W.s/°C)	0.0009			
C3 (W.s/°C)	0.023			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 PowerSSO-16 package information

Figure 47. PowerSSO-16 package dimensions

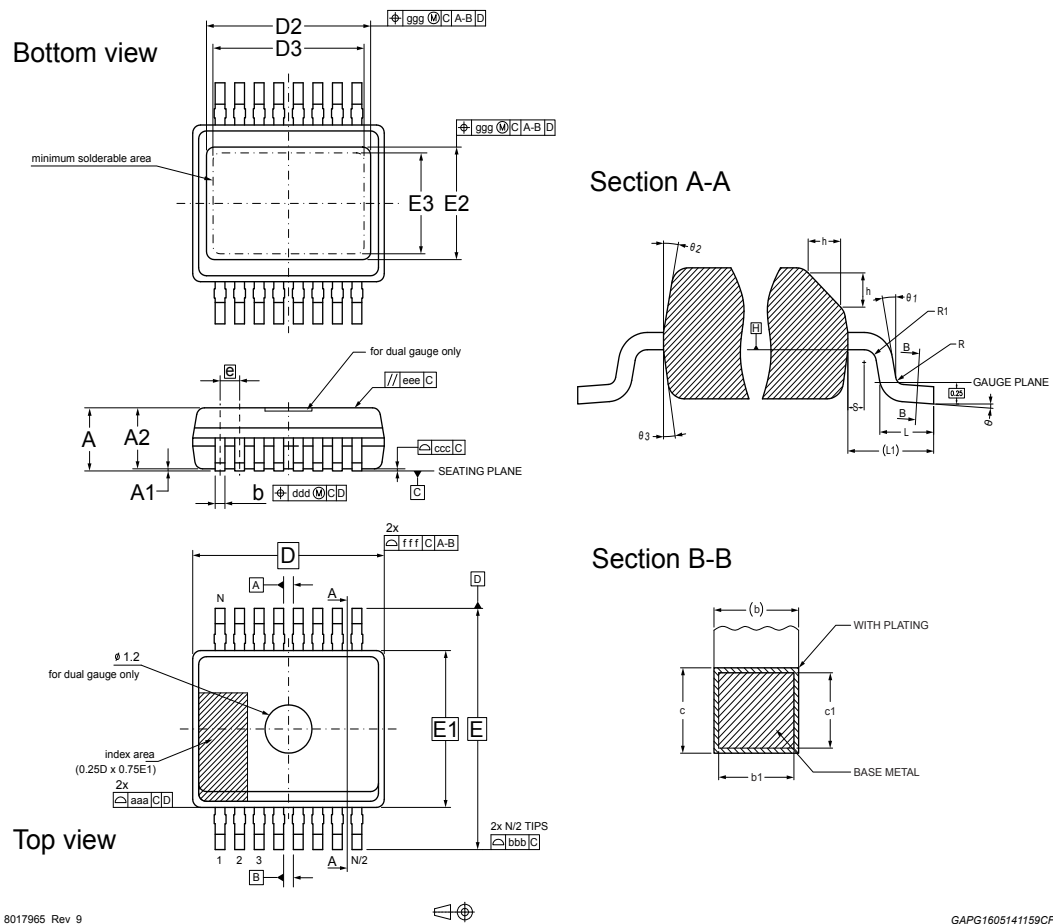
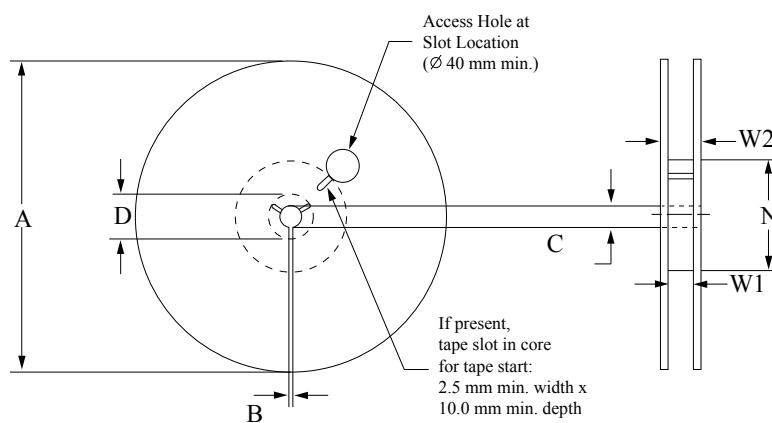


Table 17. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
$\Theta 1$	0°		
$\Theta 2$	5°		15°
$\Theta 3$	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.90 BSC		
D2	3.31		3.91
D3	2.61		
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.20		2.80
E3	1.49		
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

7.2 PowerSSO-16 packing information

Figure 48. PowerSSO-16 reel 13"



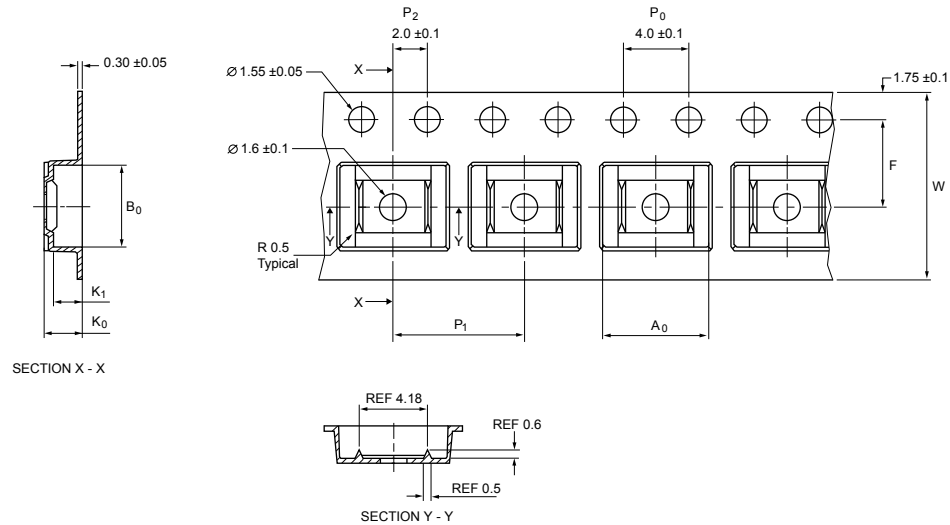
TAPG2004151655CFT

Table 18. Reel dimensions

Description	Value ⁽¹⁾
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. All dimensions are in mm.

Figure 49. PowerSSO-16 carrier tape



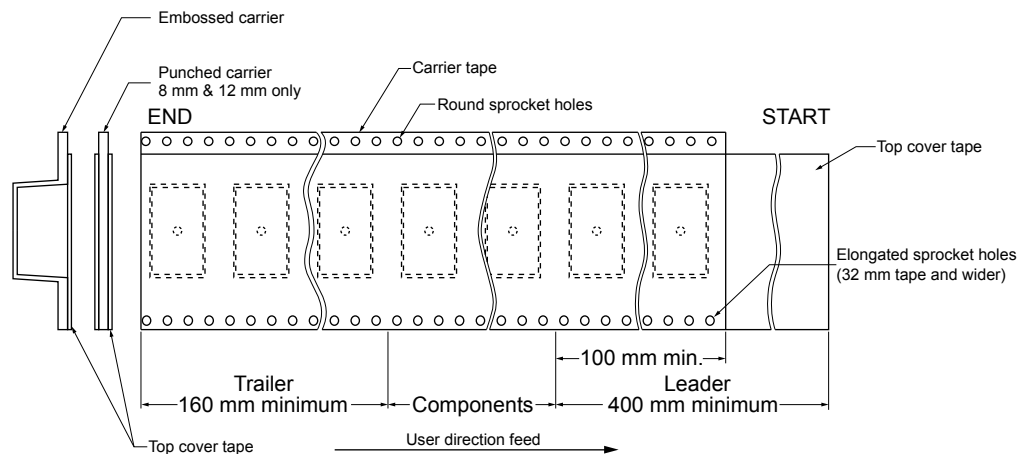
GAPG2204151242CFT

Table 19. PowerSSO-16 carrier tape dimensions

Description	Value ⁽¹⁾
A ₀	6.50 ± 0.1
B ₀	5.25 ± 0.1
K ₀	2.10 ± 0.1
K ₁	1.80 ± 0.1
F	5.50 ± 0.1
P ₁	8.00 ± 0.1
W	12.00 ± 0.3

1. All dimensions are in mm.

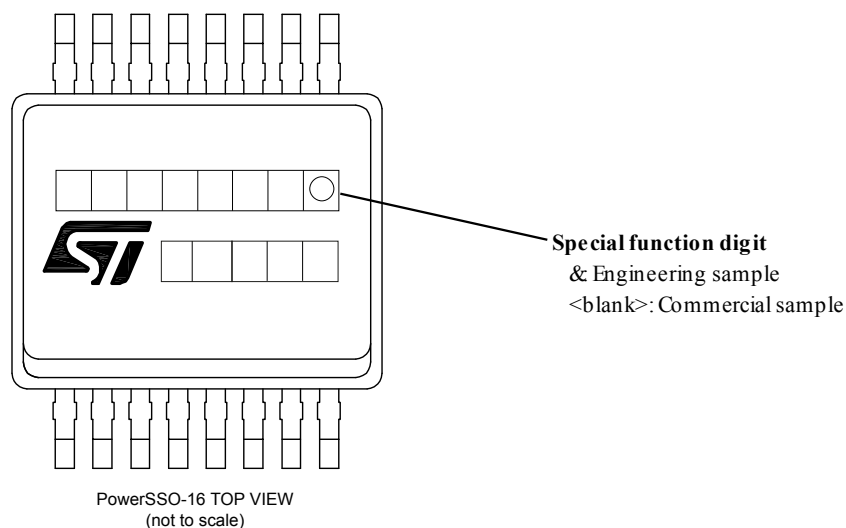
Figure 50. PowerSSO-16 schematic drawing of leader and trailer tape



GAPG2004151511CFT

7.3 PowerSSO-16 marking information

Figure 51. PowerSSO-16 marking information



GADG0310161234SMD

Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 20. Document revision history

Date	Version	Changes
08-June-2018	1	Initial release.
08-Jan-2019	2	Updated features and application in cover page. Updated Table 4. Thermal data , Section 2.3 Main electrical characteristics , Figure 12. Standby mode activation . Inserted Section 2.5 Electrical characteristics curves , Section 5 Maximum demagnetization energy (V_{CC} = 16 V) and Section 6 Package and PCB thermal data . Minor text changes.
18-Feb-2019	3	Updated Figure 44 and Figure 45 .

Contents

1	Block diagram and pin description	3
2	Electrical specification	5
2.1	Absolute maximum ratings	5
2.2	Thermal data	6
2.3	Main electrical characteristics	7
2.4	Waveforms	15
2.5	Electrical characteristics curves	19
3	Protections	23
3.1	Power limitation	23
3.2	Thermal shutdown	23
3.3	Current limitation	23
3.4	Negative voltage clamp	23
4	Application information	24
4.1	GND protection network against reverse battery	24
4.1.1	Diode (DGND) in the ground line	25
4.2	Immunity against transient electrical disturbances	25
4.3	MCU I/Os protection	26
4.4	CS - analog current sense	26
4.4.1	Principle of CurrentSense signal generation	27
4.4.2	Short to VCC and OFF-state open-load detection	30
5	Maximum demagnetization energy (VCC = 16 V)	32
6	Package and PCB thermal data	33
6.1	PowerSSO-16 thermal data	33
7	Package information	36
7.1	PowerSSO-16 package information	36
7.2	PowerSSO-16 packing information	37
7.3	PowerSSO-16 marking information	39
	Revision history	41

List of tables

Table 1.	Pin functions	3
Table 2.	Suggested connections for unused and not connected pins	4
Table 3.	Absolute maximum ratings	5
Table 4.	Thermal data	6
Table 5.	Electrical characteristics during cranking	7
Table 6.	Power section	7
Table 7.	Switching	8
Table 8.	Logic Inputs	8
Table 9.	Protections	9
Table 10.	CurrentSense	10
Table 11.	Truth table	15
Table 12.	Current sense multiplexer addressing	15
Table 13.	ISO 7637-2 - electrical transient conduction along supply line	26
Table 14.	CurrentSense pin levels in off-state	30
Table 15.	PCB properties	33
Table 16.	Thermal parameters	35
Table 17.	PowerSSO-16 mechanical data	37
Table 18.	Reel dimensions	38
Table 19.	PowerSSO-16 carrier tape dimensions	39
Table 20.	Document revision history	41

List of figures

Figure 1.	Block diagram	3
Figure 2.	Configuration diagram (top view).	4
Figure 3.	Current and voltage conventions.	5
Figure 4.	I_{OUT}/I_{SENSE} versus I_{OUT}	12
Figure 5.	Current sense accuracy versus I_{OUT}	13
Figure 6.	Switching times and Pulse skew	13
Figure 7.	Current sense timings (current sense mode).	14
Figure 8.	T_{DSKON}	14
Figure 9.	Latch functionality - behavior in hard short-circuit condition ($T_{AMB} << T_{TSD}$)	16
Figure 10.	Latch functionality - behavior in hard short-circuit condition.	16
Figure 11.	Latch functionality - behavior in hard short-circuit condition (autorestart mode + latch off).	17
Figure 12.	Standby mode activation	17
Figure 13.	Standby state diagram.	18
Figure 14.	OFF-state output current	19
Figure 15.	Standby current	19
Figure 16.	$I_{GND(ON)}$ vs. I_{out}	19
Figure 17.	Logic input high level voltage	19
Figure 18.	Logic input low level voltage.	19
Figure 19.	High level logic input current.	19
Figure 20.	Low level logic input current	20
Figure 21.	Logic input hysteresis voltage.	20
Figure 22.	FaultRST Input clamp voltage.	20
Figure 23.	Undervoltage shutdown	20
Figure 24.	On-state resistance vs. T_{case}	20
Figure 25.	On-state resistance vs. V_{CC}	20
Figure 26.	Turn-on voltage slope	21
Figure 27.	Turn-off voltage slope	21
Figure 28.	W_{on} vs. T_{case}	21
Figure 29.	W_{off} vs. T_{case}	21
Figure 30.	OFF-state open-load voltage detection threshold	21
Figure 31.	V_{SENSE} clamp vs. T_{case}	21
Figure 32.	V_{SENSEH} vs. T_{case}	22
Figure 33.	Application diagram.	24
Figure 34.	Simplified internal structure	25
Figure 35.	CurrentSense and diagnostic – block diagram	27
Figure 36.	CurrentSense block diagram	28
Figure 37.	Analog HSD – open-load detection in off-state	29
Figure 38.	Open-load / short to V_{CC} condition	30
Figure 40.	Maximum turn off current versus inductance.	32
Figure 41.	Maximum turn off energy versus inductance.	32
Figure 42.	PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)	33
Figure 43.	PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)	33
Figure 44.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)	34
Figure 45.	PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)	34
Figure 46.	Thermal fitting model of a double-channel HSD in PowerSSO-16	35
Figure 47.	PowerSSO-16 package dimensions	36
Figure 48.	PowerSSO-16 reel 13"	38
Figure 49.	PowerSSO-16 carrier tape	39
Figure 50.	PowerSSO-16 schematic drawing of leader and trailer tape	39
Figure 51.	PowerSSO-16 marking information	40

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved