Microchip

28C16A

16K (2K x 8) CMOS Electrically Erasable PROM

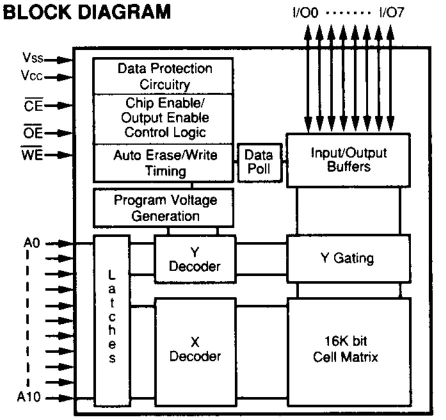
FEATURES

- Fast Read Access Time—150ns
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- Data polling
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - —24-pin Dual-In-Line Package
  - —32-pin Chip Carrier (Leadless or Plastic)
  - —28-pin Thin Small Outline Package (TSOP)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C

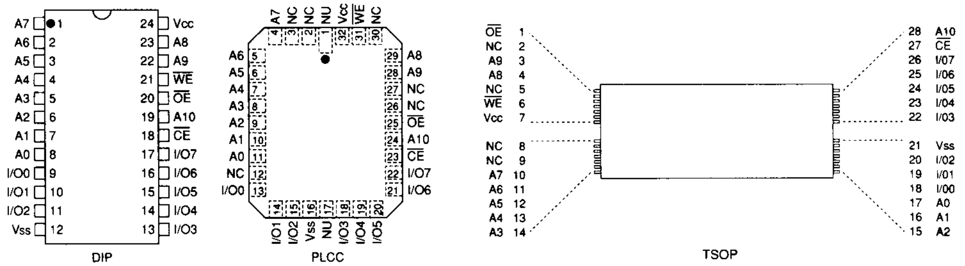
DESCRIPTION

The Microchip Technology Inc 28C16A is a CMOS 16K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses Data polling. Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

BLOCK DIAGRAM



PIN CONFIGURATION



DIP PLCC TSOP

●Pin 1 indicator on PLCC on top of package

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss ....-0.6V to + 6.25V
Voltage on $\overline{\text{OE}}$ w.r.t. Vss ....-0.6V to +13.5V
Voltage on A9 w.r.t. Vss ....-0.6V to +13.5V
Output Voltage w.r.t. Vss ....-0.6V to Vcc+0.6V
Storage temperature ....-65° C to 125° C
Ambient temp. with power applied........-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Supply Current, Active	TTL input	Icc		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{\text{CE}}$ = VIH (0° C to 70° C) $\overline{\text{CE}}$ = VIH (-40° C to 85° C) $\overline{\text{CE}}$ = Vcc-0.3 to Vcc+1

Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

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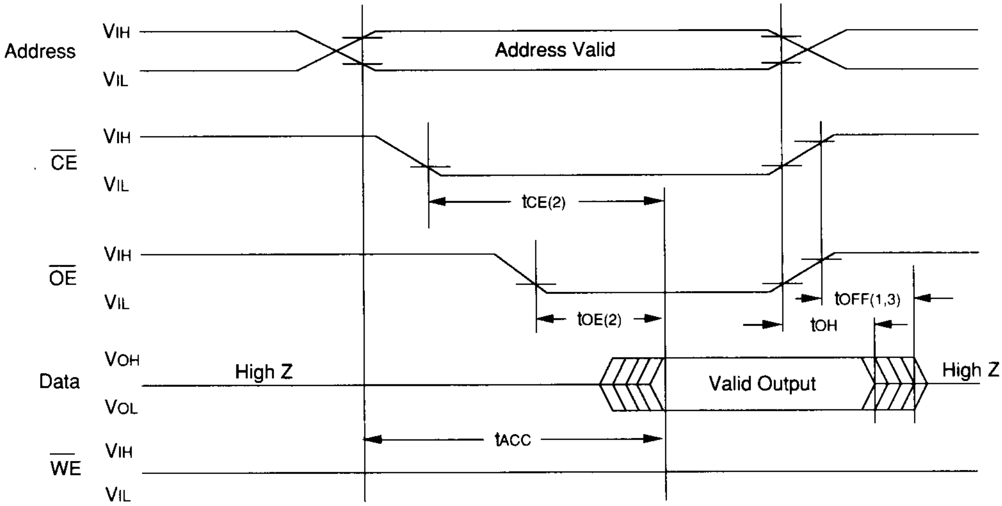
READ OPERATION
AC Characteristics

AC Testing Waveform: $V_{IH} = 2.4V$; $V_{IL} = 0.45V$; $V_{OH} = 2.0V$; $V_{OL} = 0.8V$
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Sym	28C16A-15		28C16A-20		28C16A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE} = \overline{CE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

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BYTE WRITE AC Characteristics

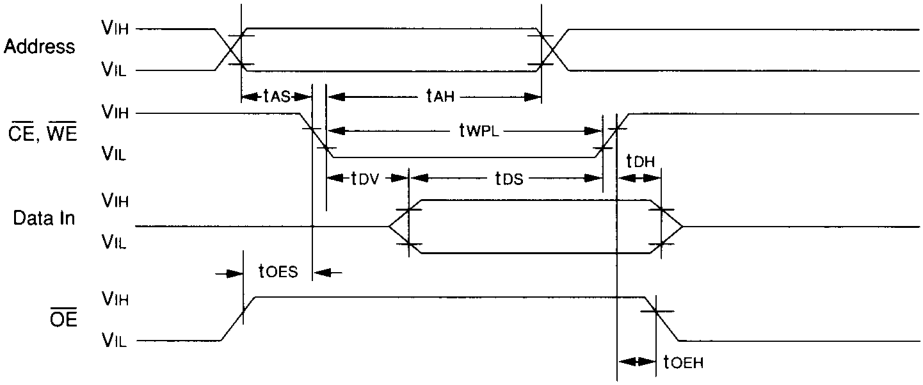
AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$; $V_{OH} = 2.0V$; $V_{OL} = 0.8V$
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C16A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	t_{WC}		200	µs	100µs typical

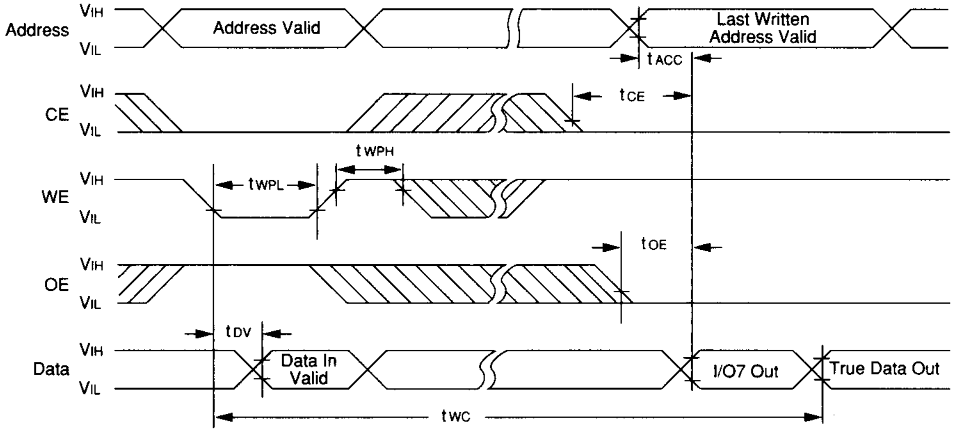
Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.

(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of WE or CE, whichever occurs first.

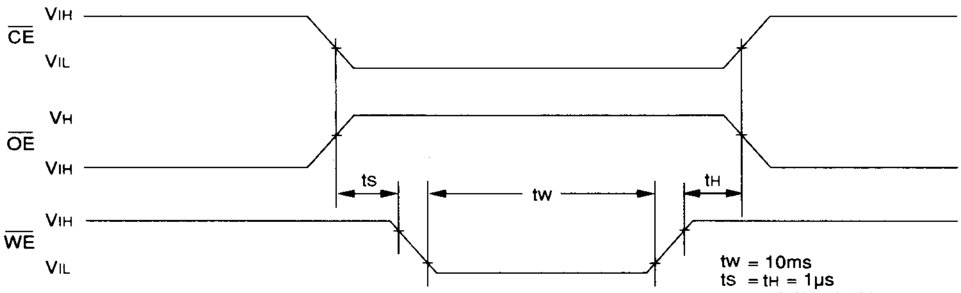
PROGRAMMING Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



t_W = 10ms
t_S = t_H = 1µs
V_H = 12.0V ±0.5V

SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Chip Clear	V_{IL}	V_H	V_{IL}	X	V_{CC}	
Extra Row Read	V_{IL}	V_{IL}	V_{IH}	A9 = V_H	V_{CC}	Data Out
Extra Row Write	*	V_{IH}	*	A9 = V_H	V_{CC}	Data In

Note: V_H = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

$\overline{\text{Data}}$ Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7E0 to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

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NOTES:

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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C16AF T - 15 I / P

Package:	J	Cerdip
	L	Plastic Leaded Chip Carrier (PLCC))
	P	Plastic DIP
	TS	Thin Small Outline Package (TSOP)
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
Access Time:	15	150 nsec
	20	200 nsec
	25	250 nsec
Shipping:	Blank	Tube
	T	Tape and Reel "L" only
Option:	-	= twc = 1ms
	F	= twc = 200µs
Device:	28C16A	2K x 8 CMOS EEPROM