

## ADC108S052 8-Channel, 200 ksps to 500 ksps, 10-Bit A/D Converter

Check for Samples: [ADC108S052](#)

### FEATURES

- Eight Input Channels
- Variable Power Management
- Independent Analog and Digital Supplies
- SPI™/ QSPI™/MICROWIRE/DSP Compatible
- Packaged in 16-Lead TSSOP

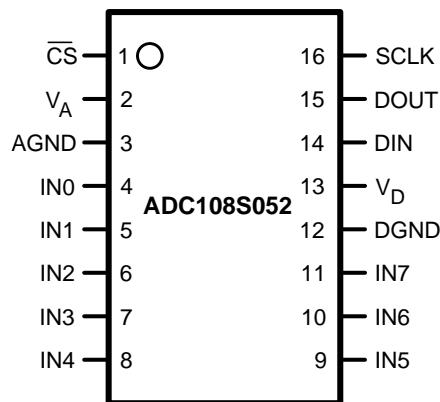
### KEY SPECIFICATIONS

- Conversion Rate: 200 ksps to 500 ksps
- DNL ( $V_A = V_D = 2.7V$  to  $5.0V$ ):  $\pm 0.4$  LSB (max)
- INL ( $V_A = V_D = 2.7V$  to  $5.0V$ ):  $\pm 0.4$  LSB (max)
- Power Consumption:
  - 3V Supply: 1.5 mW (typ)
  - 5V Supply: 7.5 mW (typ)

### APPLICATIONS

- Automotive Navigation
- Portable Systems
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems

### Connection Diagram



**Figure 1. TSSOP Package**  
See Package Number PW0016A

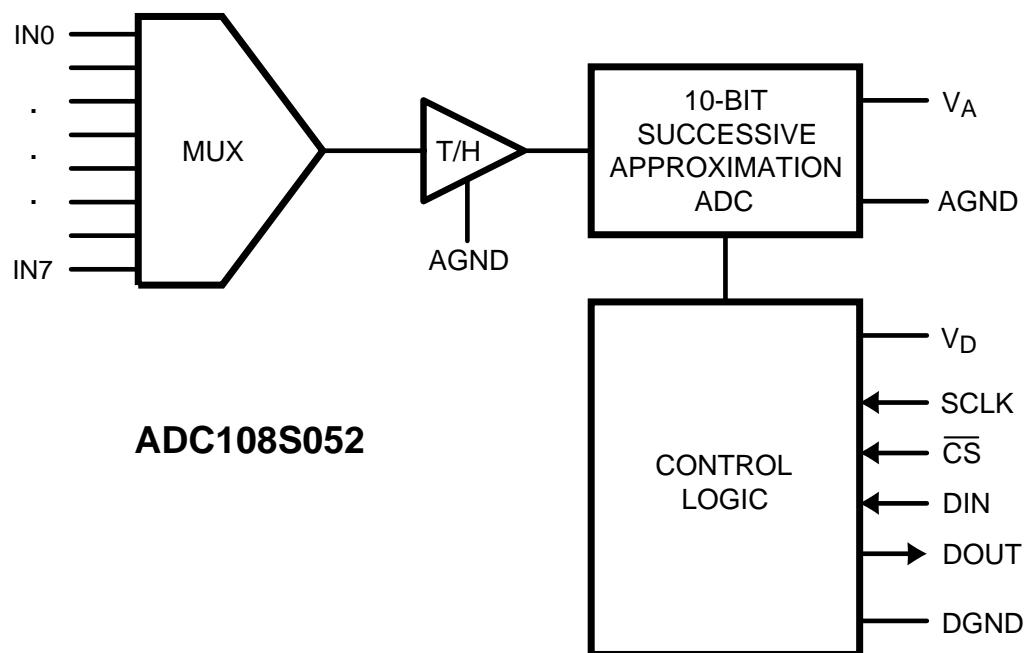


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## Block Diagram



## Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
<b>ANALOG I/O</b>			
4 - 11	IN0 to IN7		Analog inputs. These signals can range from 0V to $V_{REF}$ .
<b>DIGITAL I/O</b>			
16	SCLK		Digital clock input. The specified performance range of frequencies for this input is 3.2 MHz to 8 MHz. This clock directly controls the conversion and readout processes.
15	DOUT		Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
14	DIN		Digital data input. The ADC108S052's Control Register is loaded through this pin on rising edges of the SCLK pin.
1	$\overline{CS}$		Chip select. On the falling edge of $\overline{CS}$ , a conversion process begins. Conversions continue as long as CS is held low.
<b>POWER SUPPLY</b>			
2	$V_A$		Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with 1 $\mu$ F and 0.1 $\mu$ F monolithic ceramic capacitors located within 1 cm of the power pin.
13	$V_D$		Positive digital supply pin. This pin should be connected to a +2.7V to $V_A$ supply, and bypassed to GND with a 0.1 $\mu$ F monolithic ceramic capacitor located within 1 cm of the power pin.
3	AGND		The ground return for the analog supply and signals.
12	DGND		The ground return for the digital supply and signals.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

Analog Supply Voltage $V_A$	−0.3V to 6.5V	
Digital Supply Voltage $V_D$	−0.3V to $V_A + 0.3V$ , max 6.5V	
Voltage on Any Pin to GND	−0.3V to $V_A + 0.3V$	
Input Current at Any Pin <sup>(3)</sup>	±10 mA	
Package Input Current <sup>(3)</sup>	±20 mA	
Power Dissipation at $T_A = 25^\circ\text{C}$	See <sup>(4)</sup>	
ESD Susceptibility <sup>(5)</sup>	Human Body Model	2500V
	Machine Model	250V
For soldering specifications: <a href="http://www.ti.com/lit/SNOA549">http://www.ti.com/lit/SNOA549</a>		
Junction Temperature	+150°C	
Storage Temperature	−65°C to +150°C	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) When the input voltage at any pin exceeds the power supplies (that is,  $V_{IN} < AGND$  or  $V_{IN} > V_A$  or  $V_D$ ), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
- (4) The absolute maximum junction temperature ( $T_{Jmax}$ ) for this device is 150°C. The maximum allowable power dissipation is dictated by  $T_{Jmax}$ , the junction-to-ambient thermal resistance ( $\theta_{JA}$ ), and the ambient temperature ( $T_A$ ), and can be calculated using the formula  $P_{D\text{MAX}} = (T_{Jmax} - T_A)/\theta_{JA}$ . In the 16-pin TSSOP,  $\theta_{JA}$  is 96°C/W, so  $P_{D\text{MAX}} = 1,200$  mW at 25°C and 625 mW at the maximum operating ambient temperature of 105°C. Note that the power consumption of this device under normal operation is a maximum of 12 mW. The values for maximum power dissipation listed above will be reached only when the ADC108S052 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
- (5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO ohms

## Operating Ratings<sup>(1)(2)</sup>

Operating Temperature	−40°C ≤ $T_A$ ≤ +105°C
$V_A$ Supply Voltage	+2.7V to +5.25V
$V_D$ Supply Voltage	+2.7V to $V_A$
Digital Input Voltage	0V to $V_A$
Analog Input Voltage	0V to $V_A$
Clock Frequency	50 kHz to 16 MHz

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

## Package Thermal Resistance

Package	$\theta_{JA}$
16-lead TSSOP on 4-layer, 2 oz. PCB	96°C / W

**ADC108S052 Converter Electrical Characteristics<sup>(1)</sup>**

The following specifications apply for  $V_A = V_D = +2.7V$  to  $+5.25V$ ,  $AGND = DGND = 0V$ ,  $f_{SCLK} = 3.2$  MHz to 8 MHz,  $f_{SAMPLE} = 200$  ksp/s to 500 ksp/s, and  $C_L = 50pF$ , unless otherwise noted. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** : all other limits  $T_A = 25^\circ C$ .

Parameter	Test Conditions	Typ	Limits <sup>(2)</sup>	Units	
<b>STATIC CONVERTER CHARACTERISTICS</b>					
Resolution with No Missing Codes			<b>10</b>	Bits	
INL	Integral Non-Linearity (End Point Method)		<b>±0.1</b>	<b>±0.4</b> LSB (max)	
DNL	Differential Non-Linearity		<b>±0.2</b>	<b>±0.4</b> LSB (min)	
$V_{OFF}$	Offset Error		<b>+0.3</b>	<b>±0.7</b> LSB (max)	
OEM	Offset Error Match		<b>±0.06</b>	<b>±0.4</b> LSB (max)	
FSE	Full Scale Error		<b>+0.1</b>	<b>±0.4</b> LSB (max)	
FSEM	Full Scale Error Match		<b>±0.06</b>	<b>±0.4</b> LSB (max)	
<b>DYNAMIC CONVERTER CHARACTERISTICS</b>					
FPBW	Full Power Bandwidth (~3dB)		<b>8</b>	MHz	
SINAD	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 40.2$ kHz, $-0.02$ dBFS	<b>61.8</b>	<b>61.3</b> dB (min)	
SNR	Signal-to-Noise Ratio	$f_{IN} = 40.2$ kHz, $-0.02$ dBFS	<b>61.8</b>	<b>61.4</b> dB (min)	
THD	Total Harmonic Distortion	$f_{IN} = 40.2$ kHz, $-0.02$ dBFS	<b>-87.4</b>	<b>-74.5</b> dB (max)	
SFDR	Spurious-Free Dynamic Range	$f_{IN} = 40.2$ kHz, $-0.02$ dBFS	<b>83.2</b>	<b>76.0</b> dB (min)	
ENOB	Effective Number of Bits	$f_{IN} = 40.2$ kHz	<b>9.98</b>	<b>9.89</b> Bits (min)	
ISO	Channel-to-Channel Isolation	$f_{IN} = 20$ kHz	<b>78.6</b>	dB	
IMD	Intermodulation Distortion, Second Order Terms	$f_a = 19.5$ kHz, $f_b = 20.5$ kHz	<b>-85.1</b>	dB	
	Intermodulation Distortion, Third Order Terms	$f_a = 19.5$ kHz, $f_b = 20.5$ kHz	<b>-81.6</b>	dB	
<b>ANALOG INPUT CHARACTERISTICS</b>					
$V_{IN}$	Input Range		0 to $V_A$	V	
$I_{DCL}$	DC Leakage Current			<b>±1</b> $\mu A$ (max)	
$C_{INA}$	Input Capacitance	Track Mode	<b>33</b>	pF	
		Hold Mode	<b>3</b>	pF	
<b>DIGITAL INPUT CHARACTERISTICS</b>					
$V_{IH}$	Input High Voltage	$V_A = V_D = +2.7V$ to $+3.6V$		<b>2.1</b>	V (min)
		$V_A = V_D = +4.75V$ to $+5.25V$		<b>2.4</b>	V (min)
$V_{IL}$	Input Low Voltage			<b>0.8</b>	V (max)
$I_{IN}$	Input Current	$V_{IN} = 0V$ or $V_D$	$±0.01$	<b>±1</b>	$\mu A$ (max)
$C_{IND}$	Digital Input Capacitance		<b>2</b>	<b>4</b>	pF (max)
<b>DIGITAL OUTPUT CHARACTERISTICS</b>					
$V_{OH}$	Output High Voltage	$I_{SOURCE} = 200$ $\mu A$ ,		<b><math>V_D - 0.5</math></b>	V (min)
$V_{OL}$	Output Low Voltage	$I_{SINK} = 200$ $\mu A$ to 1.0 mA,		<b>0.4</b>	V (max)
$I_{OZH}, I_{OZL}$	Hi-Impedance Output Leakage Current			<b>±1</b>	$\mu A$ (max)
$C_{OUT}$	Hi-Impedance Output Capacitance <sup>(1)</sup>		<b>2</b>	<b>4</b>	pF (max)
	Output Coding		Straight (Natural) Binary		

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.  
 (2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).

**ADC108S052 Converter Electrical Characteristics<sup>(1)</sup> (continued)**

The following specifications apply for  $V_A = V_D = +2.7V$  to  $+5.25V$ ,  $AGND = DGND = 0V$ ,  $f_{SCLK} = 3.2$  MHz to 8 MHz,  $f_{SAMPLE} = 200$  ksp/s to 500 ksp/s, and  $C_L = 50pF$ , unless otherwise noted. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** : all other limits  $T_A = 25^\circ C$ .

Parameter		Test Conditions	Typ	Limits <sup>(2)</sup>	Units
<b>POWER SUPPLY CHARACTERISTICS</b> ( $C_L = 10$ pF)					
$V_A, V_D$	Analog and Digital Supply Voltages	$V_A \geq V_D$		<b>2.7</b>	V (min)
				<b>5.25</b>	V (max)
$I_A + I_D$	Total Supply Current Normal Mode (CS low)	$V_A = V_D = +2.7V$ to $+3.6V$ , $f_{SAMPLE} = 500$ kSPS, $f_{IN} = 40$ kHz	0.49	<b>1.1</b>	mA (max)
		$V_A = V_D = +4.75V$ to $+5.25V$ , $f_{SAMPLE} = 500$ kSPS, $f_{IN} = 40$ kHz	1.50	<b>2.4</b>	mA (max)
	Total Supply Current Shutdown Mode (CS high)	$V_A = V_D = +2.7V$ to $+3.6V$ , $f_{SCLK} = 0$ ksp/s	30		nA
		$V_A = V_D = +4.75V$ to $+5.25V$ , $f_{SCLK} = 0$ ksp/s	60		nA
$P_C$	Power Consumption Normal Mode (CS low)	$V_A = V_D = +3.0V$ $f_{SAMPLE} = 500$ kSPS, $f_{IN} = 40$ kHz	1.5	<b>3.3</b>	mW (max)
		$V_A = V_D = +5.0V$ $f_{SAMPLE} = 500$ kSPS, $f_{IN} = 40$ kHz	7.5	<b>12.1</b>	mW (max)
	Power Consumption Shutdown Mode (CS high)	$V_A = V_D = +3.0V$ $f_{SCLK} = 0$ ksp/s	0.09		μW
		$V_A = V_D = +5.0V$ $f_{SCLK} = 0$ ksp/s	0.30		μW
<b>AC ELECTRICAL CHARACTERISTICS</b>					
$f_{SCLKMIN}$	Minimum Clock Frequency		0.8	<b>3.2</b>	MHz (min)
$f_{SCLK}$	Maximum Clock Frequency		16	<b>8</b>	MHz (max)
$f_s$	Sample Rate Continuous Mode		50	<b>200</b>	ksp/s (min)
			1000	<b>500</b>	ksp/s (max)
$t_{CONVERT}$	Conversion (Hold) Time			<b>13</b>	SCLK cycles
$DC$	SCLK Duty Cycle		30	<b>40</b>	% (min)
			70	<b>60</b>	% (max)
$t_{ACQ}$	Acquisition (Track) Time			<b>3</b>	SCLK cycles
	Throughput Time	Acquisition Time + Conversion Time		<b>16</b>	SCLK cycles
$t_{AD}$	Aperture Delay		4		ns

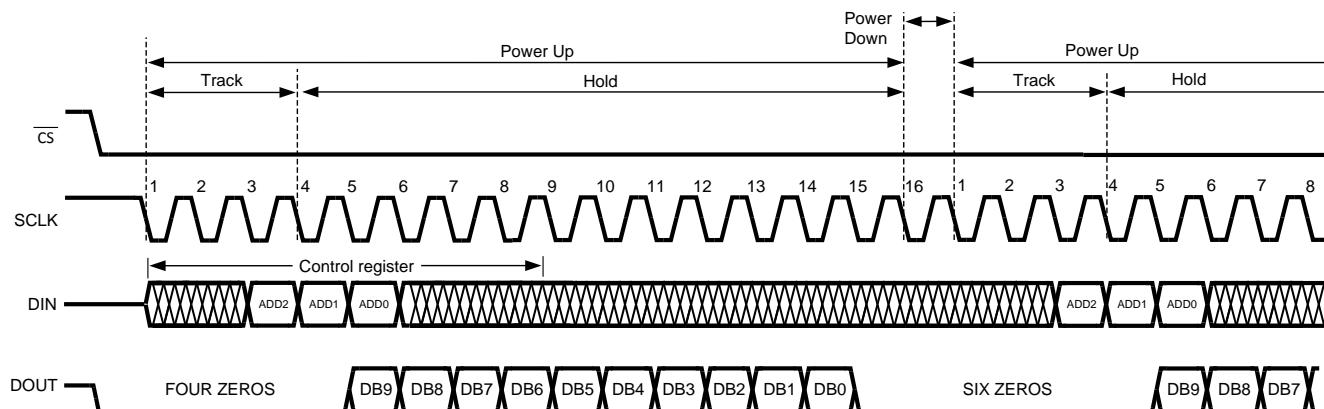
## ADC108S052 Timing Specifications

The following specifications apply for  $V_A = V_D = +2.7V$  to  $+5.25V$ ,  $AGND = DGND = 0V$ ,  $f_{SCLK} = 3.2$  MHz to 8 MHz,  $f_{SAMPLE} = 200$  ksp/s to 500 ksp/s, and  $C_L = 50pF$ . **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** : all other limits  $T_A = 25^\circ C$ .

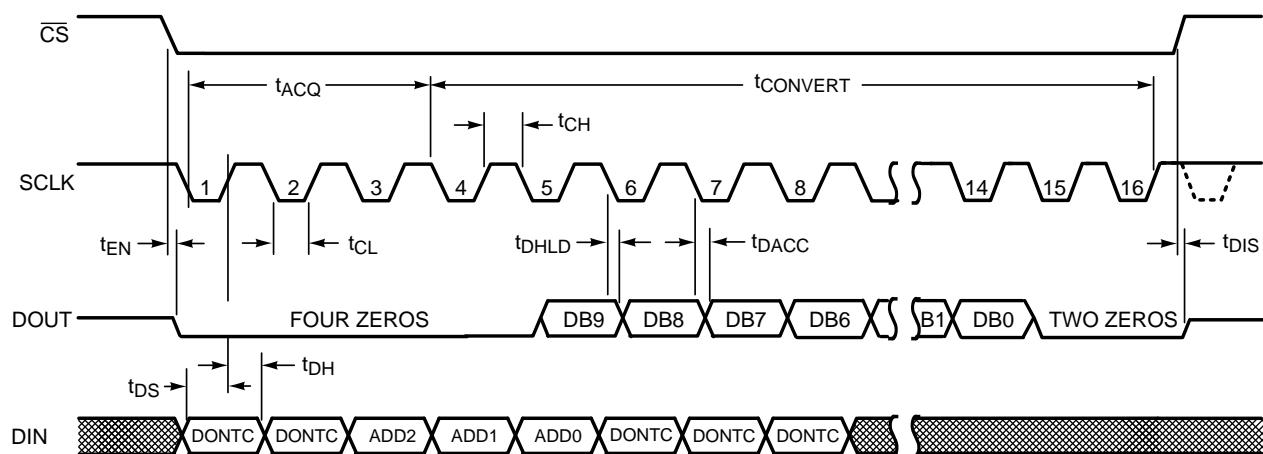
Parameter	Test Conditions	Typ	Limits (1)	Units
$t_{CSH}$	CS Hold Time after SCLK Rising Edge	0	<b>10</b>	ns (min)
$t_{CSS}$	$\overline{CS}$ Setup Time prior to SCLK Rising Edge	5	<b>10</b>	ns (min)
$t_{EN}$	$\overline{CS}$ Falling Edge to DOUT enabled	5	<b>30</b>	ns (max)
$t_{DACC}$	DOUT Access Time after SCLK Falling Edge	17	<b>27</b>	ns (max)
$t_{DHLD}$	DOUT Hold Time after SCLK Falling Edge	4		ns (typ)
$t_{DS}$	DIN Setup Time prior to SCLK Rising Edge	3	<b>10</b>	ns (min)
$t_{DH}$	DIN Hold Time after SCLK Rising Edge	3	<b>10</b>	ns (min)
$t_{CH}$	SCLK High Time		<b>0.4 x <math>t_{SCLK}</math></b>	ns (min)
$t_{CL}$	SCLK Low Time		<b>0.4 x <math>t_{SCLK}</math></b>	ns (min)
$t_{DIS}$	$\overline{CS}$ Rising Edge to DOUT High-Impedance	DOUT falling	<b>20</b>	ns (max)
		DOUT rising	0.9	<b>20</b>

(1) Tested limits are ensured to AOQL (Average Outgoing Quality Level).

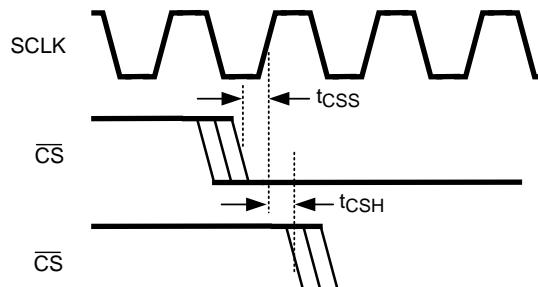
## Timing Diagrams



**Figure 2. ADC108S052 Operational Timing Diagram**



**Figure 3. ADC108S052 Serial Timing Diagram**



**Figure 4. SCLK and CS Timing Parameters**

## Specification Definitions

**ACQUISITION TIME** is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

**APERTURE DELAY** is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

**CONVERSION TIME** is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

**CHANNEL-TO-CHANNEL ISOLATION** is resistance to coupling of energy from one channel into another channel.

**CROSSTALK** is the coupling of energy from one channel into another channel. This is similar to Channel-to-Channel Isolation, except for the sign of the data.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**DUTY CYCLE** is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as  $(\text{SINAD} - 1.76) / 6.02$  and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**FULL SCALE ERROR (FSE)** is a measure of how far the last code transition is from the ideal  $1\frac{1}{2}$  LSB below  $V_{\text{REF}}^+$  and is defined as:

$$V_{\text{FSE}} = V_{\text{max}} + 1.5 \text{ LSB} - V_{\text{REF}}^+$$

where

- $V_{\text{max}}$  is the voltage at which the transition to the maximum code occurs. FSE can be expressed in Volts, LSB or percent of full scale range. (1)

**GAIN ERROR** is the deviation of the last code transition (111...110) to (111...111) from the ideal ( $V_{\text{REF}} - 1.5$  LSB), after adjusting for offset error.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from negative full scale ( $\frac{1}{2}$  LSB below the first code transition) through positive full scale ( $\frac{1}{2}$  LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in both the second or the third order intermodulation products to the power in one of the original frequencies. Second order products are  $f_a \pm f_b$ , where  $f_a$  and  $f_b$  are the two sine wave input frequencies. Third order products are  $(2f_a \pm f_b)$  and  $(f_a \pm 2f_b)$ . IMD is usually expressed in dB.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. The ADC108S052 is specified not to have any missing codes.

**OFFSET ERROR** is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including d.c. or the harmonics included in THD.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal where a spurious signal is any signal present in the output spectrum that is not present at the input, including harmonics but excluding d.c.

**TOTAL HARMONIC DISTORTION (THD)** is the ratio, expressed in dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$\text{THD} = 20 \times \log_{10} \sqrt{\frac{A_{f2}^2 + \dots + A_{f6}^2}{A_{f1}^2}}$$

where

- $A_{f1}$  is the RMS power of the input frequency at the output and  $A_{f2}$  through  $A_{f6}$  are the RMS power in the first 5 harmonic frequencies. (2)

**THROUGHPUT TIME** is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion and read out times. In the case of the ADC108S052, this is 16 SCLK periods.

### Typical Performance Characteristics

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 500 \text{ kspS}$ ,  $f_{\text{SCLK}} = 8 \text{ MHz}$ ,  $f_{\text{IN}} = 40.2 \text{ kHz}$  unless otherwise stated.

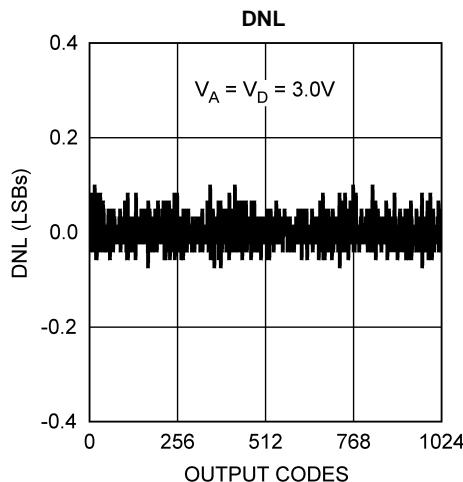


Figure 5.

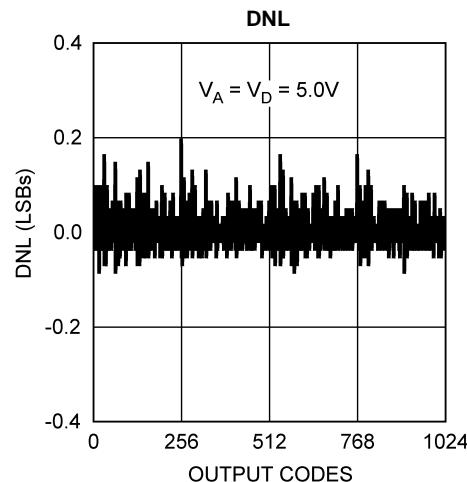


Figure 6.

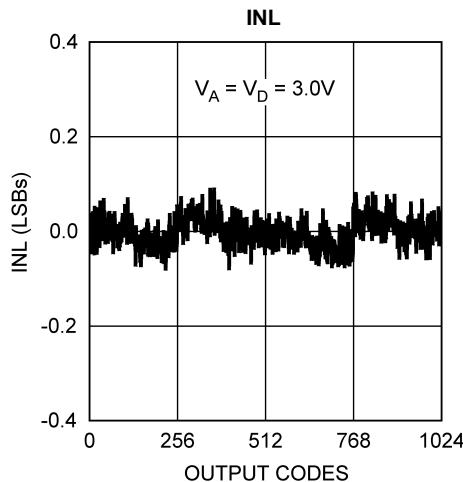


Figure 7.

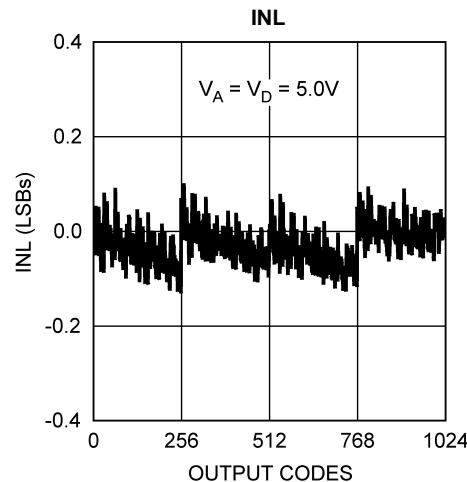


Figure 8.

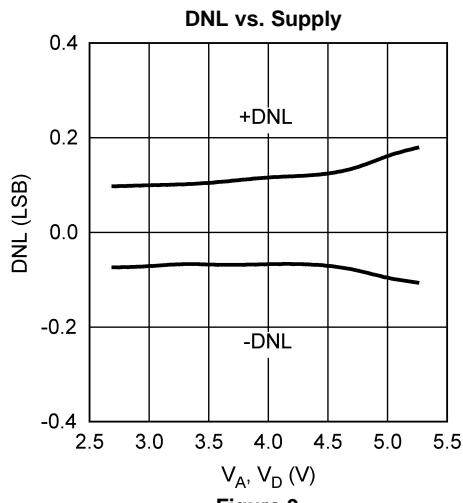


Figure 9.

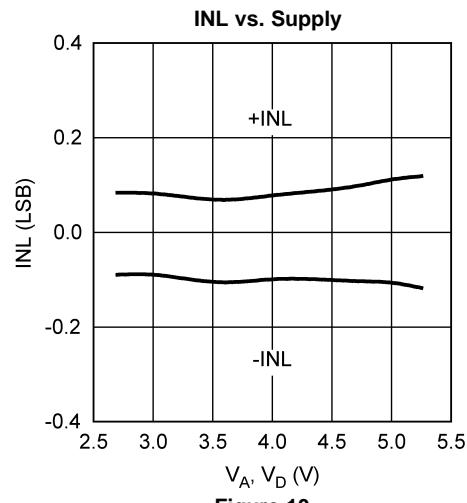


Figure 10.

### Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 500 \text{ ksps}$ ,  $f_{\text{SCLK}} = 8 \text{ MHz}$ ,  $f_{\text{IN}} = 40.2 \text{ kHz}$  unless otherwise stated.

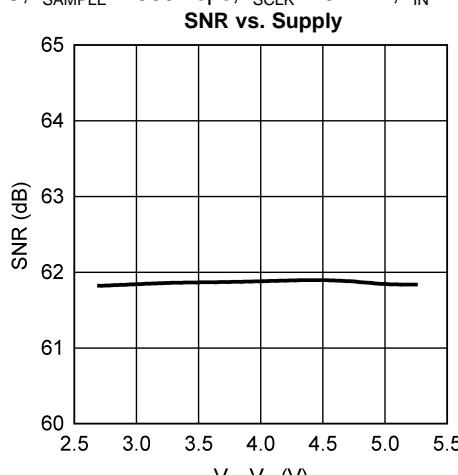


Figure 11.

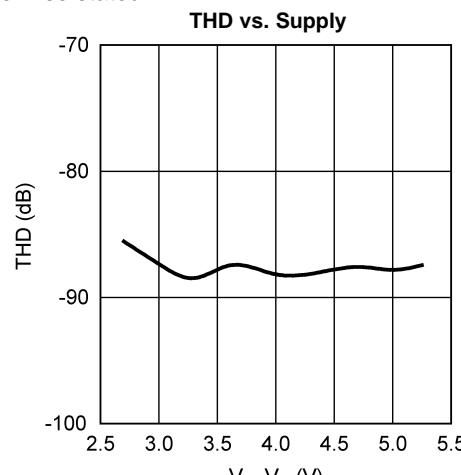


Figure 12.

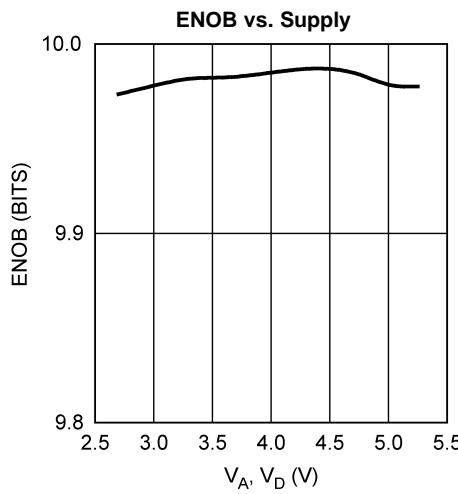


Figure 13.

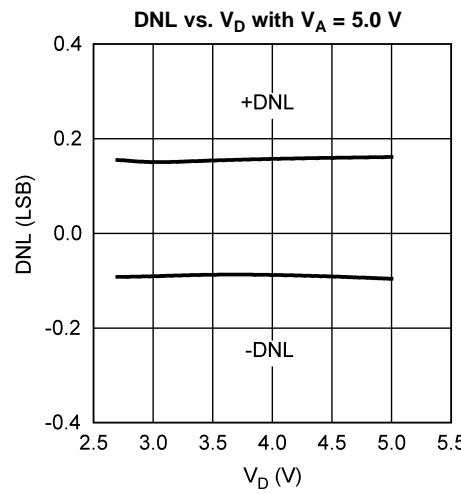


Figure 14.

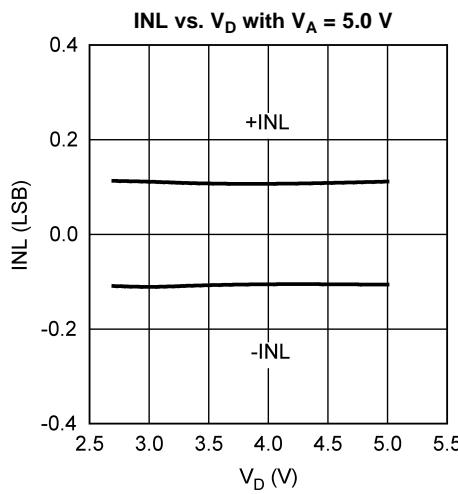


Figure 15.

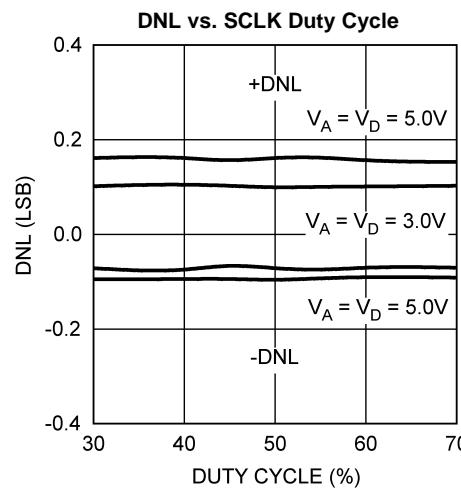


Figure 16.

### Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 500 \text{ ksps}$ ,  $f_{\text{SCLK}} = 8 \text{ MHz}$ ,  $f_{\text{IN}} = 40.2 \text{ kHz}$  unless otherwise stated.

#### INL vs. SCLK Duty Cycle

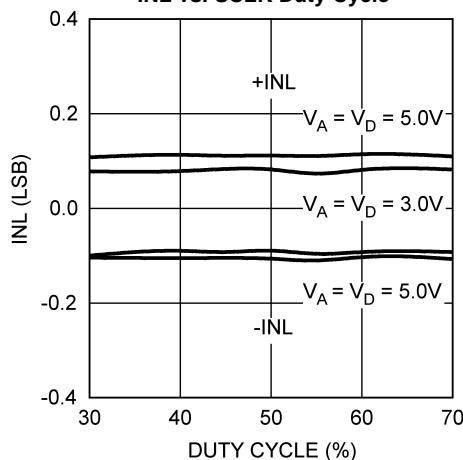


Figure 17.

#### SNR vs. SCLK Duty Cycle

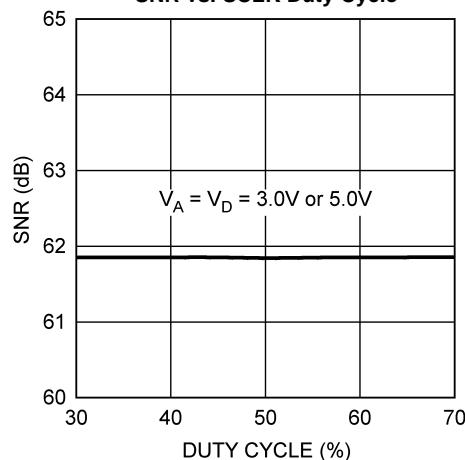


Figure 18.

#### THD vs. SCLK Duty Cycle

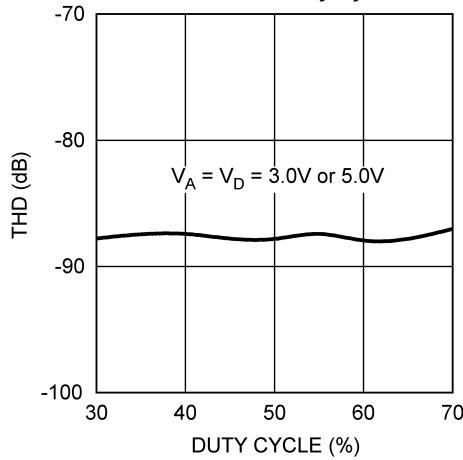


Figure 19.

#### ENOB vs. SCLK Duty Cycle

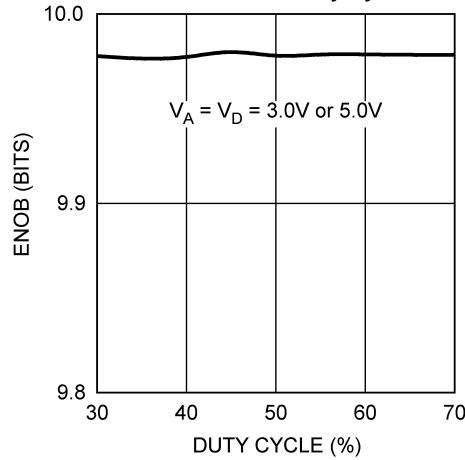


Figure 20.

#### DNL vs. SCLK

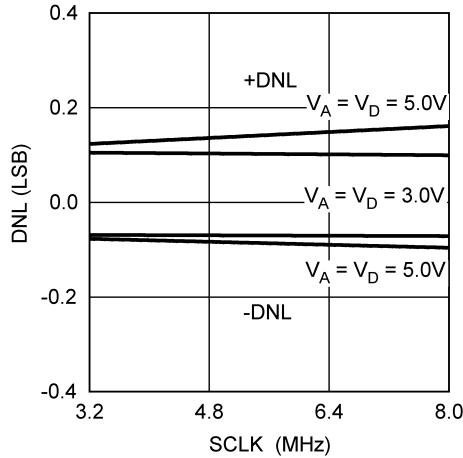


Figure .

#### INL vs. SCLK

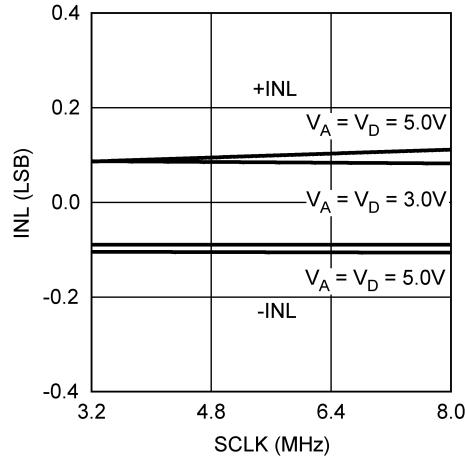


Figure 21.

### Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 500$  ksps,  $f_{\text{SCLK}} = 8$  MHz,  $f_{\text{IN}} = 40.2$  kHz unless otherwise stated.

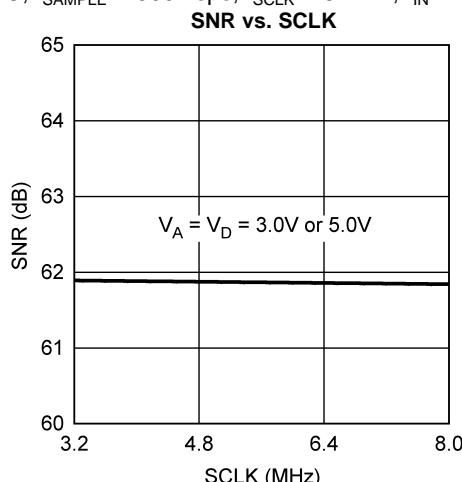


Figure 21.

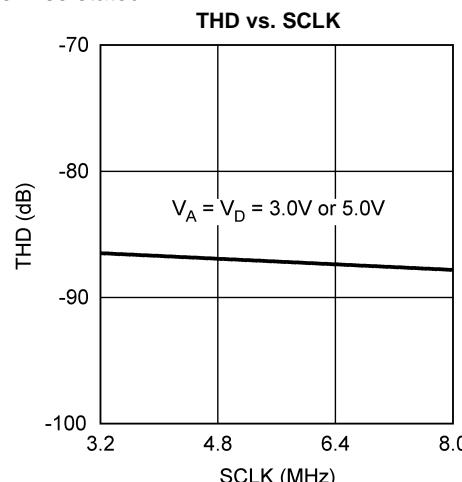


Figure 22.

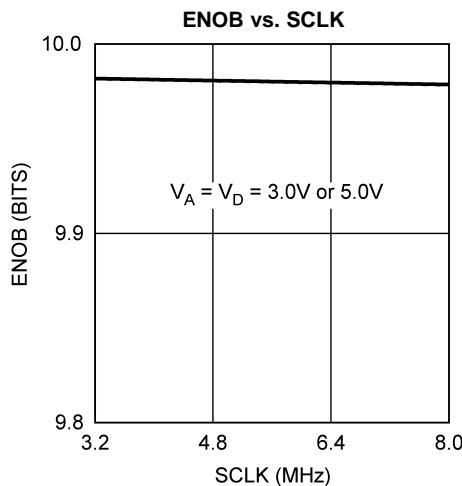


Figure 23.

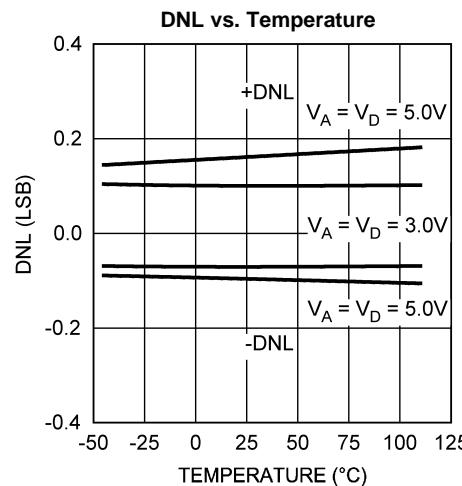


Figure 24.

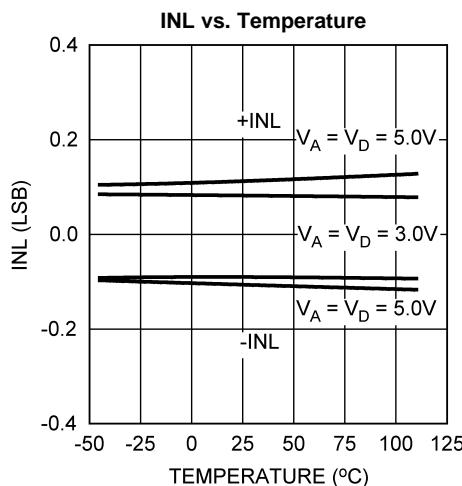


Figure 25.

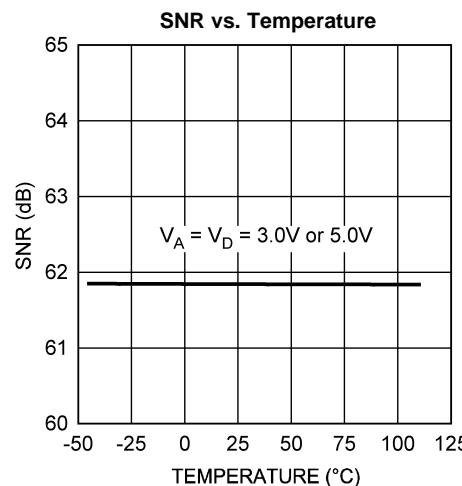


Figure 26.

### Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 500 \text{ kspS}$ ,  $f_{\text{SCLK}} = 8 \text{ MHz}$ ,  $f_{\text{IN}} = 40.2 \text{ kHz}$  unless otherwise stated.

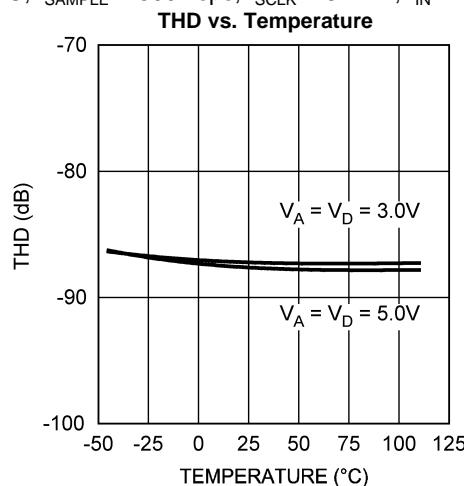


Figure 27.

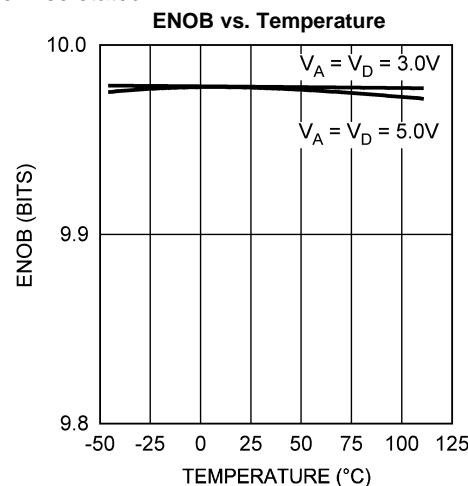


Figure 28.

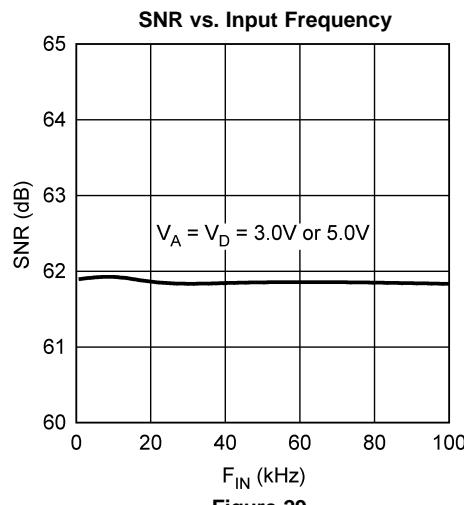


Figure 29.

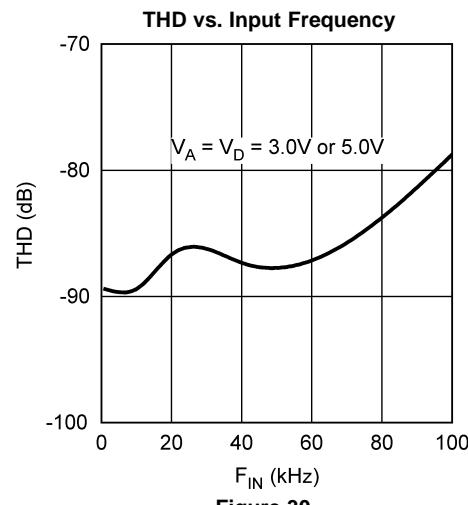


Figure 30.

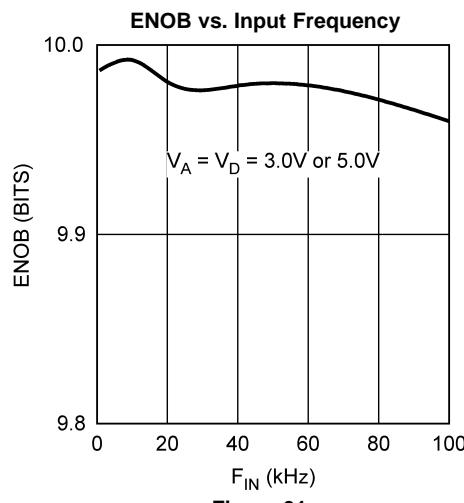


Figure 31.

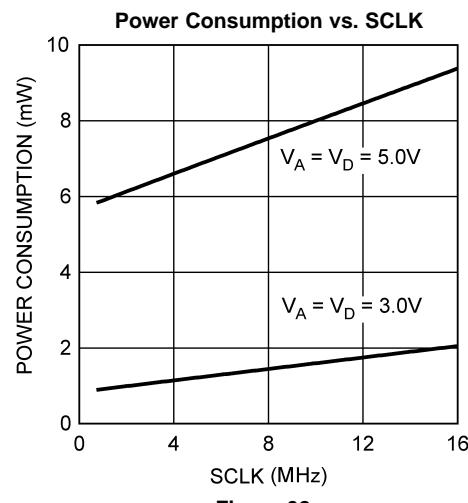


Figure 32.

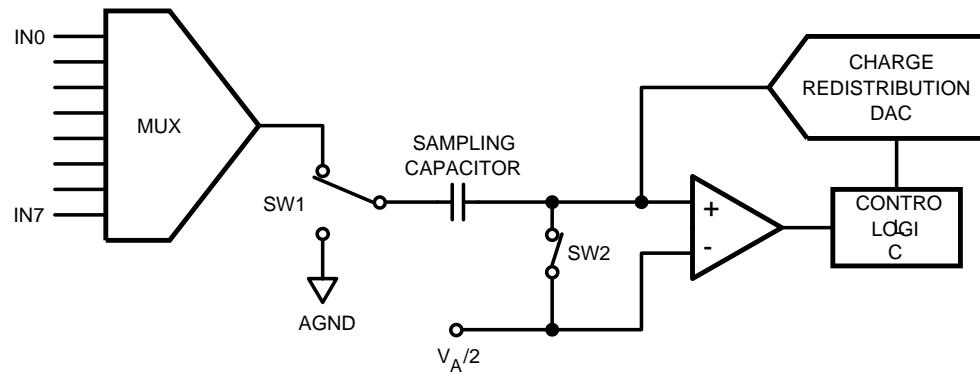
## FUNCTIONAL DESCRIPTION

The ADC108S052 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter.

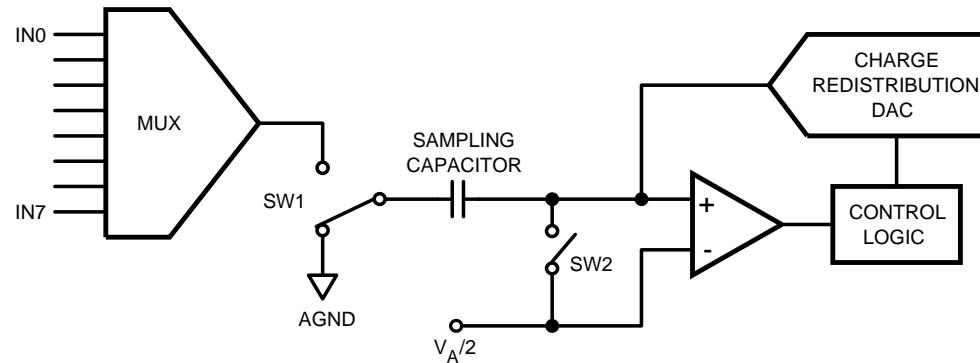
### ADC108S052 OPERATION

Simplified schematics of the ADC108S052 in both track and hold operation are shown in [Figure 33](#) and [Figure 34](#) respectively. In [Figure 33](#), the ADC108S052 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC108S052 is in this state for the first three SCLK cycles after CS is brought low.

[Figure 34](#) shows the ADC108S052 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC108S052 is in this state for the last thirteen SCLK cycles after CS is brought low.



**Figure 33. ADC108S052 in Track Mode**



**Figure 34. ADC108S052 in Hold Mode**

## SERIAL INTERFACE

An operational timing diagram and a serial interface timing diagram for the ADC108S052 are shown in The [Timing Diagrams](#) section. CS, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC108S052's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of  $\overline{CS}$  and ends on the rising edge of  $\overline{CS}$ . Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when CS is high and is active when CS is low. Thus, CS acts as an output enable. Similarly, SCLK is internally gated off when CS is brought high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros, falling edges 5 through 14 clock out the conversion result, MSB first, and falling edges 15 and 16 clock out trailing zeros. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter the track mode on the falling edge of SCLK after the  $N*16$ th rising edge of SCLK and re-enter the hold/convert mode on the  $N*16+4$ th falling edge of SCLK. "N" is an integer value.

The ADC108S052 enters track mode under three different conditions. In [Figure 2](#), CS goes low with SCLK high and the ADC enters track mode on the first falling edge of SCLK. In the second condition, CS goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of CS is seen as the first falling edge of SCLK. In the third condition, CS and SCLK go low simultaneously and the ADC enters track mode. While there is no timing restriction with respect to the rising edges of CS and SCLK, see [Figure 4](#) for setup and hold time requirements for the falling edge of CS with respect to the rising edge of SCLK.

While a conversion is in progress, the address of the next input for conversion is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of CS. See [Table 1](#), [Table 2](#), and [Table 3](#).

There is no need to incorporate a power-up delay or dummy conversion as the ADC108S052 is able to acquire the input signal to full resolution in the first conversion immediately following power-up. The first conversion result after power-up will be that of IN0.

**Table 1. Control Register Bits**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>DONTC</b>	<b>DONTC</b>	<b>ADD2</b>	<b>ADD1</b>	<b>ADD0</b>	<b>DONTC</b>	<b>DONTC</b>	<b>DONTC</b>

**Table 2. Control Register Bit Descriptions**

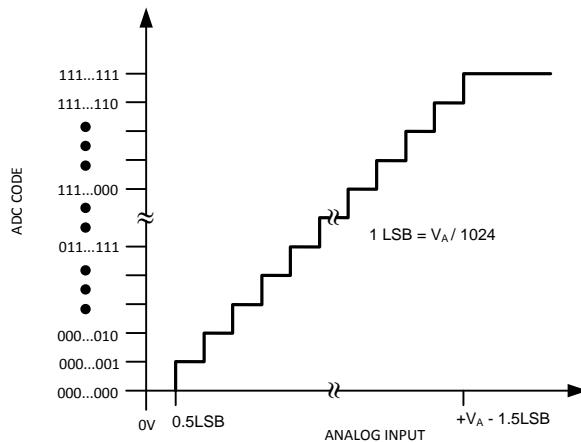
Bit #:	Symbol:	Description
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in <a href="#">Table 3</a> .
4	ADD1	
3	ADD0	

**Table 3. Input Channel Selection**

ADD2	ADD1	ADD0	Input Channel
0	0	0	IN0 (Default)
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

## ADC108S052 TRANSFER FUNCTION

The output format of the ADC108S052 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC108S052 is  $V_A / 1024$ . The ideal transfer characteristic is shown in [Figure 35](#). The transition from an output code of 00 0000 0000 to a code of 00 0000 0001 is at 1/2 LSB, or a voltage of  $V_A / 2048$ . Other code transitions occur at steps of one LSB.

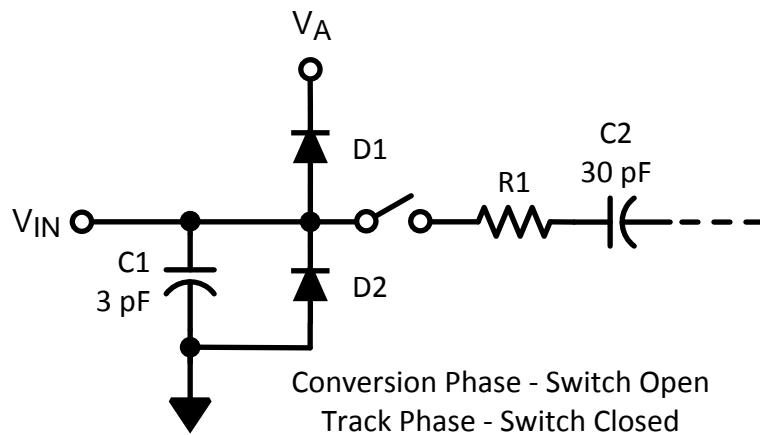


**Figure 35. Ideal Transfer Characteristic**

## ANALOG INPUTS

An equivalent circuit for one of the ADC108S052's input channels is shown in [Figure 36](#). Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to  $V_A$ . Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in [Figure 36](#) has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch and is typically 500 ohms. Capacitor C2 is the ADC108S052 sampling capacitor, and is typically 30 pF. The ADC108S052 will deliver best performance when driven by a low-impedance source (less than 100 ohms). This is especially important when using the ADC108S052 to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.



**Figure 36. Equivalent Input Circuit**

## DIGITAL INPUTS AND OUTPUTS

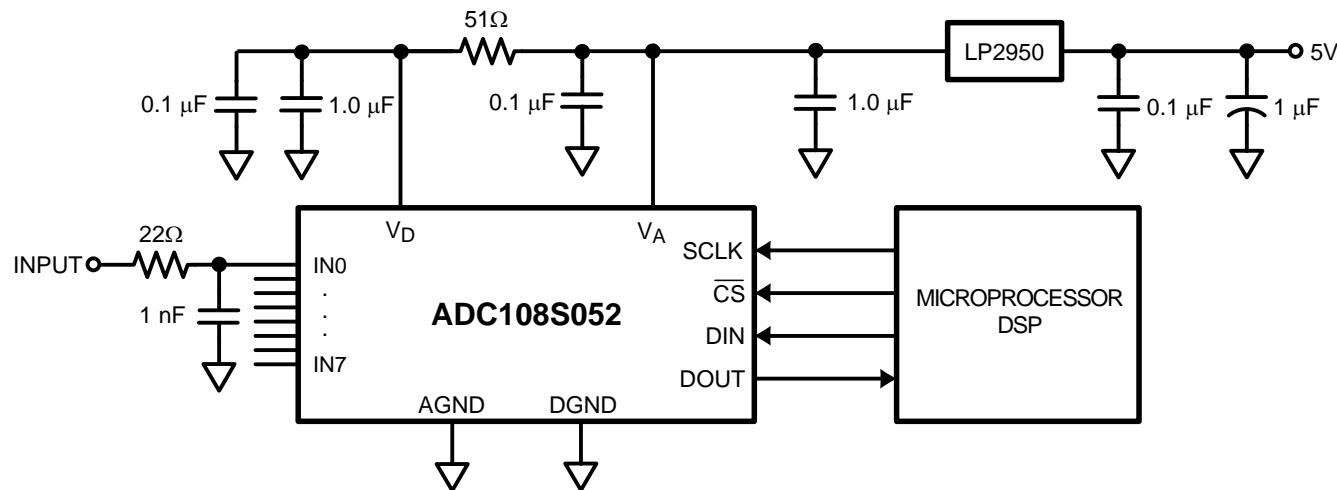
The ADC108S052's digital inputs (SCLK,  $\overline{CS}$ , and DIN) have an operating range of 0 V to  $V_A$ . They are not prone to latch-up and may be asserted before the digital supply ( $V_D$ ) without any risk. The digital output (DOUT) operating range is controlled by  $V_D$ . The output high voltage is  $V_D - 0.5V$  (min) while the output low voltage is 0.4V (max).

## Applications Information

### TYPICAL APPLICATION CIRCUIT

A typical application is shown in [Figure 37](#). The split analog and digital supply pins are both powered in this example by the LP2950 low-dropout voltage regulator. The analog supply is bypassed with a capacitor network located close to the ADC108S052. The digital supply is separated from the analog supply by an isolation resistor and bypassed with additional capacitors. The ADC108S052 uses the analog supply ( $V_A$ ) as its reference voltage, so it is very important that  $V_A$  be kept as clean as possible. Due to the low power requirements of the ADC108S052, it is also possible to use a precision reference as a power supply.

To minimize the error caused by the changing input capacitance of the ADC108S052, a capacitor is connected from each input pin to ground. The capacitor, which is much larger than the input capacitance of the ADC108S052 when in track mode, provides the current to quickly charge the sampling capacitor of the ADC108S052. An isolation resistor is added to isolate the load capacitance from the input source.



**Figure 37. Typical Application Circuit**

## POWER SUPPLY CONSIDERATIONS

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

### Power Supply Sequence

The ADC108S052 is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply ( $V_D$ ) cannot exceed the analog supply ( $V_A$ ) by more than 300 mV, not even on a transient basis. Therefore,  $V_A$  must ramp up before or concurrently with  $V_D$ .

### Power Management

The ADC108S052 is fully powered-up whenever  $\overline{CS}$  is low and fully powered-down whenever  $\overline{CS}$  is high, with one exception. If operating in continuous conversion mode, the ADC108S052 automatically enters power-down mode between SCLK's 16th falling edge of a conversion and SCLK's 1st falling edge of the subsequent conversion (see [Figure 2](#)).

In continuous conversion mode, the ADC108S052 can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the ADC108S052 will perform conversions continuously as long as CS is held low. Continuous mode offers maximum throughput.

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. The Power Consumption vs. SCLK curve in the [Typical Performance Characteristics](#) section shows the typical power consumption of the ADC108S052. To calculate the power consumption ( $P_C$ ), simply multiply the fraction of time spent in the normal mode ( $t_N$ ) by the normal mode power consumption ( $P_N$ ), and add the fraction of time spent in shutdown mode ( $t_S$ ) multiplied by the shutdown mode power consumption ( $P_S$ ) as shown in [Figure 38](#).

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S$$

**Figure 38. Power Consumption Equation**

### Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply,  $V_D$ . The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100  $\Omega$  series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Since the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

## LAYOUT AND GROUNDING

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC108S052 due to supply noise, do not use the same supply for the ADC108S052 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.

**REVISION HISTORY**

<b>Changes from Revision F (March 2013) to Revision G</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	20

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC108S052CIMT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	108S052 CIMT	<b>Samples</b>
ADC108S052CIMTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	108S052 CIMT	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

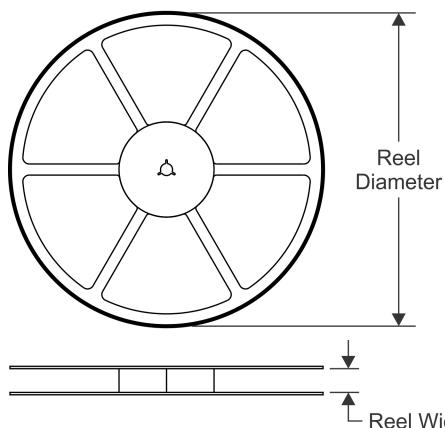
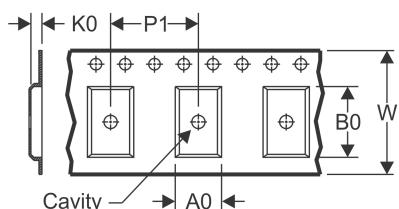
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

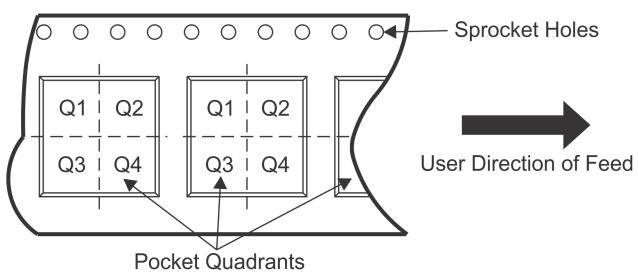
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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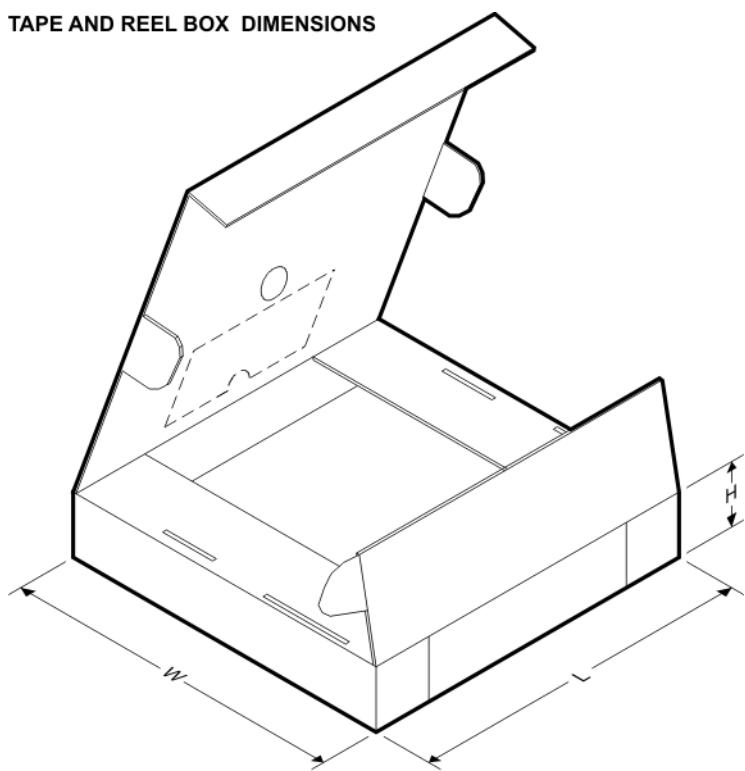
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC108S052CIMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

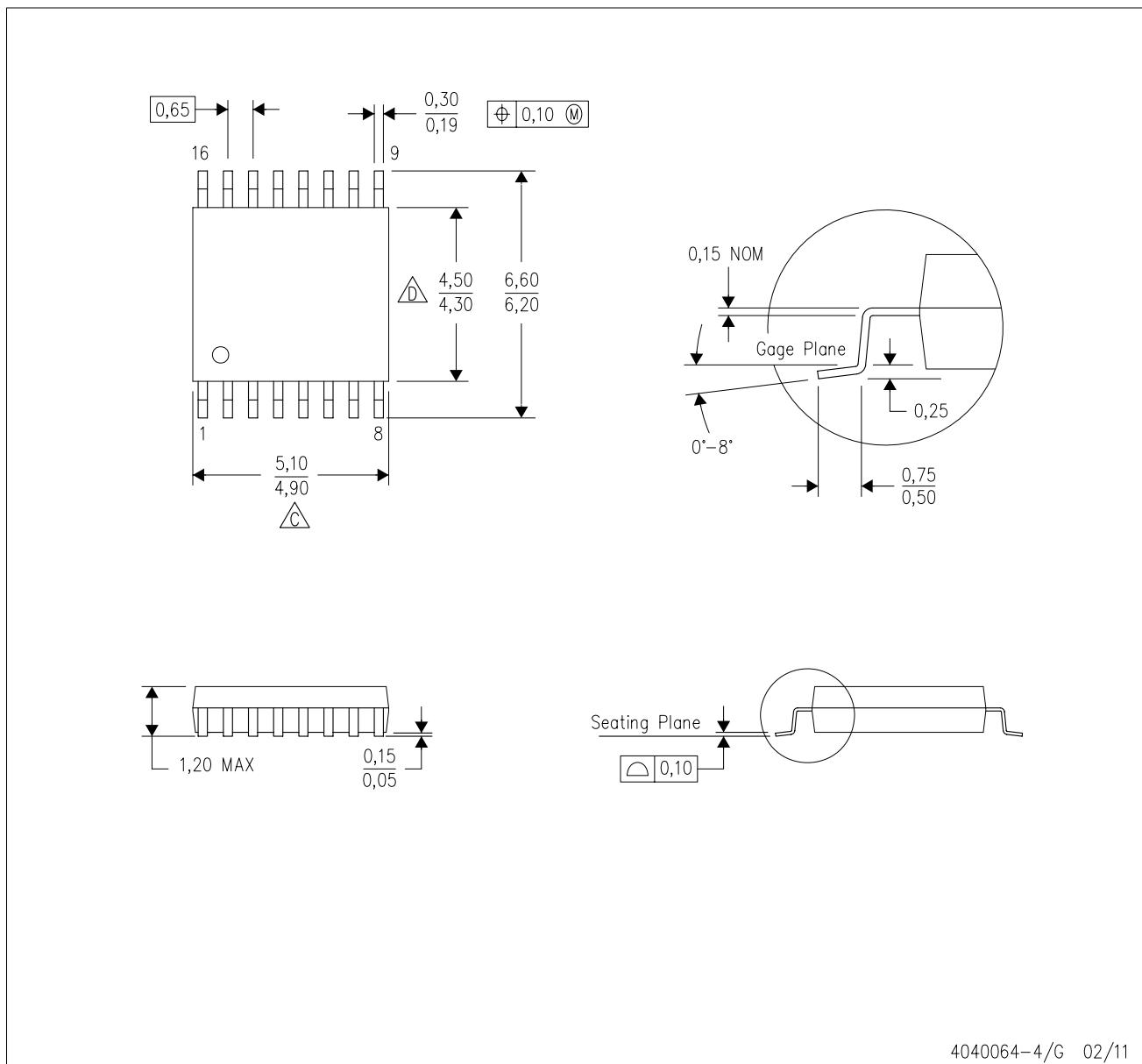
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC108S052CIMTX/NOPB	TSSOP	PW	16	2500	349.0	337.0	45.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

△ C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△ D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

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Products	Applications
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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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