

## 74VCX162374

### Low Voltage 16-Bit D-Type Flip-Flop with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

#### General Description

The VCX162374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and output enable ( $\overline{OE}$ ) are common to each byte and can be shorted together for full 16-bit operation.

The VCX162374 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers/transmitters.

The 74VCX162374 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74VCX162374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.65V–3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 3.4 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.8 ns max for 2.3V to 2.7V  $V_{CC}$
  - 9.6 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - ±12 mA @ 3.0V  $V_{CC}$
  - ±8 mA @ 2.3V  $V_{CC}$
  - ±3 mA @ 1.65V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

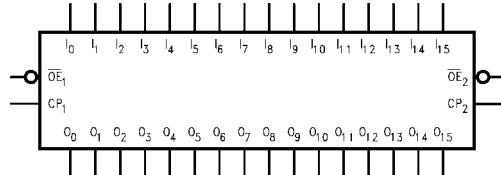
**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX162374MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

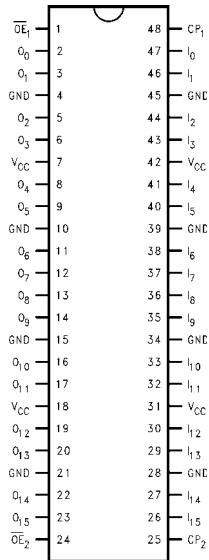
#### Logic Symbol



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP <sub>n</sub>	Clock Pulse Input
I <sub>0</sub> –I <sub>15</sub>	Inputs
O <sub>0</sub> –O <sub>15</sub>	Outputs

## Connection Diagram



## Truth Tables

Inputs		Outputs	
CP <sub>1</sub>	OE <sub>1</sub>	I <sub>0</sub> -I <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
/	L	H	H
/	L	L	L
L	L	X	O <sub>0</sub>
X	H	X	Z

Inputs		Outputs	
CP <sub>2</sub>	OE <sub>2</sub>	I <sub>8</sub> -I <sub>15</sub>	O <sub>8</sub> -O <sub>15</sub>
/	L	H	H
/	L	L	L
L	L	X	O <sub>0</sub>
X	H	X	Z

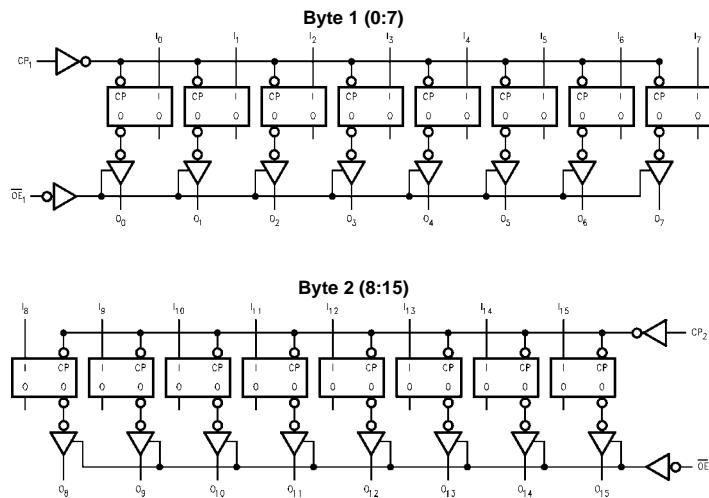
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance  
 O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW of CP

## Functional Description

The 74VCX162374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each clock has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-

flop will store the state of their individual I inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP<sub>n</sub>) transition. With the Output Enable (OE<sub>n</sub>) LOW, the contents of the flip-flops are available at the outputs. When OE<sub>n</sub> is HIGH, the outputs go to the high impedance state. Operations of the OE<sub>n</sub> input does not affect the state of the flip-flops.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

<b>Absolute Maximum Ratings</b> (Note 2)		<b>Recommended Operating Conditions</b> (Note 4)				
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply				
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V	Operating	1.65V to 3.6V			
Output Voltage ( $V_O$ )		Data Retention Only	1.2V to 3.6V			
Outputs 3-STATE	-0.5V to +4.6V	Input Voltage	-0.3V to +3.6V			
Outputs Active (Note 3)	-0.5V to $V_{CC}$ +0.5V	Output Voltage ( $V_O$ )				
DC Input Diode Current ( $I_{IK}$ )		Output in Active States	0V to $V_{CC}$			
$V_I < 0V$	-50 mA	Output in "OFF" State	0.0V to 3.6V			
DC Output Diode Current ( $I_{OK}$ )		Output Current in $I_{OH}/I_{OL}$				
$V_O < 0V$	-50 mA	$V_{CC} = 3.0V$ to 3.6V	$\pm 12$ mA			
$V_O > V_{CC}$	+50 mA	$V_{CC} = 2.3V$ to 2.7V	$\pm 8$ mA			
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA	$V_{CC} = 1.65V$ to 2.3V	$\pm 3$ mA			
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C			
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	Minimum Input Edge Rate ( $\Delta t/\Delta V$ )				
		$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V			
<b>Note 2:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.						
<b>Note 3:</b> $I_O$ Absolute Maximum Rating must be observed.						
<b>Note 4:</b> Floating or unused inputs must be held HIGH or LOW.						
<b>DC Electrical Characteristics (2.7V &lt; <math>V_{CC} \leq 3.6V</math>)</b>						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 – 3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7 – 3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 – 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -6 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -8 \text{ mA}$	3.0	2.4		V
		$I_{OH} = -12 \text{ mA}$	3.0	2.2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7 – 3.6		0.2	V
		$I_{OL} = 6 \text{ mA}$	2.7		0.4	V
		$I_{OL} = 8 \text{ mA}$	3.0		0.55	V
		$I_{OL} = 12 \text{ mA}$	3.0		0.8	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7 – 3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.7 – 3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7 – 3.6		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)	2.7 – 3.6		$\pm 20$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 – 3.6		750	$\mu A$
<b>Note 5:</b> Outputs disabled or 3-STATE only.						

### DC Electrical Characteristics ( $2.3V \leq V_{CC} \leq 2.7V$ )

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.3 – 2.7	1.6		V
$V_{IL}$	LOW Level Input Voltage		2.3 – 2.7		0.7	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 – 2.7	$V_{CC} - 0.2$		V
		$I_{OH} = -4 mA$	2.3	2.0		V
		$I_{OH} = -6 mA$	2.3	1.8		V
		$I_{OH} = -8 mA$	2.3	1.7		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 – 2.7		0.2	V
		$I_{OL} = 6 mA$	2.3		0.4	V
		$I_{OL} = 8 mA$	2.3		0.6	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.3 – 2.7		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 – 2.7		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 2.7		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 6)	2.3 – 2.7		$\pm 20$	$\mu A$

Note 6: Outputs disabled or 3-STATE only.

### DC Electrical Characteristics ( $1.65V \leq V_{CC} < 2.3V$ )

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 – 2.3	$0.65 \times V_{CC}$		V
$V_{IL}$	LOW Level Input Voltage		1.65 – 2.3		$0.35 \times V_{CC}$	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 – 2.3	$V_{CC} - 0.2$		V
		$I_{OH} = -3 mA$	1.65	1.25		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 – 2.3		0.2	V
		$I_{OL} = 3 mA$	1.65		0.3	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 – 2.3		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	1.65 – 2.3		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.65 – 2.3		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 7)	1.65 – 2.3		$\pm 20$	$\mu A$

Note 7: Outputs disabled or 3-STATE only.

## AC Electrical Characteristics (Note 8)

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 30 \text{ pF}$ , $R_L = 500\Omega$						Units	
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$			
		Min	Max	Min	Max	Min	Max		
$f_{MAX}$	Maximum Clock Frequency	250		200		100		MHz	
$t_{PHL}, t_{PLH}$	Prop Delay CP to $O_n$	0.8	3.4	1.0	4.8	1.5	9.6	ns	
$t_{PZL}, t_{PZH}$	Output Enable Time	0.8	3.9	1.0	5.4	1.5	9.8	ns	
$t_{PLZ}, t_{PHZ}$	Output Disable Time	0.8	4.0	1.0	4.4	1.5	7.9	ns	
$t_S$	Setup Time	1.5		1.5		2.5		ns	
$t_H$	Hold Time	1.0		1.0		1.0		ns	
$t_W$	Pulse Width	1.5		1.5		4.0		ns	
$t_{OSHL}$	Output to Output Skew (Note 9)			0.5		0.5		ns	
$t_{OSLH}$							0.75	ns	

Note 8: For  $C_L = 50\text{pF}$ , add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

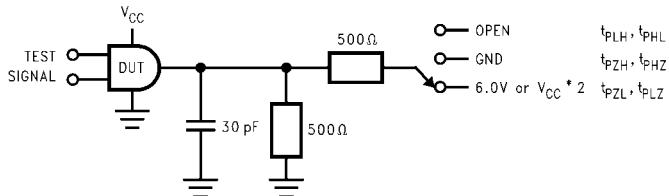
## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30 \text{ pF}$ , $V_{IH} = V_{CC}$ , $V_{IL} = 0\text{V}$	1.8	0.15	
			2.5	0.25	
			3.3	0.35	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 30 \text{ pF}$ , $V_{IH} = V_{CC}$ , $V_{IL} = 0\text{V}$	1.8	-0.15	
			2.5	-0.25	
			3.3	-0.35	V
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$	$C_L = 30 \text{ pF}$ , $V_{IH} = V_{CC}$ , $V_{IL} = 0\text{V}$	1.8	1.55	
			2.5	2.05	
			3.3	2.65	V

## Capacitance

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$	Units
			Typical	
$C_{IN}$	Input Capacitance	$V_{CC} = 1.8V, 2.5V$ or $3.3V$ , $V_I = 0\text{V}$ or $V_{CC}$	6	pF
$C_{OUT}$	Output Capacitance	$V_I = 0\text{V}$ or $V_{CC}$ , $V_{CC} = 1.8V, 2.5V$ or $3.3V$	7	pF
$C_{PD}$	Power Dissipation Capacitance	$V_I = 0\text{V}$ or $V_{CC}$ , $f = 10 \text{ MHz}$ , $V_{CC} = 1.8V, 2.5V$ or $3.3V$	20	pF

## AC Loading and Waveforms



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$6V \text{ at } V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2 \text{ at } V_{CC} = 2.5 \pm 0.2V, 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

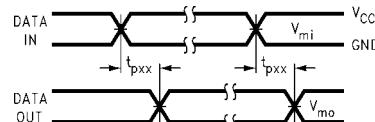


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

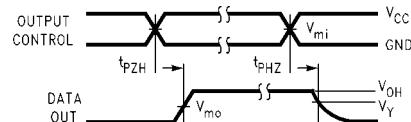


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

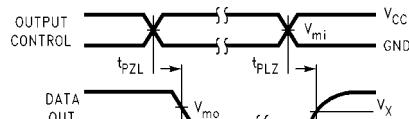


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

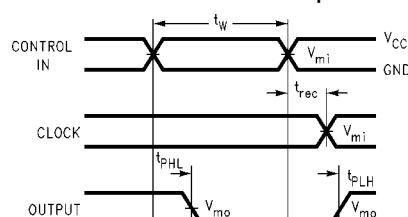
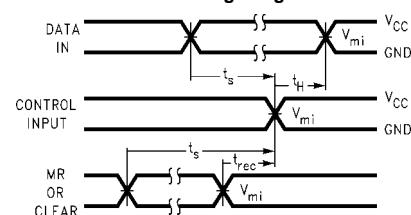
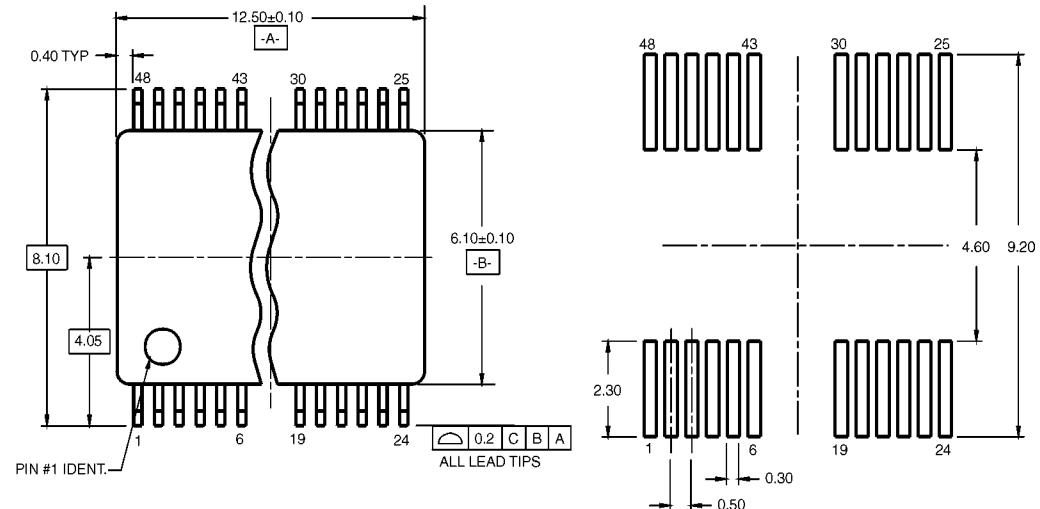
FIGURE 5. Propagation Delay, Pulse Width and  $t_{REC}$  Waveforms

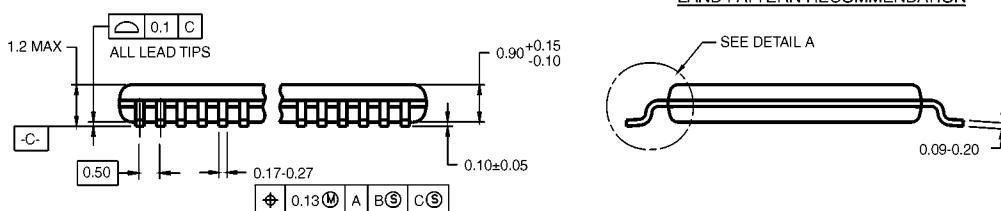
FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



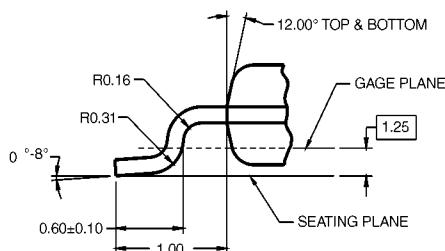
DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

DETAIL A



**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Body Width  
Package Number MTD48**

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