



Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374T/AT/CT/DT - 2374T/AT/CT

IDT54/74FCT534T/AT/CT

IDT54/74FCT574T/AT/CT/DT - 2574T/AT/CT

FEATURES:

• Common features:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

• Features for FCT374T/FCT534T/FCT574T:

- Std., A, C and D speed grades
- High drive outputs (-15mA I_{OH} , 48mA I_{OL})

• Features for FCT2374T/FCT2574T:

- Std., A, and C speed grades
- Resistor outputs (-15mA I_{OH} , 12mA I_{OL} Com.)
(-12mA I_{OH} , 12mA I_{OL} Mil.)
- Reduced system switching noise

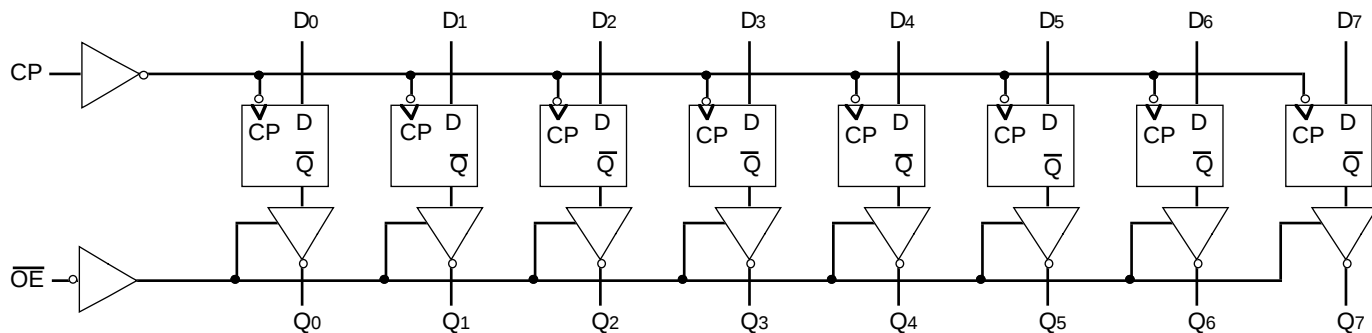
DESCRIPTION

The FCT374T/FCT2374T, FCT534T and FCT574T/FCT2574T are 8-bit registers built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

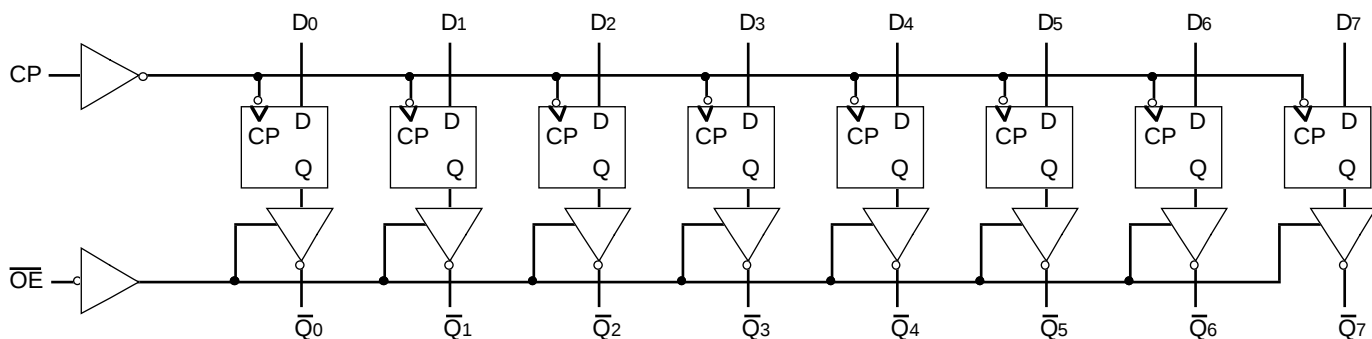
The FCT2374T and FCT2574T have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM FCT374/FCT2374T AND FCT574/FCT2574T



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FUNCTIONAL BLOCK DIAGRAM FCT534T



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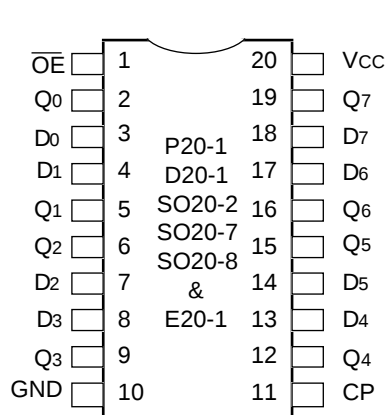
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

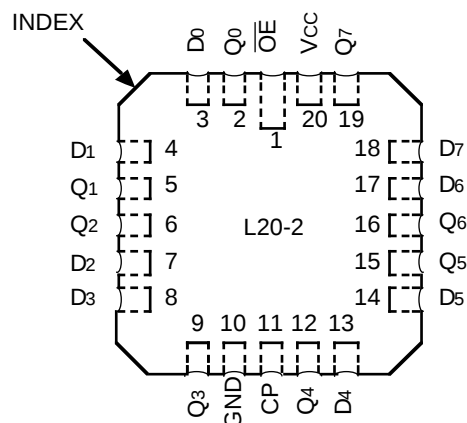
AUGUST 1995

PIN CONFIGURATIONS

IDT54/74FCT374T



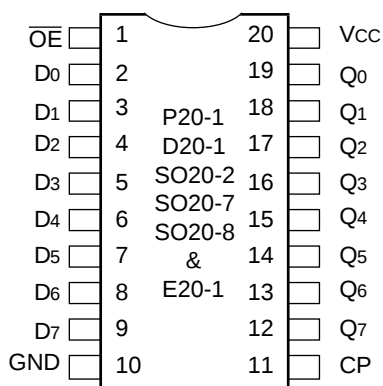
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



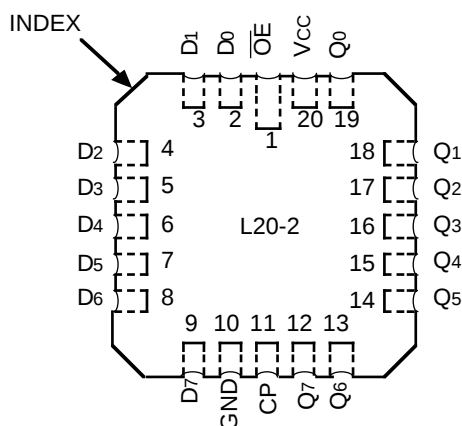
LCC
TOP VIEW

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IDT54/74FCT574T



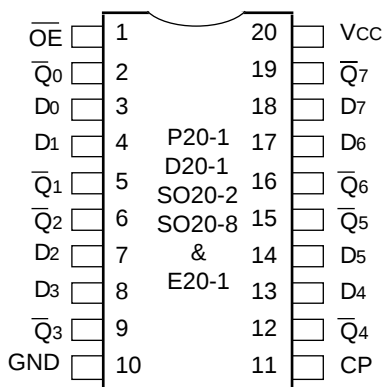
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



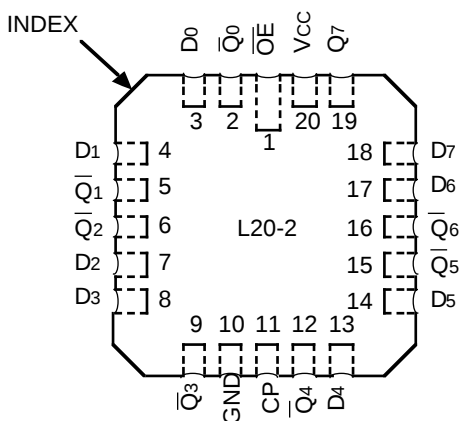
LCC
TOP VIEW

2569 drw 04

IDT54/74FCT534T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

2569 drw 05

PIN DESCRIPTION

Pin Names	Description
DN	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
QN	3-state outputs, (true)
$\overline{Q_N}$	3-state outputs, (inverted)
$\overline{OE}$	Active LOW 3-state Output Enable input

2569 tbl 01

FUNCTION TABLE⁽¹⁾

Function	Inputs			534		374/574	
				Outputs	Internal	Outputs	Internal
	$\overline{OE}$	CP	DN	$\overline{Q_N}$	QN	QN	$\overline{Q_N}$
HI-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
LOAD REGISTER	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

NOTE:

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1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} + 0.5	−0.5 to V _{CC} + 0.5	V
T _A	Operating Temperature	0 to +70	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	−60 to +120	−60 to +120	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT374T/534T/574T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL.}$	2.4	3.3	—	V
			$I_{OH} = -8\text{mA COM'L.}$				
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾		-60	-120	-225	mA

2569 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2374T/2574T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾		16	48	—	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾		-16	-48	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12\text{mA}$	—	0.3	0.50	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾			Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = GND$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			$V_{IN} = 3.4$ $V_{IN} = GND$	FCTxxxT	—	2.0	5.5	
				FCT2xxxT		1.1	4.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = GND$ Eight Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	FCTxxxT	—	3.8	7.3 ⁽⁵⁾	
				FCT2xxxT	—	1.5	4.0 ⁽⁵⁾	
			$V_{IN} = 3.4$ $V_{IN} = GND$	FCTxxxT	—	6.0	16.3 ⁽⁵⁾	
				FCT2xxxT	—	3.8	13.0 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_{HT} = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_{HT}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT374T/534T/574T FCT2374T/2574T				FCT374AT/534AT/574AT FCT2374AT/2574AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to QN ⁽³⁾	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
tpZH tpZL	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
tpHZ tPLZ	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
tsu	Set-up Time HIGH or LOW, DN to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns

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Symbol	Parameter	Conditions ⁽¹⁾	FCT374CT/534CT/574CT FCT2374CT/2574CT				FCT374DT/574DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Q _N ⁽³⁾	CL = 50pF RL = 500Ω	2.0	5.2	2.0	6.2	2.0	4.2	—	—	ns
tpZH tpZL	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.8	—	—	ns
tpHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.7	1.5	4.0	—	—	ns
tsu	Set-up Time HIGH or LOW, D _N to CP		2.0	—	2.0	—	2.0	—	—	—	ns
th	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.0	—	—	—	ns
tw	CP Pulse Width HIGH or LOW ⁽⁴⁾		5.0	—	6.0	—	3.0	—	—	—	ns

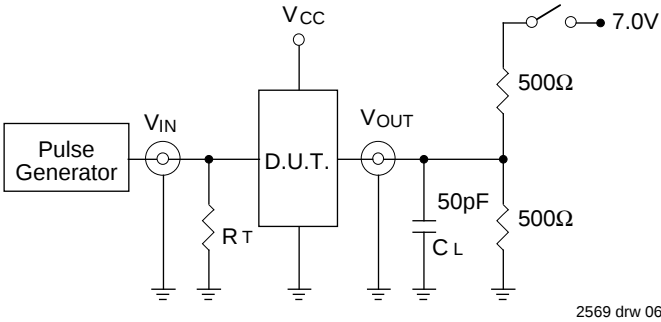
NOTES:

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- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- On for FCT374/2374T and FCT574/2574T, $\overline{O}_N$ for FCT534T.
- This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

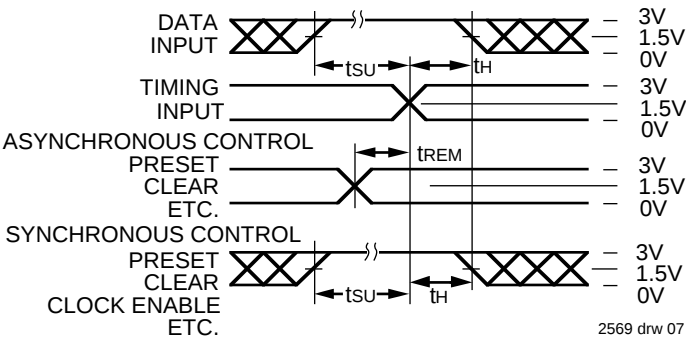


SWITCH POSITION

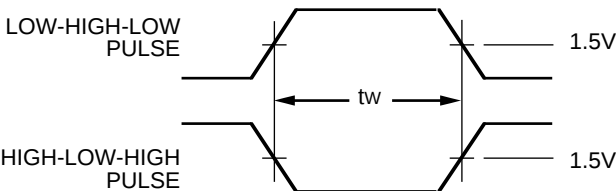
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

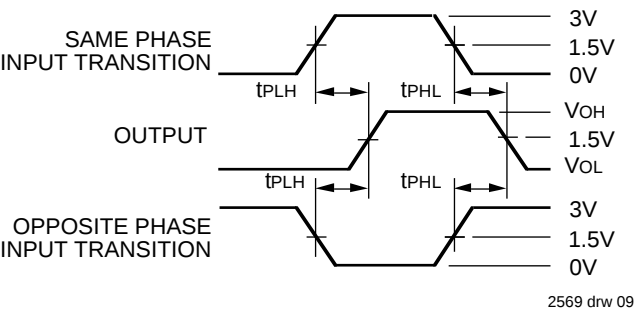
SET-UP, HOLD AND RELEASE TIMES



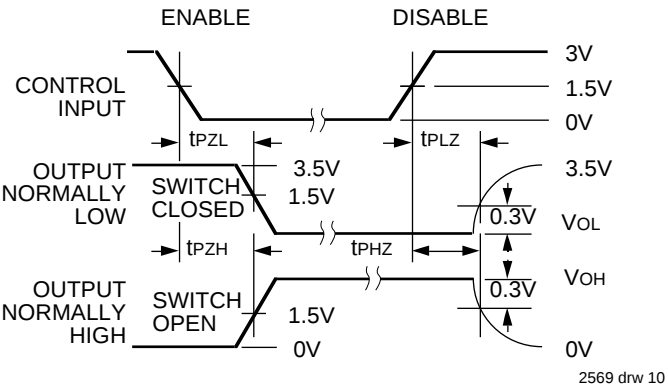
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION

IDT	XX	FCT	X	XXXX	X	X		
Temp. Range	Family	Device Type	Package	Process				
						Blank	Commercial	
						B	MIL-STD-883, Class B	
						P	Plastic DIP	
						D	CERDIP	
						SO	Small Outline IC	
						L	Leadless Chip Carrier	
						E	CERPACK	
						PY	Shrink Small Outline Package	
						Q	Quarter-size Small Outline Package	
						374T	Non-Inverting Octal D Register	
						574T	Non-Inverting Octal D Register	
						534T	Inverting Octal D Register	
						374AT		
						574AT		
						534AT		
						374CT		
						574CT		
						534CT		
						374DT		
						574DT		
						Blank	High Drive	
						2	Balanced Drive	
						54	−55°C to +125°C	
						74	0°C to +70°C	

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