1MSPS, 12-/10-Bit ADCs in 6 Lead SOT-23

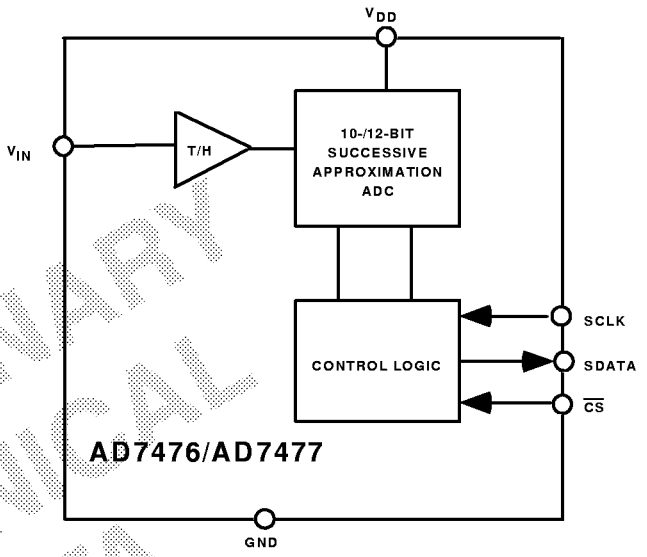
Preliminary Technical Data — AD7476/AD7477

FEATURES

Fast Throughput Rate: 1MSPS
Specified for V_{DD} of 2.35 V to 5.25 V
Low Power:
3.6mW typ at 1MSPS with 3V Supplies
15mW typ at 1MSPS with 5V Supplies
Wide Input Bandwidth:
70dB SNR at 200kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface
SPI/QSPI/µWire/DSP Compatible

Standby Mode: 1µA max
6-Lead SOT-23 Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7476/AD7477 are 12-bit and 10-bit, high speed, low power, successive-approximation ADCs respectively. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates up to 1MSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 1MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7476/AD7477 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. First 10-/12-Bit ADCs in a SOT-23 package.
2. High Throughput with Low Power Consumption
3. Flexible Power/Serial Clock Speed Management
   The conversion rate is determined by the serial clock allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power cunsumption to be reduced when a powerdown mode is used while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 1µA max when in shutdown.
4. Reference derived from the power supply.
5. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

REV. PrH 10/99

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AD7476–SPECIFICATIONS[1] (V_{DD} = +2.35 V to +5.25 V, A Grade: f_{SCLK} = 20MHz, f_{SAMPLE} = 1Msps unless otherwise noted; B Grade: f_{SCLK} = 11MHz, f_{SAMPLE} = 600Ksps unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				F_{IN} = 100kHz Sine Wave A Grade: V_{DD} = (2.7V to 5.25V)[5]
Signal to Noise + Distortion (SINAD)[2]	70	70	dB min	
Signal to Noise Ratio (SNR)[2]	70	70	dB min	
Total Harmonic Distortion (THD)[2]	–76	-76	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	–76	-76	dB max	
Intermodulation Distortion (IMD)[2]				
Second Order Terms	–78	-78	dB typ	
Third Order Terms	–78	-78	dB typ	
Aperture Delay	10	10	ns max	
Aperture Jitter	10	10	ps typ	
Full Power Bandwidth	5	5	MHz typ	@ 3 dB
DC ACCURACY				B Grade, V_{DD} = (2.35V to 3.6V)[6].
Resolution	12	12	Bits	
Integral Nonlinearity[2]		±1.5	LSB max	
	±1.5	±1	LSB typ	
Differential Nonlinearity[2]		±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits.
	±0.9		LSB typ	
Offset Error[2]		±3	LSB max	
	±3		LSB typ	
Gain Error[2]		±3	LSB max	
	±3		LSB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	Volts	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.8	2.8	V min	V_{DD} = 5V
	2.4	2.4	V min	V_{DD} = 3V
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2,3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} -0.2	V_{DD} -0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[2,3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	0.8	1.45	µs max	16 SCLK cycles
Track/Hold Acquisition Time	400	400	ns max	Full-scale step input
	330	400	ns max	Sine wave input <= 100KHz
Throughput Rate	1000	600	KSPS max	Conversion Time + Quiet Time.

AD7476–SPECIFICATIONS[1] (V_{DD} = +2.35 V to +5.25 V, A Grade: f_{SCLK} = 20MHz, f_{SAMPLE} = 1Msps unless otherwise noted; B Grade: f_{SCLK} = 11MHz, f_{SAMPLE} = 600Ksps unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.35/+5.25	+2.35/+5.25	V min/max	
I_{DD}[5]				Digital I/Ps = 0V or V_{DD}.
Normal Mode(Static)	2.1	2.1	mA typ	V_{DD} = 4.75V to 5.25V. SCLK on or off.
	1	1	mA typ	V_{DD} = 2.35V to 3.6V. SCLK on or off.
Normal Mode (Operational)	4	3	mA max	V_{DD} = 4.75V to 5.25V.F_{SAMPLE} =F_{SAMPLE}MAX[7]
	2	1.7	mA max	V_{DD} = 2.35V to 3.6V.F_{SAMPLE} = F_{SAMPLE}MAX[7]
Full Power-Down Mode	1	1	µA max	SCLK on or off.
Power Dissipation[4]				
Normal Mode (Operational)	20	15	mW max	V_{DD} = 5V. F_{SAMPLE} = F_{SAMPLE}MAX[7]
	6	5.1	mW max	V_{DD} = 3V. F_{SAMPLE} = F_{SAMPLE}MAX[7]
Full Power-Down	5	5	µW max	V_{DD} = 5 V.
	3	3	µW max	V_{DD} = 3 V.

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested @ +25°C to ensure compliance.
[4]See POWER VERSUS THROUGHPUT RATE section.
[5] A Grade spec applies as a typical figure when V_{DD} = 2.35V.
[6] B Grade spec applies as a typical figure when V_{DD} = 5.25V.
[7] A Grade: F_{SAMPLE}MAX = 1Msps; B Grade: F_{SAMPLE}MAX = 600Ksps.
Specifications subject to change without notice.

AD7477–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, f_{SCLK} = 20MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD7477[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal to Noise + Distortion (SINAD)	61	dB min	F_{IN} = 100kHz Sine Wave, f_{SAMPLE} = 1Msps
Signal to Noise Ratio (SNR)	61	dB min	F_{IN} = 100kHz Sine Wave, f_{SAMPLE} = 1Msps
Total Harmonic Distortion (THD)	-76	dB max	F_{IN} = 100kHz Sine Wave, f_{SAMPLE} = 1Msps
Peak Harmonic or Spurious Noise (SFDR)	-76	dB max	F_{IN} = 100kHz Sine Wave, f_{SAMPLE} = 1Msps
Intermodulation Distortion (IMD)			
Second Order Terms	-67	dB typ	
Third Order Terms	-67	dB typ	
Aperture Delay	10	ns max	
Aperture Jitter	10	ps typ	
Full Power Bandwidth	5	MHz typ	@ 3 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits.
Offset Error	±1	LSB max	
Gain Error	±1	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	Volts	
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	V_{DD} = 5V
	2.4	V min	V_{DD} = 3V
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2,3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} -0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[2,3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20MHz
Track/Hold Acquisition Time	400	ns max	
Throughput Rate	1	MSPS max	Conversion Time + Quiet Time.
POWER REQUIREMENTS			
V_{DD}	+2.7/+5.25	V min/max	
I_{DD}[5]			Digital I/Ps = 0V or V_{DD}.
Normal Mode(Static)	2.1	mA typ	V_{DD} = 4.75V to 5.25V. SCLK on or off.
	1	mA typ	V_{DD} = 2.7V to 3.6V. SCLK on or off.
Normal Mode (Operational)	4	mA max	V_{DD} = 4.75V to 5.25V. F_{SAMPLE} = 1MSPS
	2	mA max	V_{DD} = 2.7V to 3.6V. F_{SAMPLE} = 1MSPS
Full Power-Down Mode	1	µA max	SCLK on or off.
Power Dissipation[4]			
Normal Mode (Operational)	20	mW max	V_{DD} = 5V. F_{SAMPLE} = 1MSPS
	6	mW max	V_{DD} = 3V. F_{SAMPLE} = 1MSPS
Full Power-Down	5	µW max	V_{DD} = 5 V.

NOTES

[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.

[2]See Terminology.

[3]Sample tested @ +25°C to ensure compliance.

[4]See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +2.35 V to +5.25 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7476/AD7477 A Version	B Version	Units	Description
f_{SCLK}[2]	10	10	kHz min	
	20	11	MHz max	
$t_{CONVERT}$	16* t_{SCLK}	16* t_{SCLK}		t_{SCLK}= 1/f_{SCLK}
			ns max	f_{SCLK} = MHz
t_{quiet}	100	100	ns min	Minimum Quiet Time required between conversions
t_2	10	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[3]	tbd	tbd	ns max	Delay from $\overline{CS}$ Until SDATA 3-State Disabled
t_4[3]	10	10	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4t_{SCLK}	0.4t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4t_{SCLK}	0.4t_{SCLK}	ns min	SCLK High Pulse Width
t_7	10	10	ns min	SCLK to Data Valid Hold Time
t_8[4]	25	25	ns max	SCLK falling Edge to SDATA High Impedance
$t_{power-up}$[5]	1	1.1	µs typ	Power up time from Full Power-down.

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.
[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.
[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5]The power up time quoted, $t_{power-up}$, includes the acquisition of an a.c. signal to within +/-0.5LSB accuracy for the A Grade or a d.c. signal to within +/-0.5LSB accuracy for the B Grade respectively. See Power-up Time section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to 7 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to 7 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial (A, B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
SOT-23 Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	229.6°C/W (SOT23)
θ_{JC} Thermal Impedance	91.99°C/W (SOT23)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7476ART	-40°C to +85°C	±1.5 typ	RT-6	CEA
AD7476BRT	-40°C to +85°C	±1.5 max	RT-6	CEB
AD7477ART	-40°C to +85°C	±1 max	RT-6	CFA

NOTES

[2]RT = SOT-23.

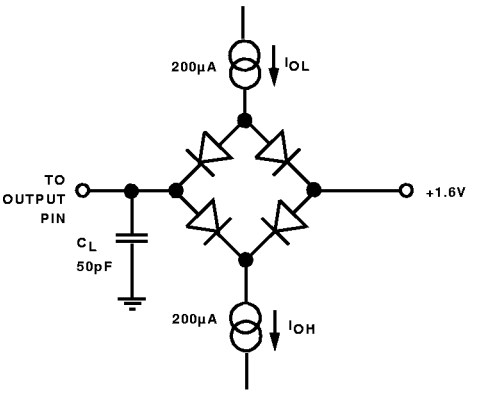


Figure 1. Load Circuit for Digital Output Timing Specifications

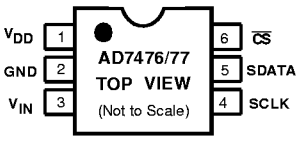
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7476/AD7477 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
6	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476/AD7477 and also frames the serial data transfer.
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7476/AD7477 is from +2.35V to +5.25V.
2	GND	Analog Ground. Ground reference point for all circuitry on the AD7476/AD7477. All analog input signals and any external reference signal should be referred to this GND voltage.
3	VIN	Analog Input. Single-ended analog input channel. The input range is 0 to V_{DD}.
5	SDATA	Data Out. Logic Output. The conversion result from the AD7476/AD7477 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476/AD7477's conversion process.

AD7476/AD7477 PINCONFIGURATION SOT-23



TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode at the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See serial interface timing section for more details.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter this is 62dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7476/AD7477, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7476/AD7477 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

AD7476/AD7477 PERFORMANCE CURVES

Figure 2 shows a typical FFT plot for the AD7476/ AD7477 at 1MHz sample rate and 100kHz input frequency.

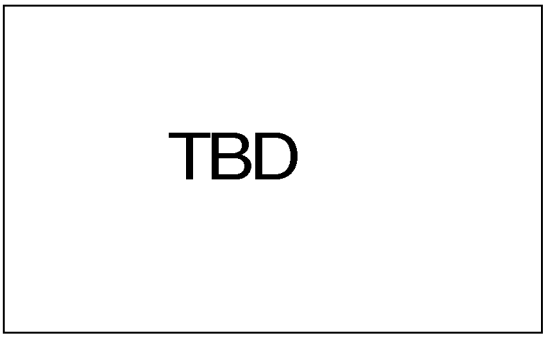


Figure 2. AD7476 Dynamic Performance

Figure 3 shows the SNR versus frequency for a 5V supply.

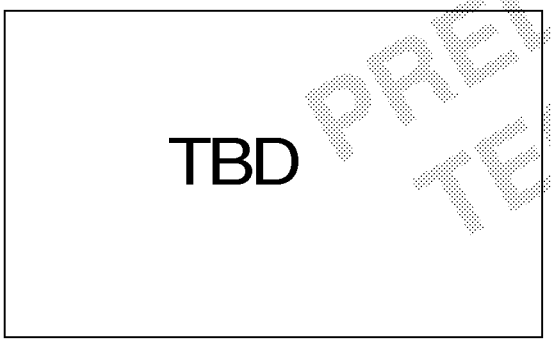


Figure 3. AD7476 SNR vs Input Frequency

CIRCUIT INFORMATION

The AD7476/AD7477 are fast, micro-power, 12-bit and 10-Bit, single supply, A/D converters respectively. The parts can be operated from a +3V (+2.7V to +3.6V) supply or from a +5V (+4.75V to +5.25V) supply. When operated from either a +5V supply or a 3V supply, the AD7476/ AD7477 are capable of throughput rates of 1Msps when provided with a 20MHz clock.

The AD7476/AD7477 provide the user with an on-chip track/hold, A/D converter, and a serial interface housed in a tiny 6-pin SOT-23 package, which offers the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to V_{DD} . An external reference is not required for the ADC and neither is there a reference on-chip. The reference for the AD7476/AD7477 is derived from the power supply and thus gives the widest dynamic input range.

The AD7476/AD7477 also feature a power-down option to allow power saving between conversions. The power-down feature is implemented across the standard serial interface as described in the "Modes of Operation" section.

CONVERTER OPERATION

The AD7476/AD7477 is a successive approximation analog-to -digital converter based around a charge redistribution DAC. Figures 4 and 5 show simplified schematics of the ADC. Figure 4 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

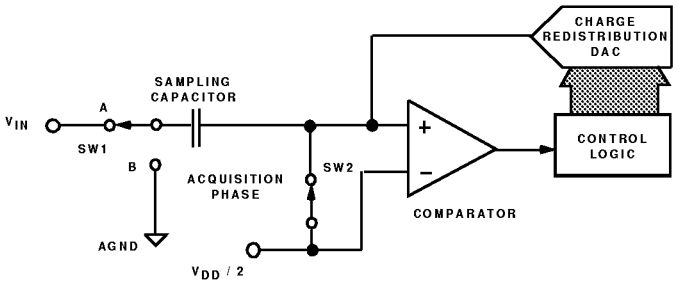


Figure 4. ADC Acquisition Phase

When the ADC starts a conversion, see figure 5, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 6 shows the ADC transfer function.

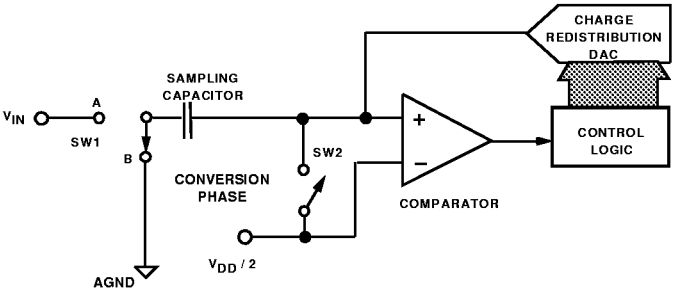


Figure 5. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7476/AD7477 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1LSB, 2LSBs, etc.). The LSB size is = $V_{REF}/4096$. The ideal transfer characteristic for the AD7476/AD7477 is shown in figure 6 below.

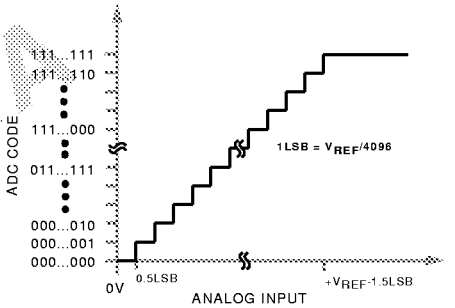


Figure 6. AD7476/AD7477 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 7 shows a typical connection diagram for the AD7476/AD7477. V_{REF} is taken internally from V_{DD} and as such V_{DD} should be well decoupled. This provides an analog input range of 0V to V_{DD}. The conversion result is output in a 16-bit word with four leading zeroes followed by the MSB of the 12-bit or 10-bit result. The 10-bit result from the AD7477 will be followed by two trailing zeroes.

Alternatively, because the supply current required by the AD7476/AD7477 is so low, a presision reference can be used as the supply source to the AD7476/AD7477. A REF19x voltage reference (REF195 for 5V or REF193 for 3V) can be used to supply the required voltage to the ADC - see figure 7. This configuration is especially useful if your power supply is quite noisy or if the system supply voltages are at some value other than 5V or 3V (e.g. 15V). The REF19x will output a steady voltage to the AD7476/ AD7477. If the low dropout REF193 is used, the current it needs to supply to the AD7476/AD7477 is typically

1mA. When the ADC is converting at a rate of 1Msps the REF193 will need to supply a maximum of 2mA to the AD7476/ASD7477. The load regulation of the REF193 is typically 10 ppm/mA (V_S = 5V), which results in an error of 20ppm (100µV) for the 2mA drawn from it. This corresponds to a 0.08 LSB error. For applications where power consumption is of concern, the power down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See Modes of Operation section of the datasheet.

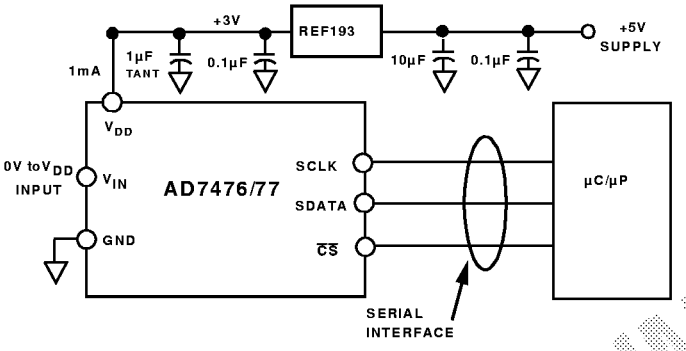


Figure 7. REF193 as Power Supply to AD7476/AD7477

Table I provides some typical performance data for various references as a V_{DD} source.

Table I

TBD

Analog Input

Figure 8 shows an equivalent circuit of the analog input sturcture of the AD7476/ASD7477. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 20mA is the maximum current these diodes can conduct without causing irreversable damage to the part. The capacitor C1 in figure 8 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 16pF typically.For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 9 shows a graph of the total harmonic distortion versus analog input signal frequency for different source impedances.

TBD

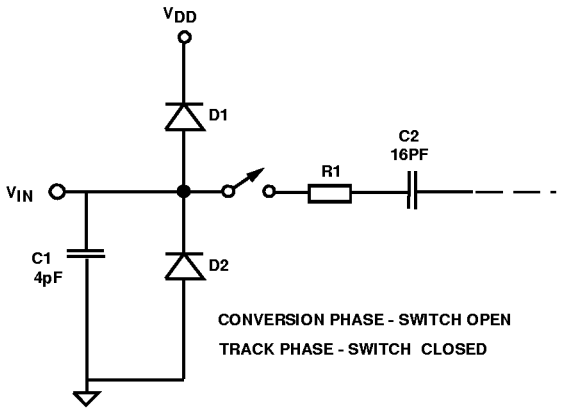


Figure 8. Equivalent Analog Input Circuit

Digital Inputs

The digital inputs applied to the AD7476/AD7477 are not limited by the maximum ratings which limit the analog inputs. Instead, the digitals inputs applied can go to 7V and are not restricted by the V_{DD} + 0.3V limit as on the analog inputs. For example, if the AD7476/AD7477 were operated with a V_{DD} of 3V then 5V logic levels could be used on the digital inputs. However it is important to note that the data output on SDATA will still have 3v logic levels when V_{DD} = 3V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3V was applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7476/AD7477 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion . There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether the AD7476/ AD7477 will enter Power-down Mode or not. Similarly, if already in Power-down then $\overline{CS}$ can control whether the device will return to Normal operation or remain in Power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/ throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7476/AD7477 remaining fully-powered all the time. Figure 10 shows the general diagram of the operation of the AD7476/AD7477 in this mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge the part will remain powered up but the conversion will be terminated and SDATA will go back into tri-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to tri-state), another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing $\overline{CS}$ low again.

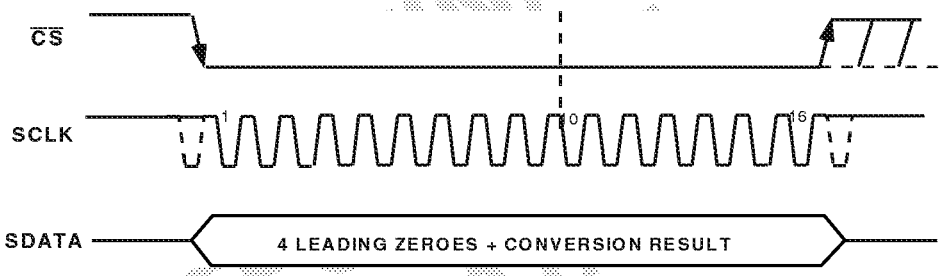


Figure 10. Normal Mode Operation

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7476/AD7477 is in power down, all analog circuitry is powered down.

To enter Power-Down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 11. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will enter power down and the conversion that was intiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into tri-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then the part will remain in Normal Mode and will not power-down. This will avoid accidental powerdown due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7476/AD7477 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device will be fully powered up once 16 SCLKs have elapsed and valid data will result from the next conversion as shown in figure 12. If $\overline{CS}$ is brought high before the tenth falling edge of SCLK, then the AD7476/AD7477 will go back into power down again. This avoids accidental power up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$ as long as it occurs before the tenth SCLK falling edge.

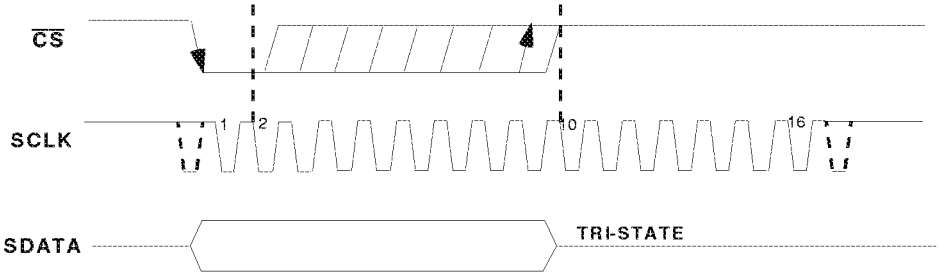


Figure 11. Entering Power Down Mode

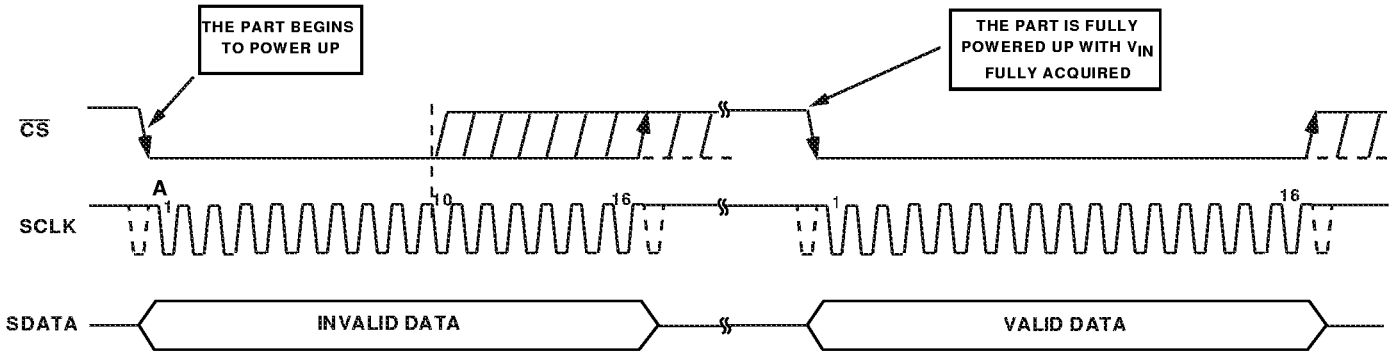


Figure 12. Exiting Power Down Mode

Power-up Time

The power-up time of the AD7476/AD7477 is typically 1µs, which means that with any frequency of SCLK up to 20MHz, one dummy cycle will always be sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC will be fully powered up and the signal will be acquired properly. The quite time t_{quiet} must still be allowed from the point where the bus goes back into tristate after the dummy conversion, to the next falling edge of $\overline{CS}$. When running at 1Msps throughput rate, the AD7476/AD7477 will power up and acquire an a.c. signal within +/- 0.5LSB in one dummy cycle, i.e. 1µs. To power up and acquire a d.c. signal within +/-0.5LSB accuracy, 1µs will not be sufficient. Instead approximately 1.1µs is necessary. However if the AD7476/AD7477 is being used in a d.c. application and a B-grade device is used, then a dummy cycle at the maximum throughput rate of 600Ksps will be more than adequate to allow power-up and full acquisition of the d.c. signal to +/- 0.5LSB accuracy.

When powering up from the power-down mode with a dummy cycle, as in figure 12, the track and hold which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as point A in figure 12. Although at any SCLK frequency one dummy cycle is sufficient to power the device up and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1µs will be sufficient to power the device up and acquire the input signal.If for example, a 5MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2µs. In one dummy cycle, 3.2µs, the part would be powered up and V_{IN} acquired fully. However after 1 µs with a 5MHz SCLK only 5 SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case the $\overline{CS}$ can be brought high after the tenth SCLK falling edge and brought low again after a time t_{quiet} to initiate the conversion.

When power supplies are first applied to the AD7476/AD7477, the ADC can either power up in the power-down mode or normal mode. Because of this it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the power-down mode while not in use and the user wishes the part to power up in power-down mode, then the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in figure 11. Once supplies are applied to the AD7476/AD7477, the power up time is the same as that when powering up from the power-down mode. It takes approximately 1µs to power up fully if the part powers up in normal mode. It is not necessary to wait 1 µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion care must be taken to ensure that adequate acquisition time has been allowed. Upon initial power-up the track and hold will already be in track mode so a dummy conversion is not required.

SERIAL INTERFACE

Figure 13 and Figure 14 show the detailed timing diagram for serial interfacing to the AD7476 and the AD7477 respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7476/AD7477 during conversion.

$\overline{CS}$ initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of tristate and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, then the track and hold will go back into track on the next SCLK rising edge as shown in figure 13 and 14 at point B. On the 16th SCLK falling edge the SDATA line will go back into tristate . If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into tri-state, otherwise SDATA returns to tri-state on the 16th SCLK falling edge as shown in Figure 13 and Figure 14. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476/AD7477. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero, thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge, i.e. the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the first leading zero provided and the 15th rising SCLK edge would have DB0 provided.

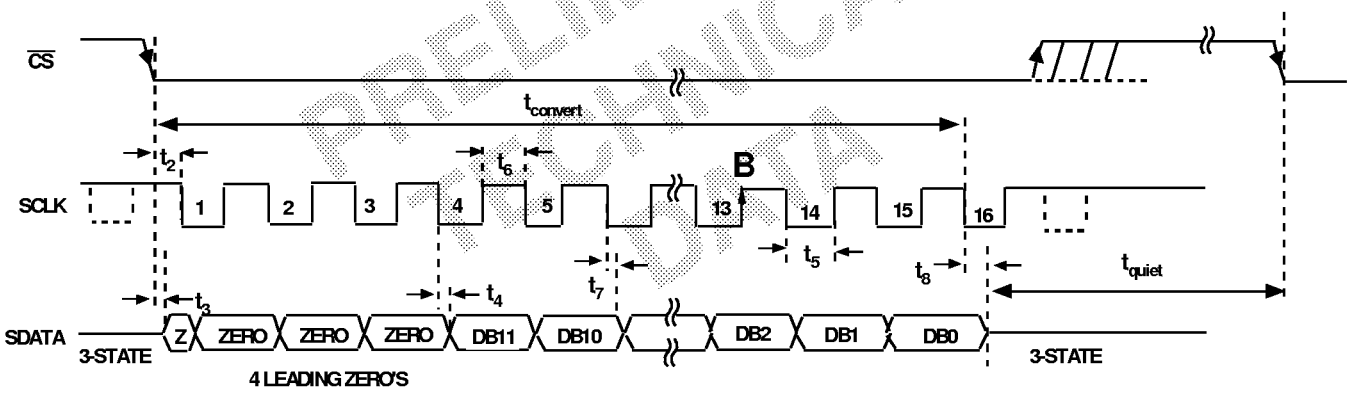


Figure 13. AD7476 Serial Interface Timing Diagram

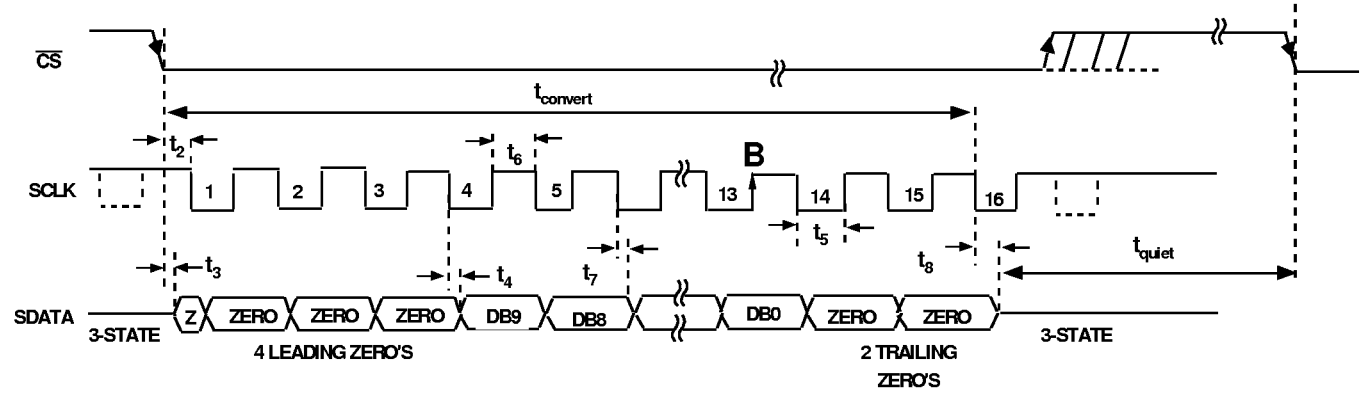


Figure 14. AD7477 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7476/AD7477 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7476/AD7477 with some of the more common microcontroller and DSP serial interface protocols.

AD7476/AD7477 to TMS320C5xC54x

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7476/AD7477. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x and the AD7476/AD7477 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The format bit, FO, may be set to 1 to set the word length to 8-bits, in order to implement the power-down mode on the AD7476/AD7477.
The connection diagram is shown in Figure 15. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C5x/C54x will provide equidistant sampling.

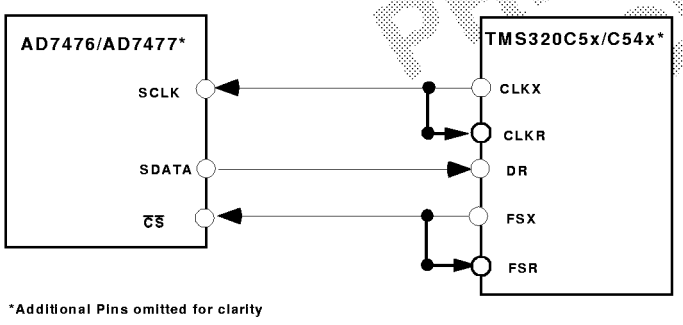


Figure 15. Interfacing to the TMS320C5x

AD7476/AD7477 to ADSP21xx

The ADSP21xx family of DSPs are interfaced directly to the AD7476/AD7477 without any glue logic required. The SPORT control register should be set up as follows:
TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data words
ISCLK = 1, Internal serial clock
TFSR = RFSR = 1, Frame every word
IRFS = 0,
ITFS = 1.
To implement the power-down mode SLEN should be set to 1001 to issue an 8-bit SCLK burst.
The connection diagram is shown in Figure 16. The ADSP21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The Frame synchronisation signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be acheived.

The Timer registers etc. are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instrustion to transmit with TFS is given, (i.e. AX0=TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP2111 has a master clock frequency of 16MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2MHz is obtained, and 8 master clock periods will elapse for every 1 SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N then equidistant sampling will be implemented by the DSP.

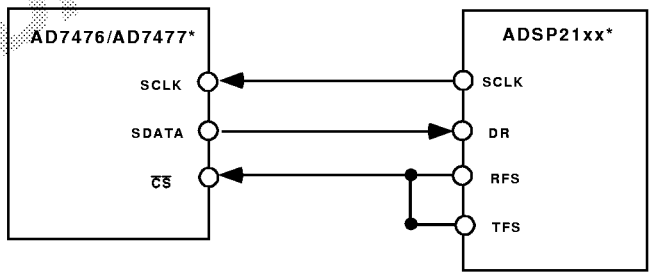


Figure 16. Interfacing to the ADSP-21xx

AD7476/AD7477 to DSP56xxx

The connection diagram in figure 17 shows how the AD7476/AD7477 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB =1) with internally generated 1-bit clock period frame sync for both TX and RX (bits FSL1 =1 and FSL0 =0 in CRB). Set the word length to 16 by setting bits WL1 =1 and WL0 = 0 in CRA. To implement the power-down mode on the AD7476/AD7477 then the word length can be changed to 8 bits by setting bits WL1 = 0 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP56xxx will provide equidistant sampling.

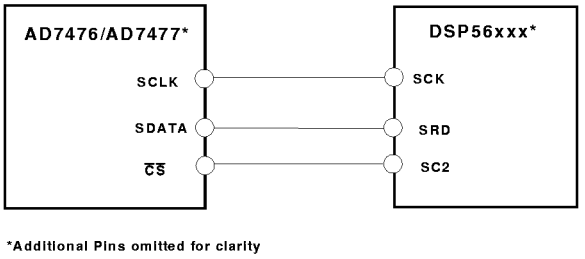


Figure 17. Interfacing to the DSP56xx

AD7476/AD7477 to MC68HC16

The Serial Peripheral Interface (SPI) on the MC68HC16 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 1 and the Clock Phase Bit (CPHA) = 0. The SPI is configured by writing to the SPI Control Register (SPCR) - see 68HC16 user manual. The serial transfer will take place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. To implement the power-down mode with an 8-bit transfer set SIZE = 0. A connection diagram is shown in figure 18.

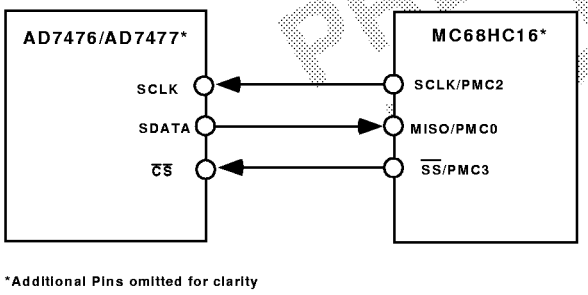


Figure 18. Interfacing to the MC68HC16

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-lead SOT23 (RT-6)