

MNLM2941-X REV 4A1

Original Creation Date: 03/21/97

Last Update Date: 05/04/01

Last Major Revision Date: 04/20/01

LOW DROPOUT ADJUSTABLE REGULATOR
General Description

The LM2941 positive voltage regulator features the ability to source 1A of output current with a typical dropout voltage of 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground pin current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{in} - V_{out} \leq 3V$).

Designed also for vehicular applications, the LM2941 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Industry Part Number

LM2941

Prime Die

LM2941

NS Part Numbers

LM2941J-MLS
LM2941J-QMLV
LM2941J/883
LM2941WG-QMLV
LM2941WG/883

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp Description		Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Output voltage adjustable from 5V to 20V
- Dropout voltage typically 0.5V @ $I_o = 1A$
- Output current in excess of 1A
- Trimmed reference voltage
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- TTL, CMOS compatible ON/OFF switch
- CONTROLLING DOCUMENT

LM2941J-QMLV 5962-9166701VEA

LM2941J/883 5962-9166701QEA

LM2941WG-QMLV 5962-9166701VYA

LM2941WG/883 5962-9166701QYA

(Absolute Maximum Ratings)

(Note 1)

Input Voltage (Survival Voltage $\leq 100\text{ms}$)	60V
Internal Power Dissipation (Note 2, 3)	Internally Limited
Maximum Junction Temperature	150 C
Storage Temperature Range	$-65\text{ C} \leq \text{TA} \leq +150\text{ C}$
Lead Temperature (Soldering, 10 seconds)	300 C
Thermal Resistance	
ThetaJA	
CERDIP (Still Air)	73 C/W
CERDIP (500LF/Min Air Flow)	37 C/W
CERAMIC SOIC (Still Air)	122 C/W
CERAMIC SOIC (500LF/Min Air Flow)	77 C/W
ThetaJC	
CERDIP	3 C/W
CERAMIC SOIC	5 C/W
Package Weight (Typical)	
CERDIP	1970mg
CERAMIC SOIC	360mg
ESD Susceptibility (Note 4)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{j\text{max}}$ (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{d\text{max}} = (T_{j\text{max}} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 4: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

(Note 1)

Input Voltage

26V

Operating Temperature Range

$-55\text{ }^{\circ}\text{C} \leq T_A \leq +125\text{ }^{\circ}\text{C}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $5V \leq V_o \leq 20V$, $V_{in} = V_o + 5V$, $C_{out} = 22\mu F$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
V _{ref}	Reference Voltage	$5mA \leq I_o \leq 1A$			1.237	1.313	V	1
					1.211	1.339	V	2, 3
V _{rline}	Line Regulation	$V_o + 2V \leq V_{in} \leq 26V$, $I_o = 5mA$	3			10	mV/V	1, 2, 3
V _{rload}	Load Regulation	$50mA \leq I_o \leq 1A$	3			10	mV/V	1, 2, 3
I _q	Quiescent Current	$V_o + 2V \leq V_{in} \leq 26V$, $I_o = 5mA$				15	mA	1
						20	mA	2, 3
		$V_{in} = V_o + 5V$, $I_o = 1A$				45	mA	1
						60	mA	2, 3
V _{do}	Dropout Voltage	$I_o = 1A$				0.8	V	1
						1.00	V	2, 3
		$I_o = 100mA$				200	mV	1
						300	mV	2, 3
I _{sc}	Short Circuit Current	$V_{in} \text{ max} = 26V$			1.6	3.5	A	1
					1.3	3.7	A	2, 3
	Maximum Operational Input Voltage		2			26	V _{dc}	1, 2, 3
	Reverse Polarity DC Input Voltage	$R_o = 100 \text{ Ohms}$, $V_o \geq -0.6V$	1		-15		V	1, 2, 3
V(T ₀)	ON/OFF Threshold Voltage ON	$I_o \leq 1A$	1			0.8	V	1, 2, 3
V(T ₀)	ON/OFF Threshold Voltage OFF	$I_o \leq 1A$	1		2.00		V	1, 2, 3
	ON/OFF Threshold Current	$V \text{ ON/OFF} = 2.0V$, $I_o \leq 1A$				100	uA	1
						300	uA	2, 3

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $5V \leq V_o \leq 20V$, $V_{in} = V_o + 5V$, $C_{out} = 22\mu F$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
	Maximum Line Transient	V_o max 1V above nominal V_o , $R_o = 100\ \Omega$, $T \leq 100mS$			60		V	4, 5, 6
	Reverse Polarity Transient Input Voltage	$T \leq 100mS$, $R_o = 100\ \Omega$			-50		V	4, 5, 6
RR	Ripple Rejection	$f_o = 1KHz$, $1\ V_{rms}$, $I_L = 100mA$	4			0.02	%/V	4
			4			0.04	%/V	5, 6

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $5V \leq V_o \leq 20V$, $V_{in} = V_o + 5V$, $C_{out} = 22\mu F$. "Delta Calculations performed on JAN S and QMLV devices at Group B, Subgroup 5 ONLY"

V_{ref}	Reference Voltage	$5mA \leq I_o \leq 1A$			-25	+25	mV	1
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Note 1: Functional test go no go only.

Note 2: Condition for V_{in} .

Note 3: Limit = mV per Volt of V_{out} .

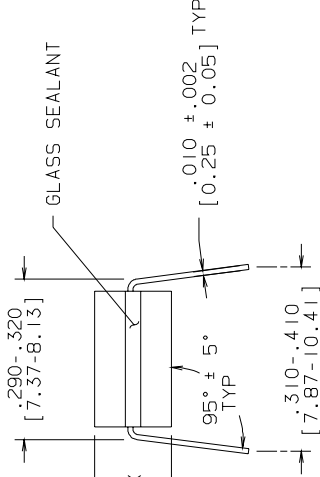
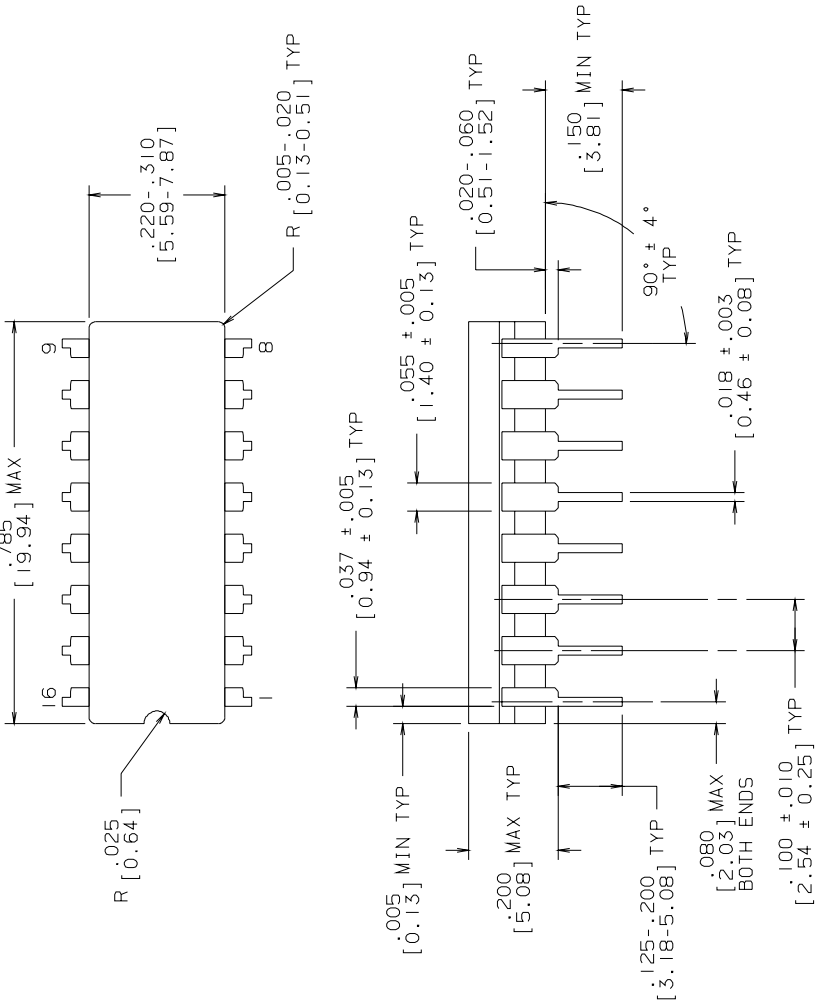
Note 4: %/V = % of V_{in} per Volt of V_{out} .

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06333HRA2	CERDIP (J), 16 LEAD (B/I CKT)
06352HRA1	CERPACK (W), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
P000158A	CERDIP (J), 16 LEAD (PINOUT)
P000378A	CERAMIC SOIC, 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

R E V I S I O N S				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/

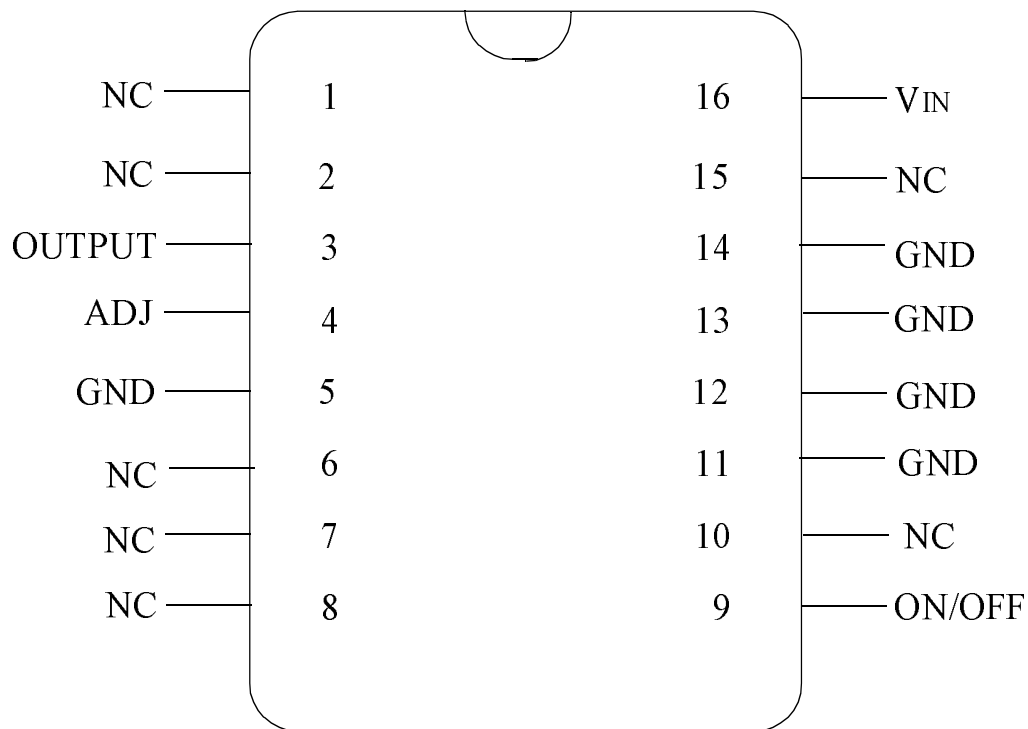


MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH				
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION		
DRAWN LEQUANG	09/15/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090		
DFTG. CHK.		CERDIP (J), 16 LEAD		
ENGR. CHK.				
APPROVAL				
 PROJECTION INCH [MM]	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J16A	L
DO NOT SCALE DRAWING		SHEET	1	OF 1

- NOTES: UNLESS OTHERWISE SPECIFIED
1. LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
 2. JEDEC REGISTRATION M0-036, VARIATION AD, DATED 04/1981.

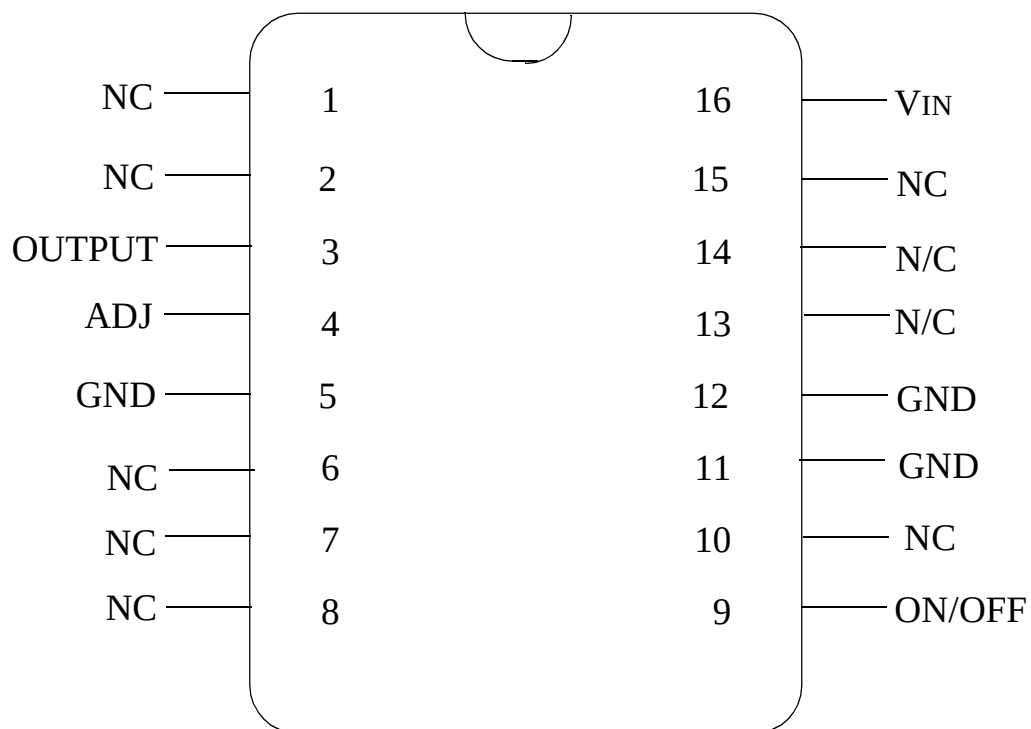


LM2941J/883
16 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000158A



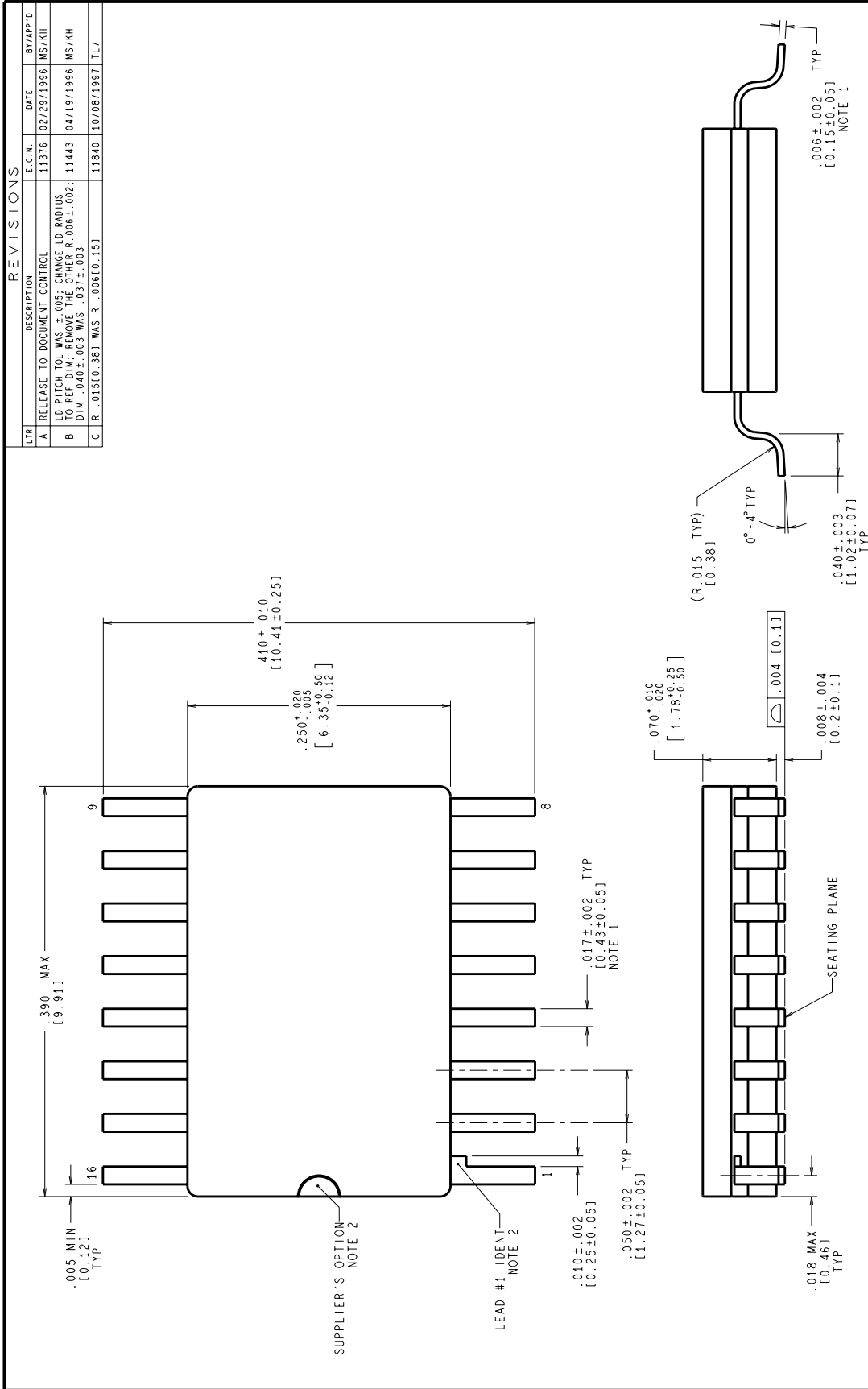
National Semiconductor™

MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050



LM2941WG
16 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000378A

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996
B	LD PITCH TOL WAS $\pm .005$; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R .006 $\pm .002$; DIM .040 $\pm .003$ WAS $.037 \pm .003$	11443	04/19/1996
C	R .015(0.38) WAS R .006(0.15)	11840	10/08/1997



NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASE METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

MIL-PRF-38535 CONFIGURATION CONTROL

APPROVALS	DATE	SCALE	SIZE	DRAWING NUMBER	REV
DESIGN MARTY SUCHY	02/29/96	N/A	C	(SC)MKT-WG16A	C
ENGINEER CHK.					
TESTER CHK.					
PROJECTION 					
DO NOT SCALE DRAWING SHEET 1 of 1					

National Semiconductor
2000 Semiconductor Dr., Santa Clara, CA 95052-8000

**CERPACK,
16 LEAD,
GULL WING**

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0001075	02/11/99	Barbara Lopez	Initial Release of: MNLM2941-X Rev. 0A0. Added note for power dissipation and reference to thermal resistance for Aluminum Nitride package.
1A1	M0003224	10/08/99	Rose Malone	Update MDS: MNLM2941-X, Rev. 0A0 to MNLM2941-X, Rev. 1A1.
2A1	M0003559	11/28/00	Rose Malone	Update MDS: MNLM2941-X, Rev. 1A1 to MNLM2941-X, Rev. 2A1. Changed V _{do} , I _o = 100mA, Max. condition subgroups to Subgroup 1 at 200mV and Subgroup 2 and 3 at 300mV.
2B1	M0003777	01/31/01	Rose Malone	Update MDS: MNLM2941-X, Rev. 2A1 to MNLM2941-X, Rev. 2B1. Added MLS part number reference to Main Table.
3A1	M0003783	05/04/01	Rose Malone	Update MDS: MNLM2941-X, Rev. 2B1 to MNLM2941-X, Rev. 3A1. Changed Electrical Section DC parameter I _{sc} Max limit Subgroup 1 from 3.3A to 3.5A and Subgroups 2, 3 from 3.5A to 3.7A
4A1	M0003801	05/04/01	Rose Malone	Update MDS: MNLM2941-X, Rev. 3A1 to MNLM2941-X, Rev. 4A1. Removed on Main Table, Feature Section and Graphics Section reference to K pkg. Added Main Table, Feature Section reference to WG pkg and Drift Value Parameter to Electrical Section.