NTTS2P02R2

Power MOSFET
-2.4 Amps, -20 Volts

Single P−Channel Micro8™

ON Semiconductor®

http://onsemi.com

−2.4 AMPERES
−20 VOLTS
$R_{DS(on)}$ = 90 mΩ

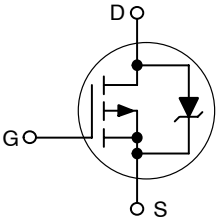
Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Micro−8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided
- Pb−Free Package is Available

Applications

- Power Management in Portable and Battery−Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

Single P−Channel



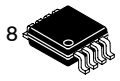
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−20	V
Gate−to−Source Voltage − Continuous	V_{GS}	±8.0	V
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 70°C Pulsed Drain Current (Note 3)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	160 0.78 −2.4 −1.92 −20	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 70°C Pulsed Drain Current (Note 3)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	88 1.42 −3.25 −2.6 −30	°C/W W A A A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −20 Vdc, V_{GS} = −4.5 Vdc, Peak I_L = −5.0 Apk, L = 28 mH, R_G = 25 Ω)	EAS	350	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

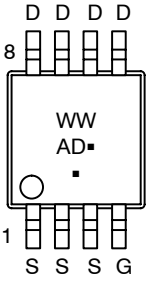
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR−4 or G−10 PCB, Steady State.
2. Mounted onto a 2″ square FR−4 Board (1 IN SQ, 2 oz Cu 0.06″ thick single sided), Steady State.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MARKING DIAGRAM & PIN ASSIGNMENT



Micro8
CASE 846A
STYLE 1



AD = Specific Device Code
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTS2P02R2	Micro8	4000/Tape & Reel
NTTS2P02R2G	Micro8 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 4)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	−20 –	– −12.7	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = −16 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = −16 Vdc, T_J = 125°C)		I_{DSS}	– –	– –	−1.0 −25	μAdc
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = −20 Vdc, T_J = 25°C)		I_{DSS}	–	–	−5.0	μAdc
Gate−Body Leakage Current (V_{GS} = −8 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	−100	nAdc
Gate−Body Leakage Current (V_{GS} = +8 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	−0.5 –	−0.90 2.5	−1.4 –	Vdc mV/°C
Static Drain−to−Source On−State Resistance (V_{GS} = −4.5 Vdc, I_D = −2.4 Adc) (V_{GS} = −2.7 Vdc, I_D = −1.2 Adc) (V_{GS} = −2.5 Vdc, I_D = −1.2 Adc)		$R_{DS(on)}$	– – –	0.070 0.100 0.110	0.090 0.130 –	Ω
Forward Transconductance (V_{DS} = −10 Vdc, I_D = −1.2 Adc)		g_{FS}	2.0	4.2	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	550	–	pF
Output Capacitance		C_{oss}	–	200	–	
Reverse Transfer Capacitance		C_{rss}	–	100	–	
SWITCHING CHARACTERISTICS (Notes 5 & 6)						
Turn−On Delay Time	(V_{DD} = −10 Vdc, I_D = −2.4 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	10	–	ns
Rise Time		t_r	–	31	–	
Turn−Off Delay Time		$t_{d(off)}$	–	33	–	
Fall Time		t_f	–	29	–	
Turn−On Delay Time	(V_{DD} = −10 Vdc, I_D = −1.2 Adc, V_{GS} = −2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	15	–	ns
Rise Time		t_r	–	40	–	
Turn−Off Delay Time		$t_{d(off)}$	–	35	–	
Fall Time		t_f	–	35	–	
Total Gate Charge	(V_{DS} = −16 Vdc, V_{GS} = −4.5 Vdc, I_D = −2.4 Adc)	Q_{tot}	–	10	18	nC
Gate−Source Charge		Q_{gs}	–	1.5	–	
Gate−Drain Charge		Q_{gd}	–	5.0	–	
BODY−DRAIN DIODE RATINGS (Note 5)						
Diode Forward On−Voltage	(I_S = −2.4 Adc, V_{GS} = 0 Vdc) (I_S = −2.4 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	– –	−0.88 −0.75	−1.0 –	Vdc
Reverse Recovery Time	(I_S = −2.4 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	–	37	–	ns
		t_a	–	16	–	
		t_b	–	21	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.025	–	μC

4. Handling precautions to protect against electrostatic discharge are mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

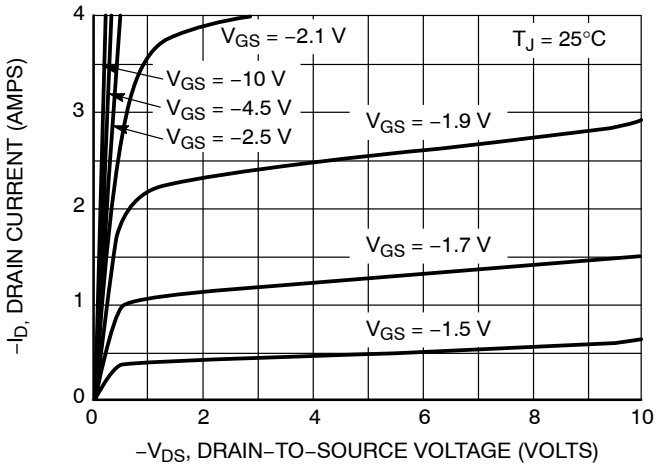


Figure 1. On−Region Characteristics.

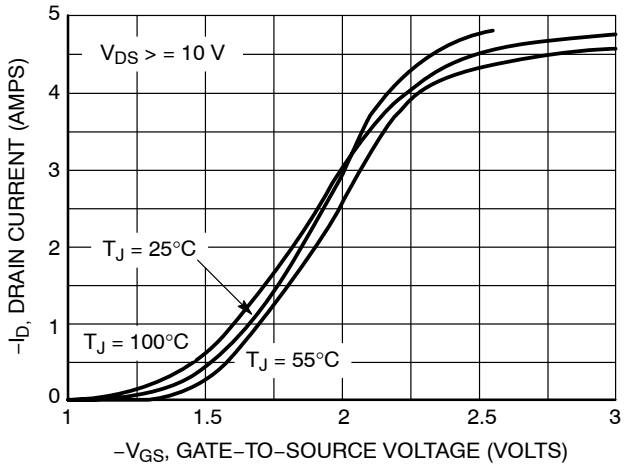


Figure 2. Transfer Characteristics.

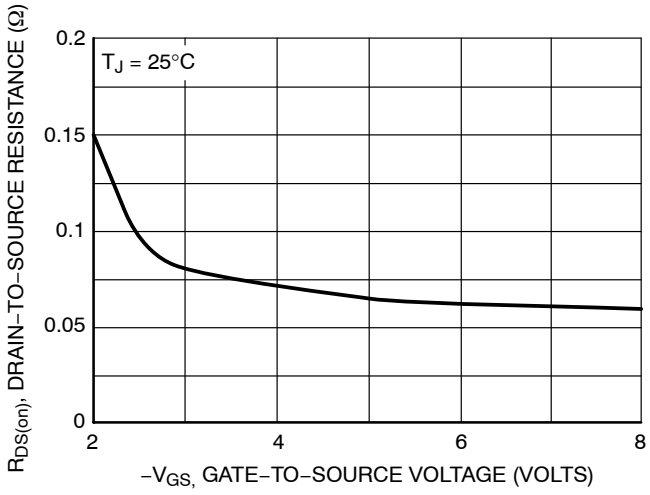


Figure 3. On−Resistance vs. Gate−to−Source Voltage.

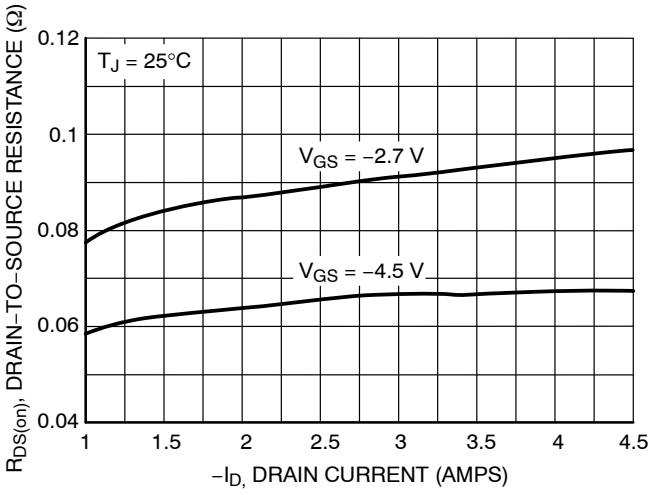


Figure 4. On−Resistance vs. Drain Current and Gate Voltage.

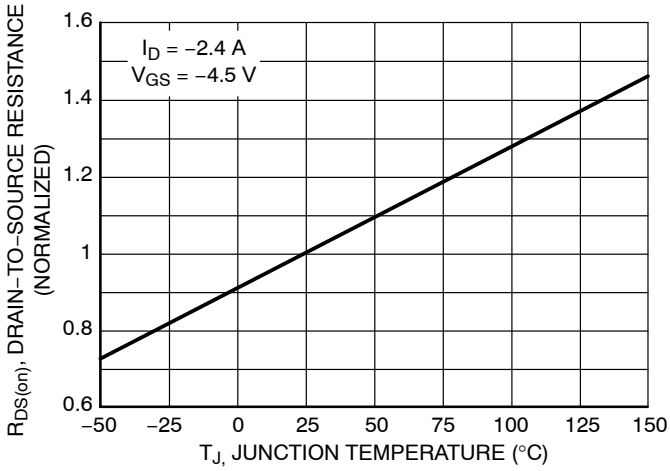


Figure 5. On−Resistance Variation with Temperature.

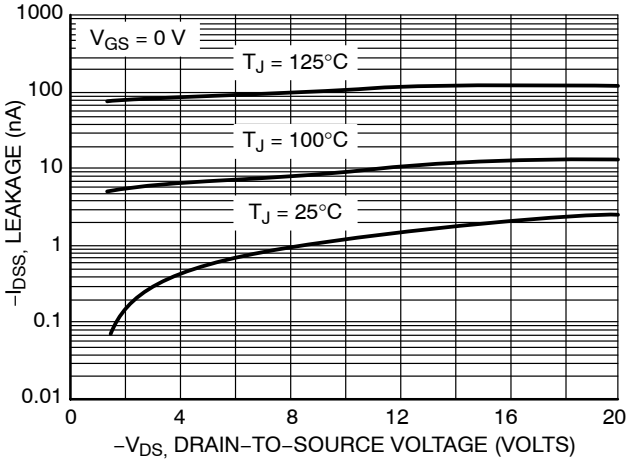


Figure 6. Drain−to−Source Leakage Current vs. Voltage.

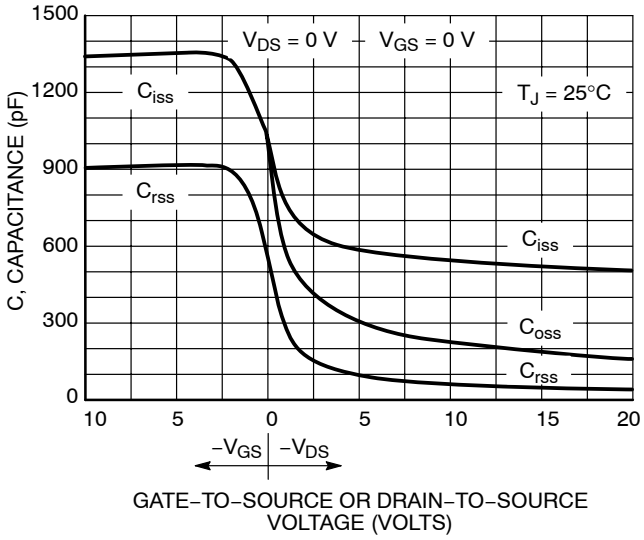


Figure 7. Capacitance Variation

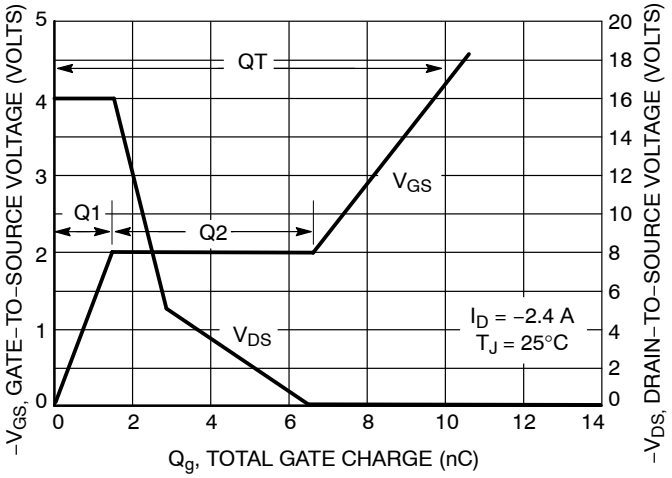


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

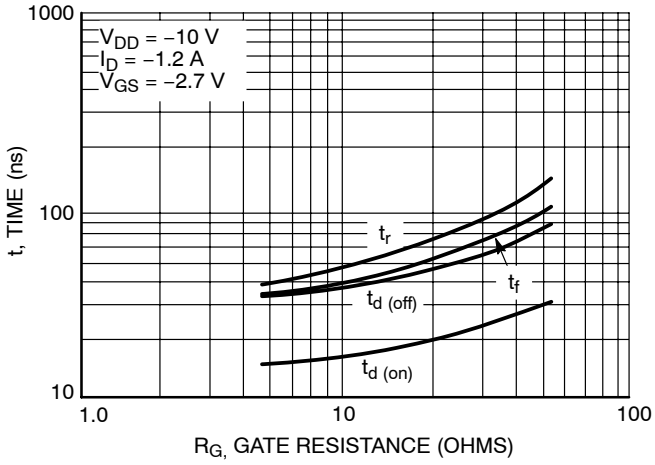


Figure 9. Resistive Switching Time Variation versus Gate Resistance

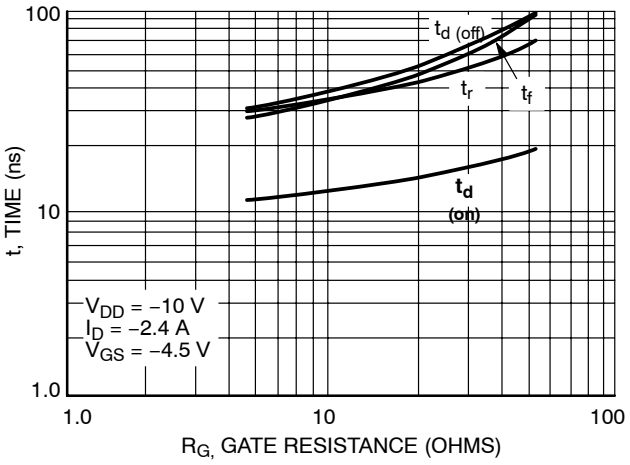


Figure 10. Resistive Switching Time Variation versus Gate Resistance

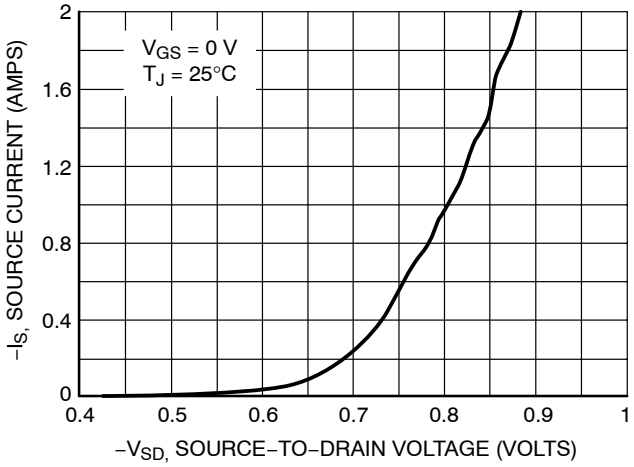


Figure 11. Diode Forward Voltage versus Current

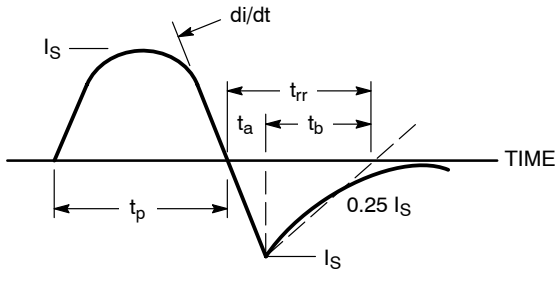


Figure 12. Diode Reverse Recovery Waveform

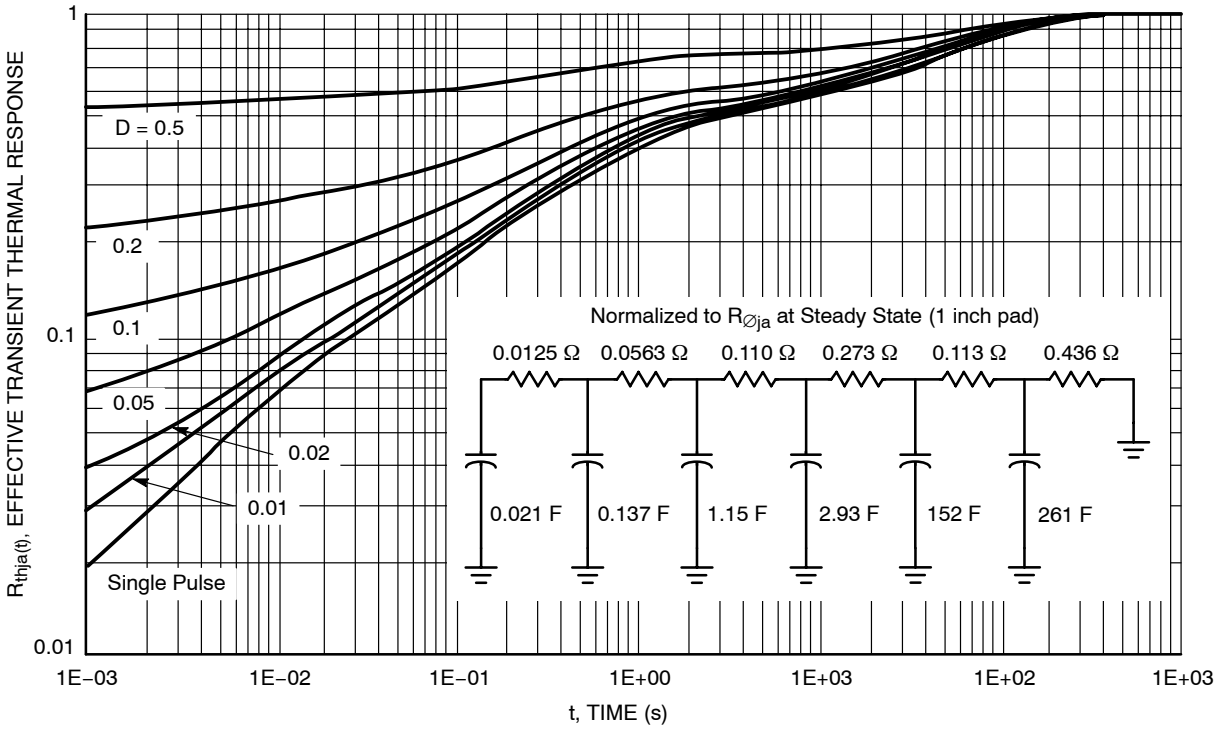


Figure 13. FET Thermal Response.

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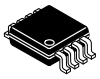
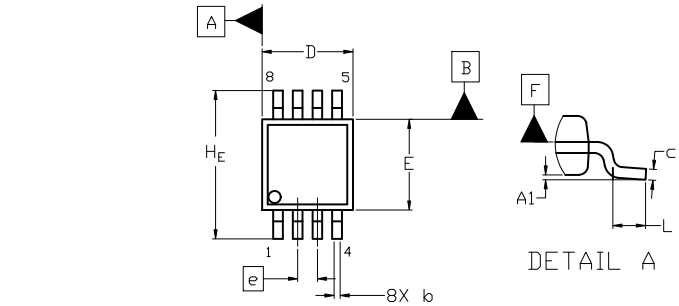
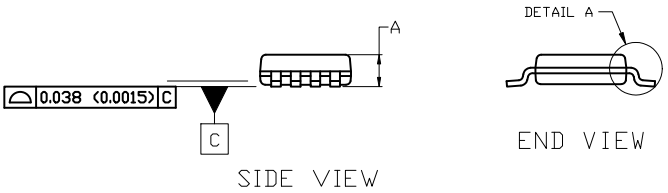


SCALE 2:1

Micro8
CASE 846A–02
ISSUE K

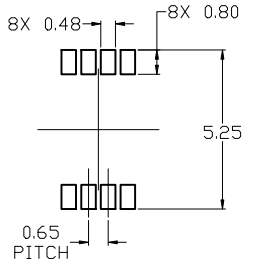
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

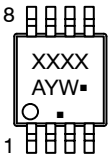


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

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