

# DN8506S

Prescaler IC for TV and VCR tuners

## ■ Overview

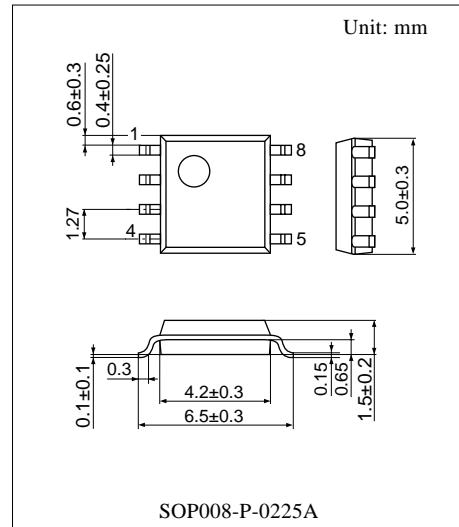
The DN8506S is a 1.1GHz prescaler IC for television and VCR tuners. It is made up of ECL flip-flop circuits divided by 128 and 136.

## ■ Features

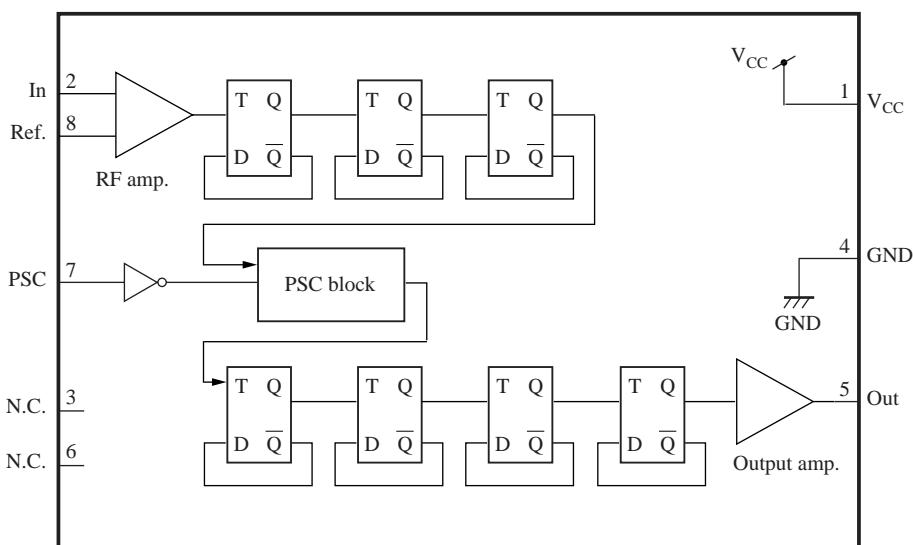
- Power dissipation: 5 V, 26 mA
- The dividing ratios of 1/128, 1/136
- ECL-level output

## ■ Applications

- Television, VCR



## ■ Block Diagram



### ■ Pin Descriptions

Pin No.	Description
1	$V_{CC}$ ( $5 \pm 0.5$ V)
2	Input
3	N.C.
4	GND
5	Output
6	N.C.
7	PSC
8	Ref. (bias)

### ■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	6	V
Input voltage	$V_I$	2.5	V[p-p]
Power dissipation	$P_D$	361	mW
Operating ambient temperature *	$T_{opr}$	-20 to +80	°C
Storage temperature *	$T_{stg}$	-55 to +125	°C

Note) \*: Except for the operating ambient temperature and storage temperature, all ratings are for  $T_a = 25$ °C.

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V

### ■ Electrical Characteristics at $T_a = 25$ °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	$I_{CC}$	$V_{CC} = 5.0$ V	—	26	35	mA
Output amplitude	$V_O$	$V_{CC} = 5.0$ V, $f = 1$ GHz, 0 dBm	0.8	1.2	1.5	V[p-p]
Input voltage *	$V_{IN1}$	$V_{CC} = 5.0$ V, $f_{IN} = 150$ MHz to 900 MHz	-24	—	—	dBm
			40	—	—	mV[p-p]
	$V_{IN2}$	$V_{CC} = 5.0$ V, $f_{IN} = 80$ MHz to 1 100 MHz	-18	—	—	dBm
			80	—	—	mV[p-p]
High-level input voltage	$V_{IH}$	PSC pin	$0.7 \times V_{CC}$	—	—	V
Low-level input voltage	$V_{IL}$	PSC pin	—	—	$0.3 \times V_{CC}$	V

Note) \*: The input level that allows a stipulated frequency-devided output.

■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)

- Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	—	—	42	$\text{mA}$
Input voltage *	$V_{IN1}$	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $f_{IN} = 150 \text{ MHz to } 900 \text{ MHz}$	30	—	1 000	$\text{mV[p-p]}$
	$V_{IN2}$	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $f_{IN} = 70 \text{ MHz to } 1 100 \text{ MHz}$	60	—	1 000	

Note) \*: The input level that allows a stipulated frequency-devided output.

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