

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-UP Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DESCRIPTION

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, and \overline{CLKBA} . The output enables are complementary (OEAB is active high, and \overline{OEBA} is active low).

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor, and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	\overline{CLKAB}
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
\overline{OEBA}	27	30	\overline{CLKBA}
LEBA	28	29	GND



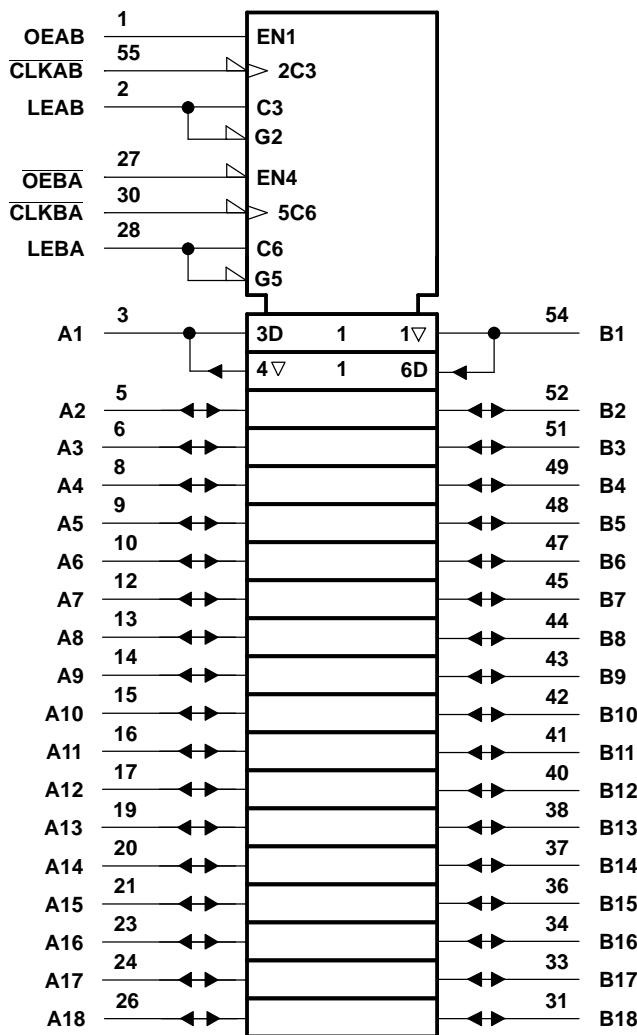
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FUNCTION TABLE⁽¹⁾

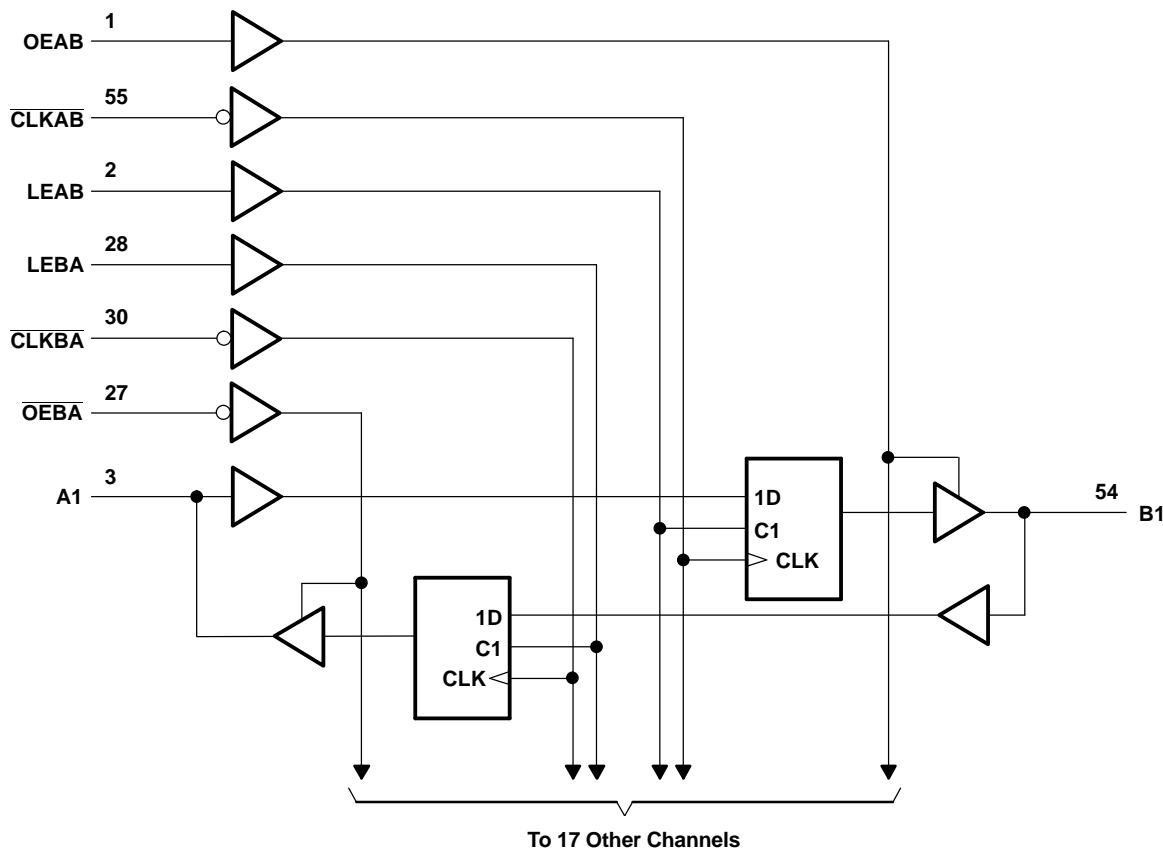
INPUTS				OUTPUT B
OEAB	LEAB	\overline{CLKAB}	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	$B_0^{(2)}$
H	L	L	X	$B_0^{(3)}$

(1) A-to-B data flow is shown; B-to-A flow is similar but uses \overline{OEBA} , $LEBA$, and \overline{CLKBA} .
 (2) Output level before the indicated steady-state input conditions were established, provided that \overline{CLKAB} was high before $LEAB$ went low
 (3) Output level before the indicated steady-state input conditions were established

LOGIC SYMBOL⁽¹⁾

(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74ALVCH16500
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES023I—JULY 1995—REVISED OCTOBER 2004



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range	Except I/O ports ⁽²⁾	-0.5	4.6
		I/O ports ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through each V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	64	$^{\circ}\text{C}/\text{W}$
		DL package	56	
T_{stg}	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$	-4	mA
		$V_{CC} = 2.3 \text{ V}$	-12	
		$V_{CC} = 2.7 \text{ V}$	-12	
		$V_{CC} = 3 \text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	12	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	$^{\circ}\text{C}$

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 μ A	1.65 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -6 mA	2.3 V		2		
	I _{OH} = -12 mA	2.3 V		1.7		
		2.7 V		2.2		
		3 V		2.4		
V _{OL}	I _{OL} = -24 mA	3 V		2		V
	I _{OL} = 100 μ A	1.65 V to 3.6 V		0.2		
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 6 mA	2.3 V		0.4		
	I _{OL} = 12 mA	2.3 V		0.7		
		2.7 V		0.4		
I _I	I _{OL} = 24 mA	3 V		0.55		μ A
	V _I = V _{CC} or GND	3.6 V		\pm 5		
	V _I = 0.58 V	1.65 V		25		
	V _I = 1.07 V	1.65 V		-25		
	V _I = 0.7 V	2.3 V		45		
	V _I = 1.7 V	2.3 V		-45		
	V _I = 0.8 V	3 V		75		
I _{I(hold)}	V _I = 2 V	3 V		-75		μ A
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V		\pm 500		
I _{OZ} ⁽³⁾	V _O = V _{CC} or GND	3.6 V		\pm 10		μ A
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		40		μ A
ΔI_{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750		μ A
C _i	Control inputs V _I = V _{CC} or GND	3.3 V		4		pF
C _{io}	A or B ports V _O = V _{CC} or GND	3.3 V		8		pF

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

				$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 2.7 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			(1)	150	150	150	MHz
t_w	Pulse duration	LE high		(1)	3.3	3.3	3.3	ns
		CLK high or low		(1)	3.3	3.3	3.3	
t_{su}	Setup time	Data before CLK↓		(1)	1.7	1.4	1.3	ns
		Data before LE↓	CLK high	(1)	1.1	1	1	
			CLK low	(1)	1.9	1.6	1.4	
t_h	Hold time	Data after CLK↓		(1)	1.7	1.6	1.3	ns
		Data after LE↓	CLK high	(1)	2	1.8	1.5	
			CLK low	(1)	1.6	1.5	1.2	

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 2.7 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	UNIT	
			MIN	TYP	MIN	MAX		
f_{max}			(1)	150	150	150	MHz	
t_{pd}	A or B	B or A	(1)	1	5.1	4.7	1	3.9
	LEAB or LEBA		(1)	1	5.9	5.5	1	4.7
	CLKAB or CLKBA		(1)	1	6.6	6.6	1.1	5.5
t_{en}	OEAB	B	(1)	1	5.7	5.4	1	4.6
t_{dis}	OEAB	B	(1)	1	6.1	5.7	1.5	5
t_{en}	OEBA	A	(1)	1	6.2	6.2	1	5.2
t_{dis}	OEBA	A	(1)	1	5.4	4.6	1	4.3

(1) This information was not available at the time of publication.

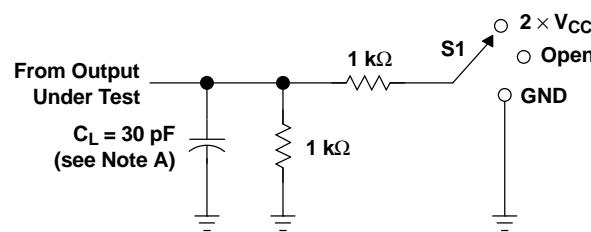
OPERATING CHARACTERISTICS $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	(1)	40	51
		Outputs disabled	(1)	6	6

(1) This information was not available at the time of publication.

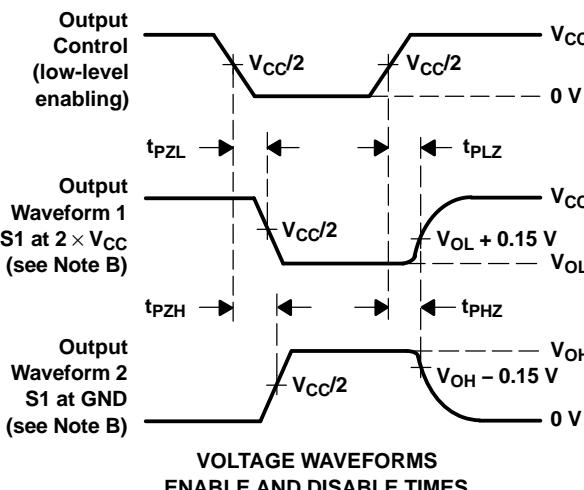
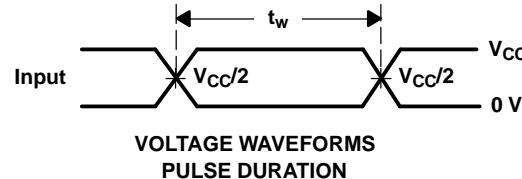
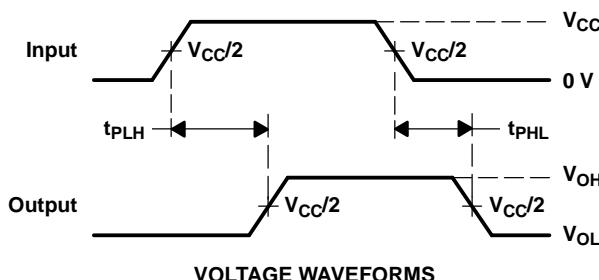
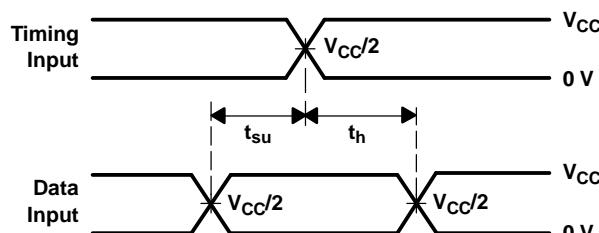
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

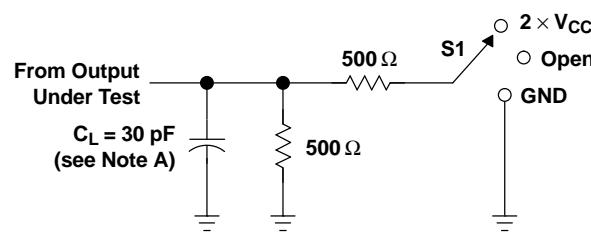


NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

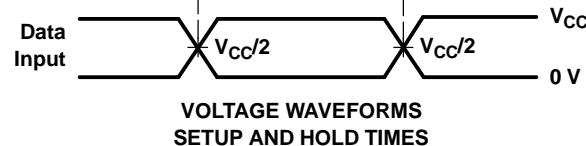
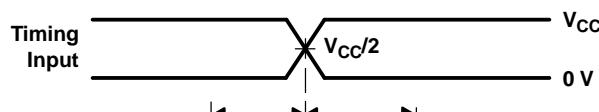
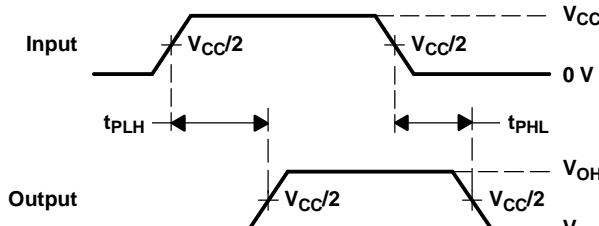
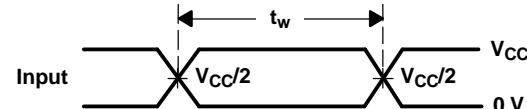
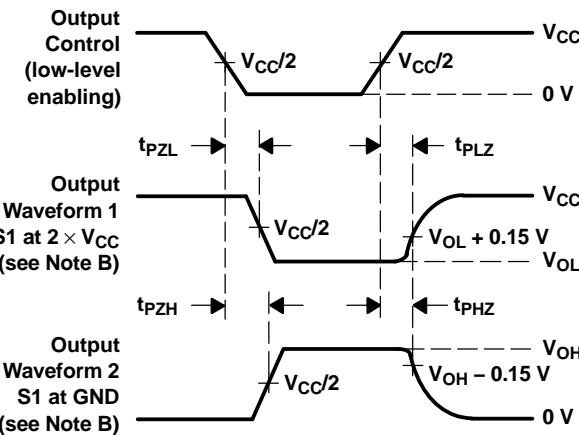
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ 

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

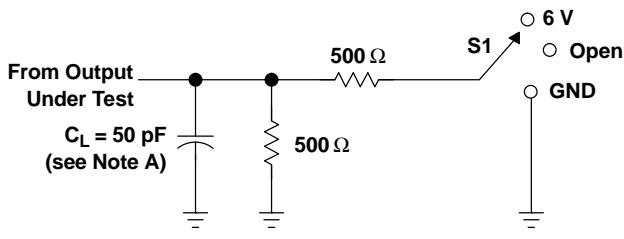
NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

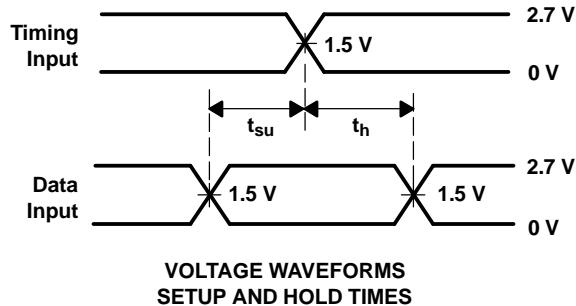
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

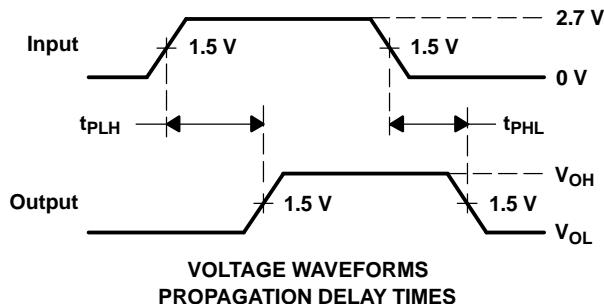
$V_{CC} = 2.7\text{ V AND }3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

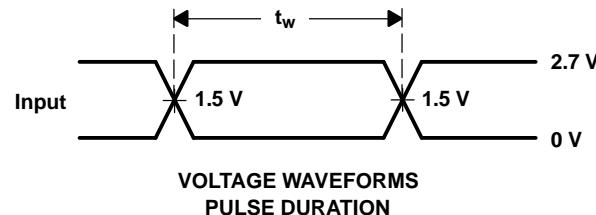


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

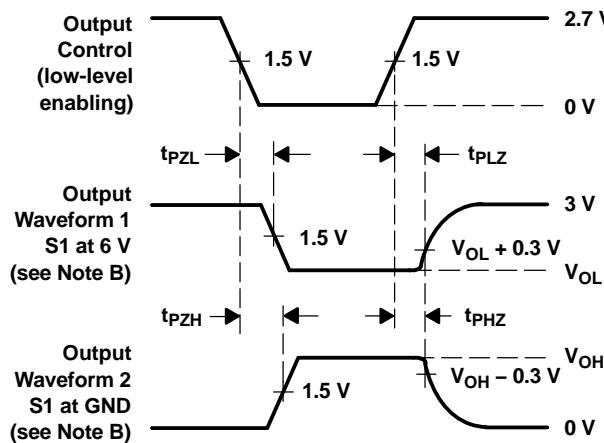


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16500DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16500DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16500DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16500DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16500DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16500DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16500DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

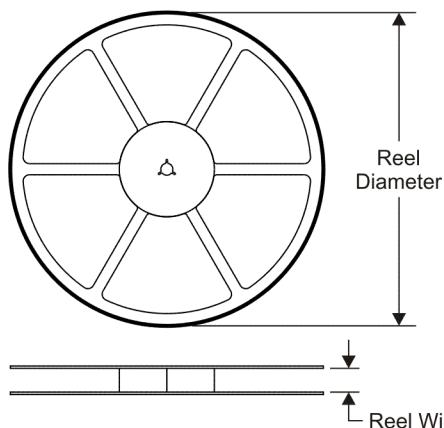
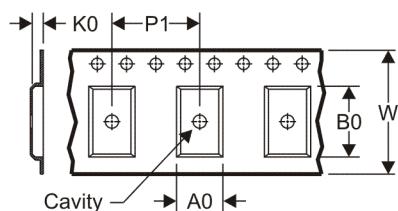
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

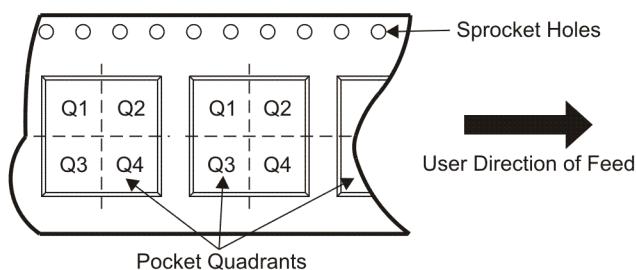
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


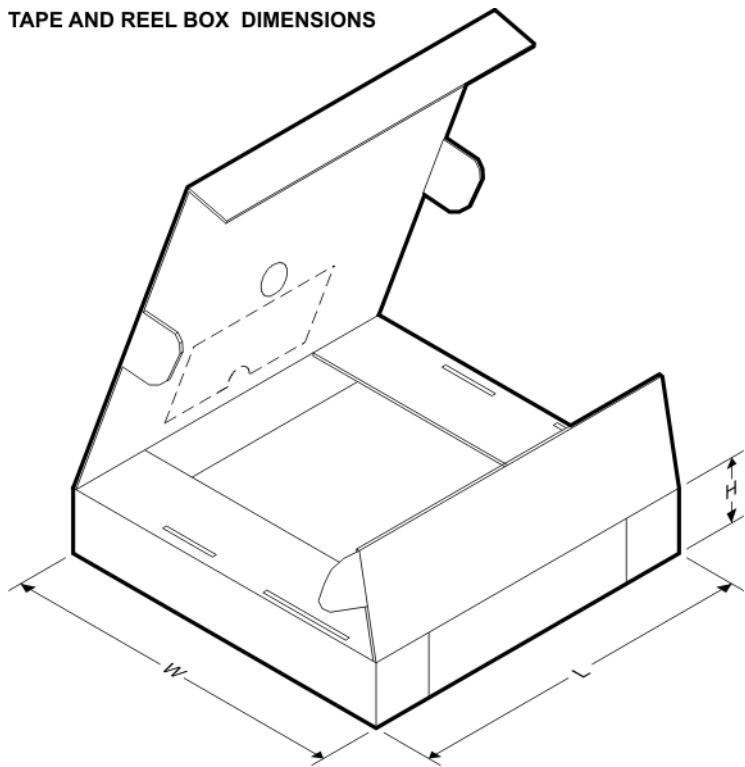
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16500DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16500DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



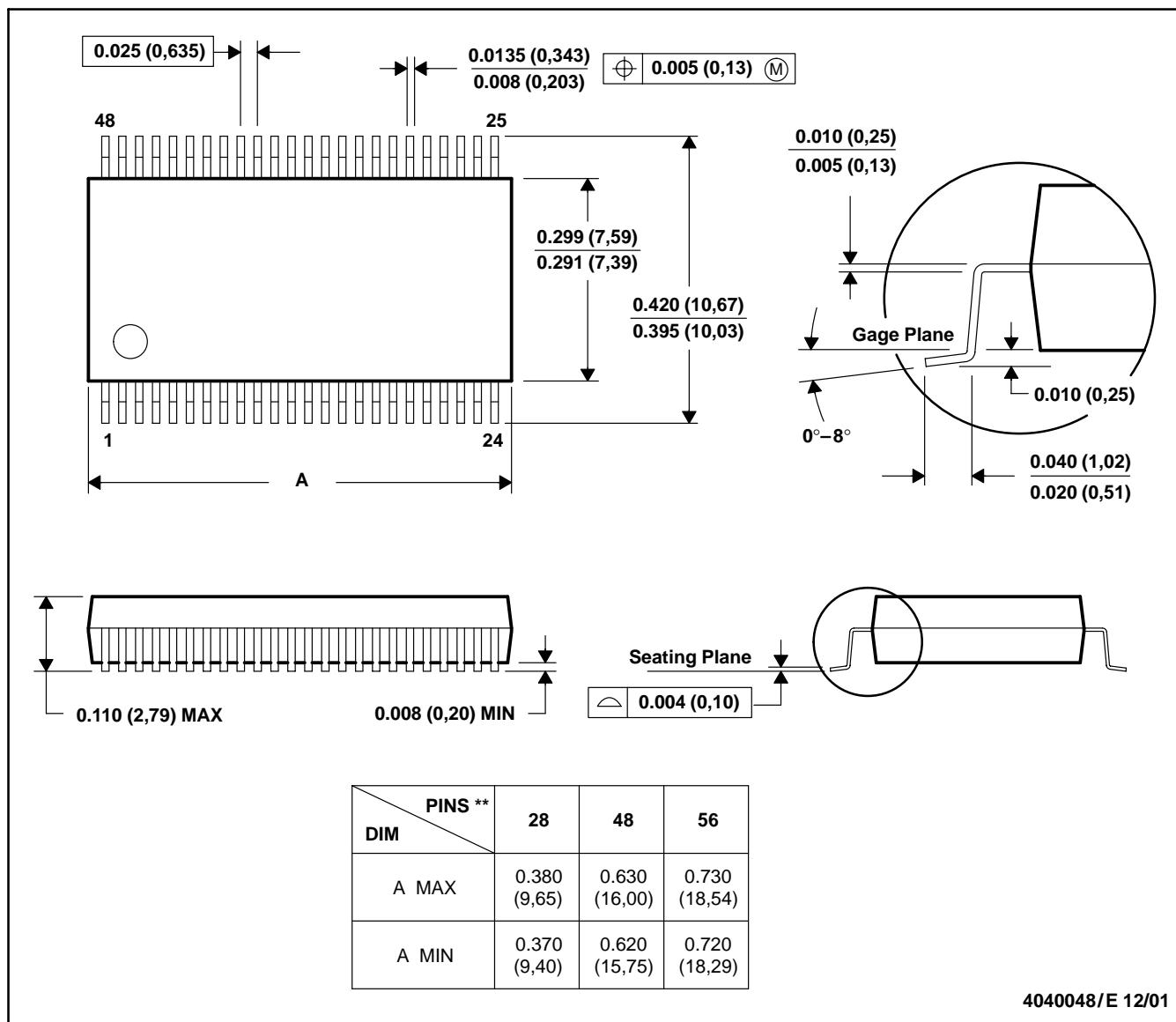
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16500DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16500DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

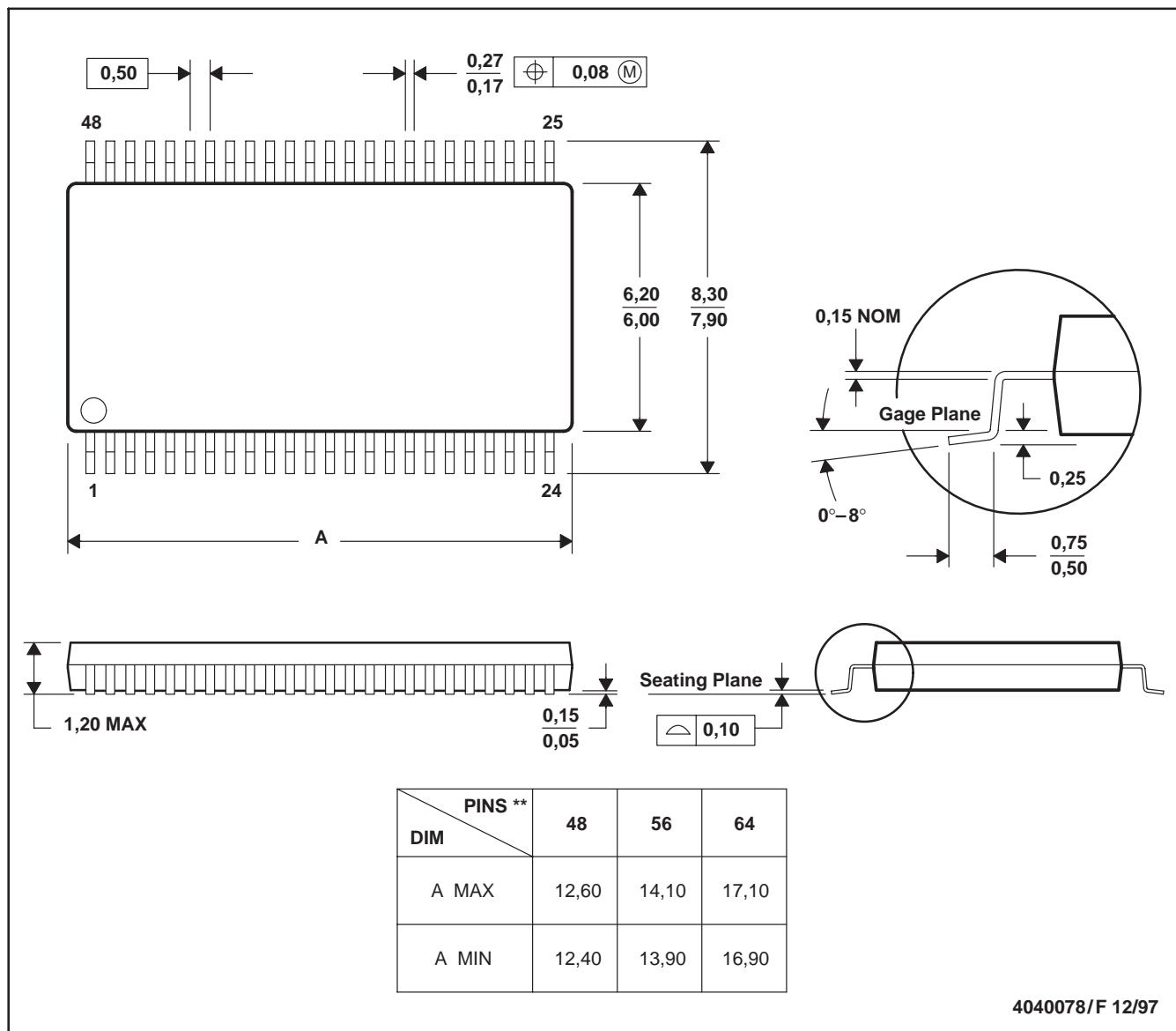


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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