



**FDG8850NZ**

## Dual N-Channel PowerTrench® MOSFET

**30V,0.75A,0.4Ω**

## Features

- Max  $r_{DS(on)} = 0.4\Omega$  at  $V_{GS} = 4.5V$ ,  $I_D = 0.75A$
- Max  $r_{DS(on)} = 0.5\Omega$  at  $V_{GS} = 2.7V$ ,  $I_D = 0.67A$
- Very low level gate drive requirements allowing operation in 3V circuits ( $V_{GS(th)} < 1.5V$ )
- Very small package outline SC70-6
- RoHS Compliant



## General Description

This dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.



## MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current -Continuous	0.75	A
	-Pulsed	2.2	
$P_D$	Power Dissipation for Single Operation	(Note 1a)	W
		(Note 1b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

## Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single operation	(Note 1a)	350	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single operation	(Note 1b)	415	

## Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.50	FDG8850NZ	7"	8mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		25		$\text{mV/}^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.65	1.0	1.5	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-3.0		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 0.75\text{A}$ $V_{GS} = 2.7\text{V}, I_D = 0.67\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 0.75\text{A}, T_J = 125^\circ\text{C}$		0.25 0.29 0.36	0.4 0.5 0.6	$\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 0.75\text{A}$		3		S

**Dynamic Characteristics**

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		90	120	$\text{pF}$
$C_{\text{oss}}$	Output Capacitance			20	30	$\text{pF}$
$C_{\text{rss}}$	Reverse Transfer Capacitance			15	25	$\text{pF}$

**Switching Characteristics (note 2)**

$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{DD} = 5\text{V}, I_D = 0.5\text{A}, V_{GS} = 4.5\text{V}, R_{\text{GEN}} = 6\Omega$		4	10	ns
$t_r$	Rise Time			1	10	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time			9	18	ns
$t_f$	Fall Time			1	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 4.5\text{V}, V_{DD} = 5\text{V}, I_D = 0.75\text{A}$		1.03	1.44	nC
$Q_{gs}$	Gate to Source Charge			0.29		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.17		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

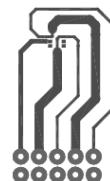
$I_S$	Maximum Continuous Drain-Source Diode Forward Current			0.3	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 0.3\text{A}$	(Note 2)	0.76	1.2	V

**Notes:**

1.  $R_{\text{fJA}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\text{fJC}}$  is guaranteed by design while  $R_{\text{fJA}}$  is determined by the user's board design.



a.  $350^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b.  $415^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

Scale 1:1 on letter size paper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

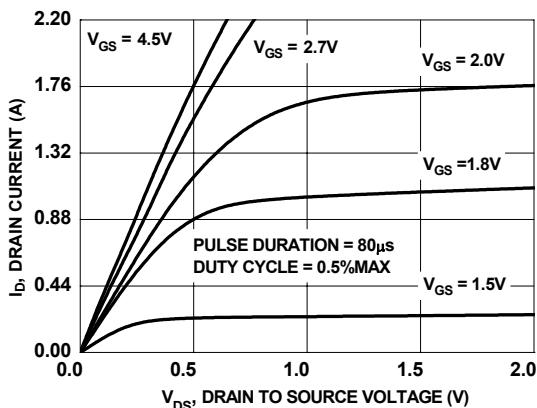


Figure 1. On-Region Characteristics

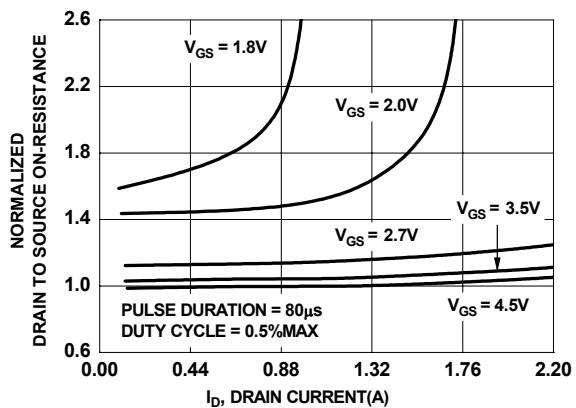


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

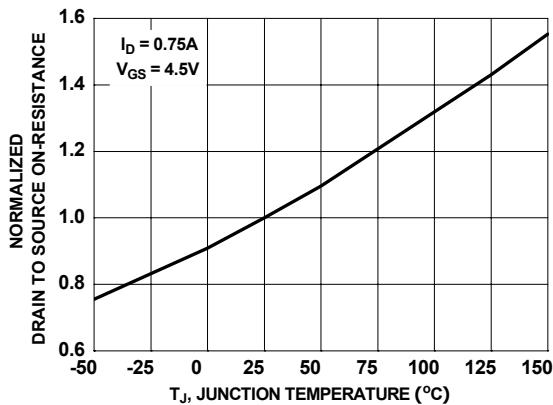


Figure 3. Normalized On-Resistance vs Junction Temperature

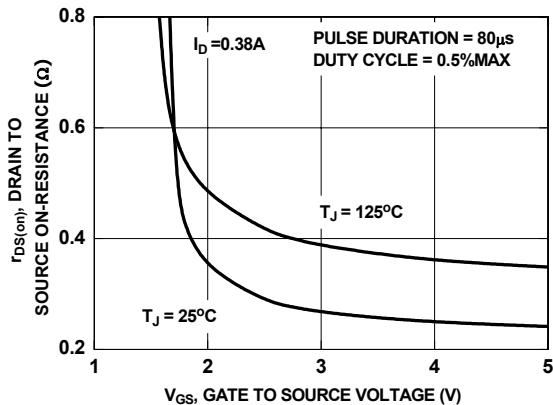


Figure 4. On-Resistance vs Gate to Source Voltage

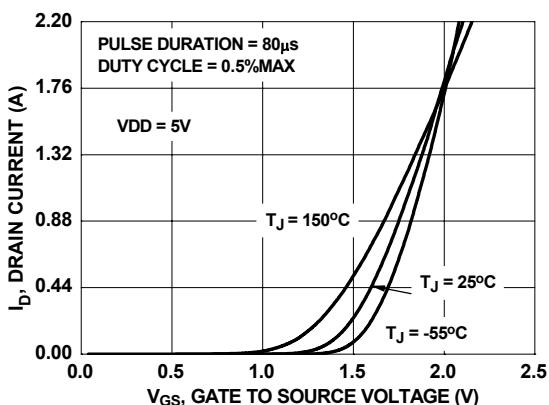


Figure 5. Transfer Characteristics

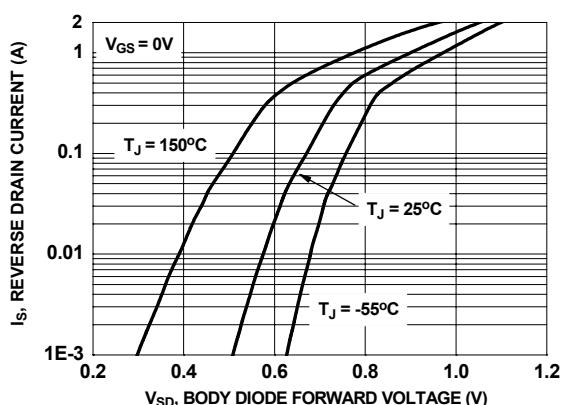


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

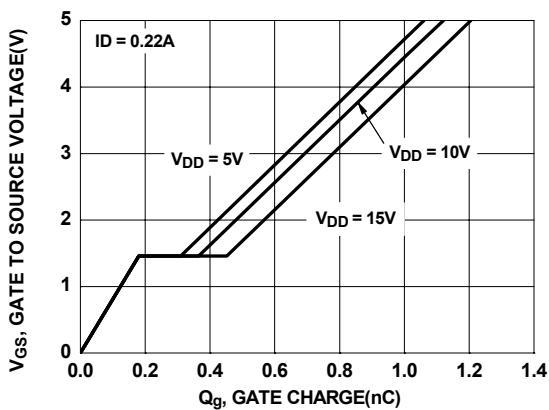


Figure 7. Gate Charge Characteristics

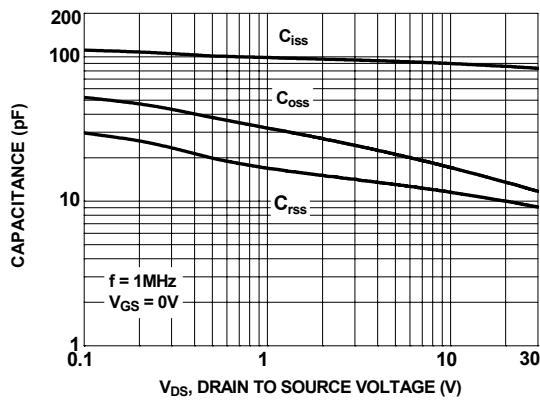


Figure 8. Capacitance vs Drain to Source Voltage

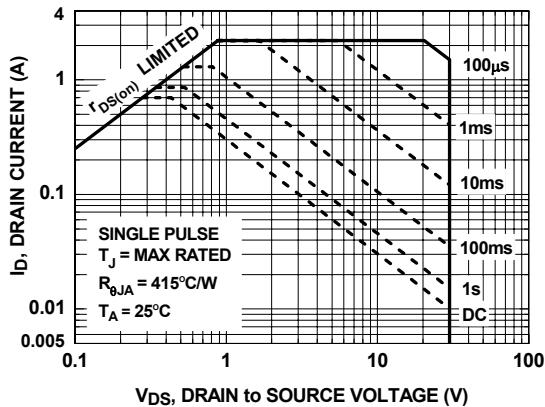


Figure 9. Forward Bias Safe Operating Area

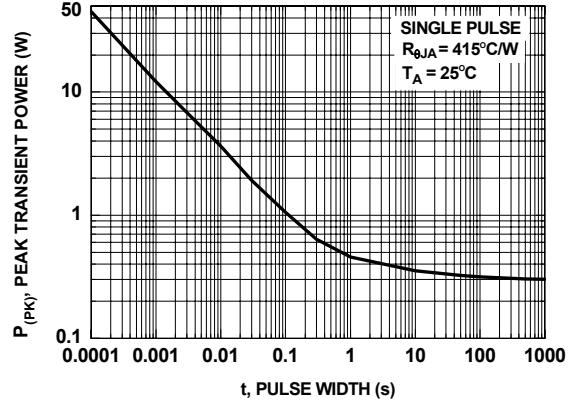


Figure 10. Single Pulse Maximum Power Dissipation

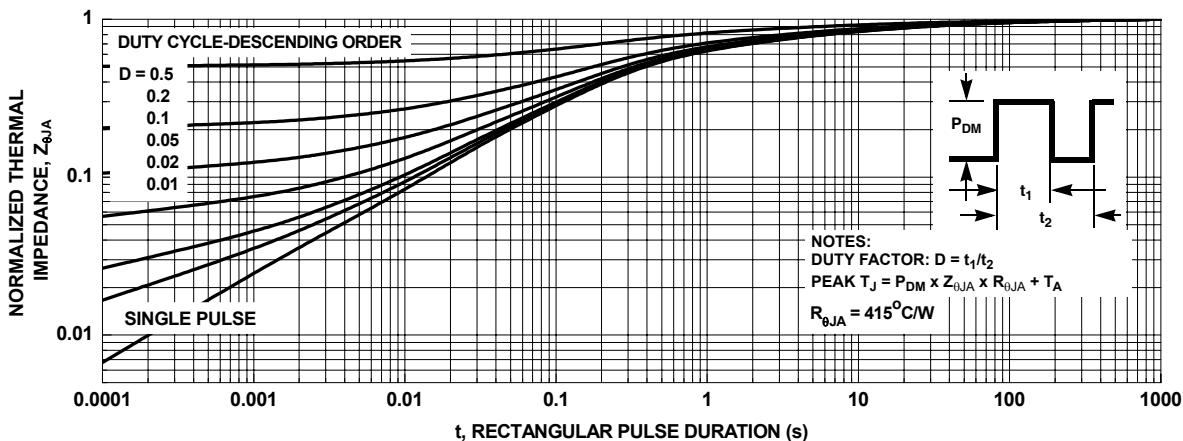


Figure 11. Transient Thermal Response Curve



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