

FEATURES

Low V_{OS} (V_{BE} match): 40 μV typical, 100 μV maximum

Low TCV_{OS} : 0.5 $\mu V/^{\circ}C$ maximum

High h_{FE} : 500 minimum

Excellent h_{FE} linearity from 10 nA to 10 mA

Low noise voltage: 0.23 μV p-p from 0.1 Hz to 10 Hz

High breakdown: 45 V min

APPLICATIONS

Weigh scales

Low noise, op amp, front end

Current mirror and current sink/source

Low noise instrumentation amplifiers

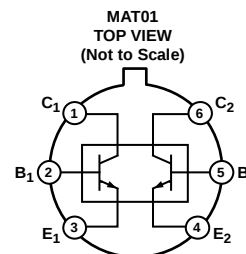
Voltage controlled attenuators

Log amplifiers

GENERAL DESCRIPTION

The **MAT01** is a monolithic dual NPN transistor. An exclusive silicon nitride triple passivation process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40 μV , temperature drift of 0.15 $\mu V/^{\circ}C$, and h_{FE} matching of 0.7%.

PIN CONNECTION DIAGRAM



NOTES

1. SUBSTRATE IS CONNECTED TO CASE.

00282-001

Figure 1.

High h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10 nA. The high gain at low collector current makes the **MAT01** ideal for use in low power, low level input stages.

MAT01* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-139: A Low Voltage Power Supply Watch-Dog Monitor Circuit

Data Sheet

- MAT01: Matched Monolithic Dual Transistor Data Sheet

DESIGN RESOURCES

- MAT01 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all MAT01 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

Features	1
Applications	1
Pin Connection Diagram	1
General Description	1
Revision History	2
Specifications	3
Electrical Characteristics	3
Absolute Maximum Ratings	5

ESD Caution	5
Typical Performance Characteristics	6
Test Circuits	8
Applications Information	9
Typical Applications	10
Outline Dimensions	11
Ordering Guide	11

REVISION HISTORY

9/14—Rev. C to Rev. D

Changes to Figure 4 and Figure 7	6
--	---

4/13—Rev. B to Rev. C

Updated Format	Universal
Added Applications Section, Deleted Figure 2, Renumbered Sequentially	1
Deleted Table 3, Renumbered Sequentially	4
Changes to Table 3	5
Changes to Typical Performance Characteristics Section	6
Updated Outline Dimensions	11
Changes to Ordering Guide	11

2/02—Rev. A to Rev. B

Edits to Features	1
Deleted Wafer Test Limits	3
Deleted DICE Characteristics	3
Edits to Table 5	7

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	MAT01AH			MAT01GH			Unit
			Min	Typ	Max	Min	Typ	Min	
VOLTAGE									
Breakdown Voltage	BV _{CEO}	I _C = 100 μA	45			45			V
Offset Voltage	V _{OS}			0.04	0.1		0.10	0.5	mV
Offset Voltage Stability									
First Month ¹	V _{OS} /Time			2.0			2.0		μV/Mo
Long Term ²				0.2			0.2		μV/Mo
CURRENT									
Offset Current	I _{OS}			0.1	0.6		0.2	3.2	nA
Bias Current	I _B			13	20		18	40	nA
Current Gain	h _{FE}	I _C = 10 nA		590			430		
		I _C = 10 μA	500	770		250	560		
		I _C = 10 mA		840			610		
Current Gain Match	Δh _{FE}	I _C = 10 μA		0.7	3.0		1.0	8.0	%
		100 nA ≤ I _C ≤ 10 mA		0.8			1.2		%
NOISE									
Low Frequency Noise Voltage	e _n p-p	0.1 Hz to 10 Hz ³		0.23	0.4		0.23	0.4	μV p-p
Broadband Noise Voltage	e _n rms	1 Hz to 10 kHz		0.60			0.60		μV rms
Noise Voltage Density	e _n	f ₀ = 10 Hz ³		7.0	9.0		7.0	9.0	nV/√Hz
		f ₀ = 100 Hz ³		6.1	7.6		6.1	7.6	nV/√Hz
		f ₀ = 1000 Hz ³		6.0	7.5		6.0	7.5	nV/√Hz
OFFSET VOLTAGE/CURRENT									
Offset Voltage Change	ΔV _{OS} /ΔV _{CB}	0 ≤ V _{CB} ≤ 30 V		0.5	3.0		0.8	8.0	μV/V
Offset Current Change	ΔI _{OS} /ΔV _{CB}	0 ≤ V _{CB} ≤ 30 V		2	15		3	70	pA/V
LEAKAGE									
Collector to Base Leakage Current	I _{CBO}	V _{CB} = 30 V, I _E = 0 ⁴		15	50		25	200	pA
Collector to Emitter Leakage Current	I _{CES}	V _{CE} = 30 V, V _{BE} = 0 ^{4,5}		50	200		90	400	pA
Collector to Collector Leakage Current	I _{CC}	V _{CC} = 30 V ⁵		20	200		30	400	pA
SATURATION									
Collector Saturation Voltage	V _{CE(SAT)}	I _B = 0.1 mA, I _C = 1 mA		0.12	0.20		0.12	0.25	V
		I _B = 1 mA, I _C = 10 mA		0.8			0.8		V
GAIN BANDWIDTH PRODUCT									
	f _T	V _{CE} = 10 V, I _C = 10 mA		450			450		MHz
CAPACITANCE									
Output Capacitance	C _{OB}	V _{CB} = 15 V, I _E = 0		2.8			2.8		pF
Collector to Collector Capacitance	C _{CC}	V _{CC} = 0		8.5			8.5		pF

¹ Exclude first hour of operation to allow for stabilization.

² Parameter describes long-term average drift after first month of operation.

³ Sample tested.

⁴ The collector to base (I_{CBO}) and collector to emitter (I_{CES}) leakage currents can be reduced by a factor of 2 to 10 times by connecting the substrate (package) to a potential that is lower than either collector voltage.

⁵ I_{CC} and I_{CES} are guaranteed by measurement of I_{CBO} .

$V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	MAT01AH			MAT01GH			Unit
			Min	Typ	Max	Min	Typ	Min	
OFFSET VOLTAGE/CURRENT									
Offset Voltage	V_{OS}			0.06	0.15		0.14	0.70	mV
Average Offset Voltage Drift ¹	TCV_{OS}			0.15	0.50		0.35	1.8	$\mu\text{V}/^\circ\text{C}$
Offset Current	I_{OS}			0.9	8.0		1.5	15.0	nA
Average Offset Current Drift ²	TCI_{OS}			10	90		15	150	$\text{pA}/^\circ\text{C}$
BIAS CURRENT	I_B			28	60		36	130	nA
CURRENT GAIN	h_{FE}		167	400		77	300		
LEAKAGE CURRENT									
Collector to Base Leakage Current	I_{CBO}	$T_A = 125^\circ\text{C}$, $V_{CB} = 30\text{ V}$, $I_E = 0^3$		15	80		25	200	nA
Collector to Emitter Leakage Current	I_{CES}	$T_A = 125^\circ\text{C}$, $V_{CE} = 30\text{ V}$, $V_{BE} = 0^{1,3}$		50	300		90	400	nA
Collector to Collector Leakage Current	I_{CC}	$T_A = 125^\circ\text{C}$, $V_{CC} = 30\text{ V}^1$		30	200		50	400	nA

¹ Guaranteed by V_{OS} test $\left(TCV_{OS} \cong \frac{V_{OS}}{T} \text{ for } V_{OS} \ll V_{BE} \right)$, $T = 298\text{ K}$ for $T_A = 25^\circ\text{C}$.

² Guaranteed by I_{OS} test limits over temperature.

³ The collector to base (I_{CBO}) and collector to emitter (I_{CES}) leakage currents can be reduced by a factor of 2 to 10 times by connecting the substrate (package) to a potential that is lower than either collector voltage.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter ¹	Rating
Breakdown Voltage of	
Collector to Base Voltage (BV_{CBO})	45 V
Collector to Emitter Voltage (BV_{CEO})	45 V
Collector to Collector Voltage (BV_{CC})	45 V
Emitter to Emitter Voltage (BV_{EE})	45 V
Emitter to Base Voltage (BV_{EBO}) ²	5 V
Current	
Collector (I_C)	25 mA
Emitter (I_E)	25 mA
Total Power Dissipation	
Case Temperature $\leq 40^\circ\text{C}$ ³	1.8 W
Ambient Temperature $\leq 70^\circ\text{C}$ ⁴	500 mW
Temperature Range	
Operating	-55°C to $+125^\circ\text{C}$
Junction	-55°C to $+150^\circ\text{C}$
Storage	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

¹ Absolute maximum ratings apply to packaged devices.

² Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5 V rating.

³ Rating applies to applications using heat sinking to control case temperature. Derate linearity at $16.4 \text{ mW}/^\circ\text{C}$ for case temperatures above 40°C .

⁴ Rating applies to applications not using heat sinking; device in free air only. Derate linearity at $6.3 \text{ mW}/^\circ\text{C}$ for ambient temperatures above 70°C .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

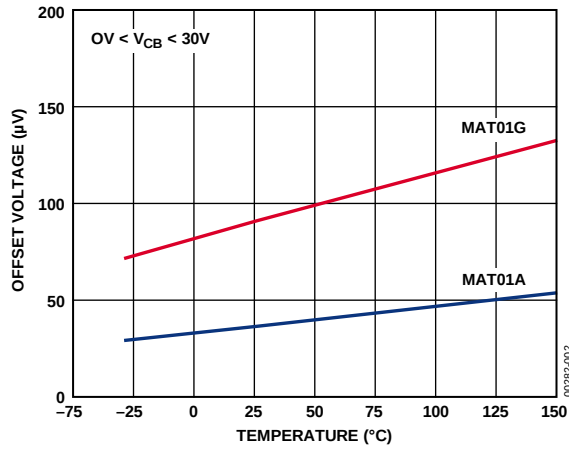


Figure 2. Offset Voltage vs. Temperature

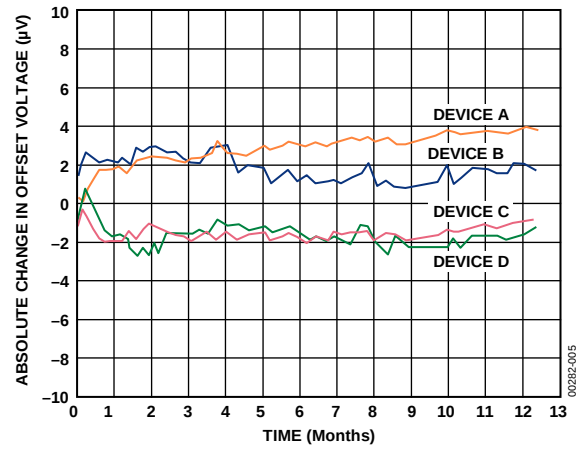


Figure 5. Offset Voltage vs. Time

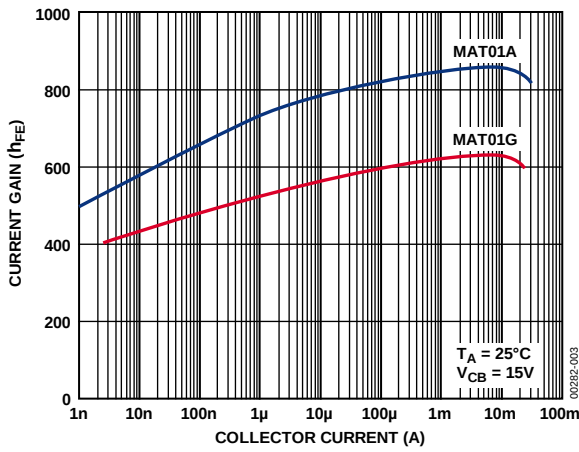


Figure 3. Current Gain vs. Collector Current

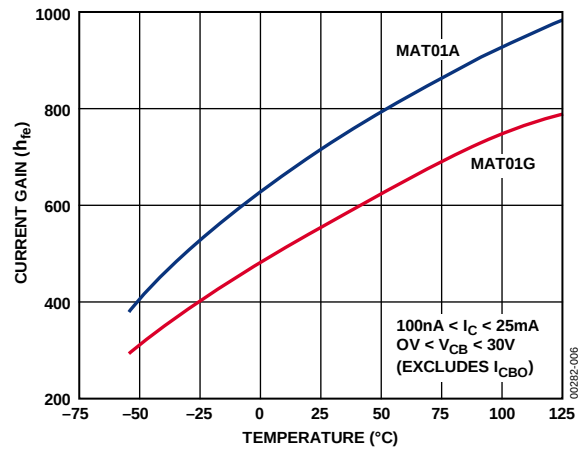


Figure 6. Current Gain vs. Temperature

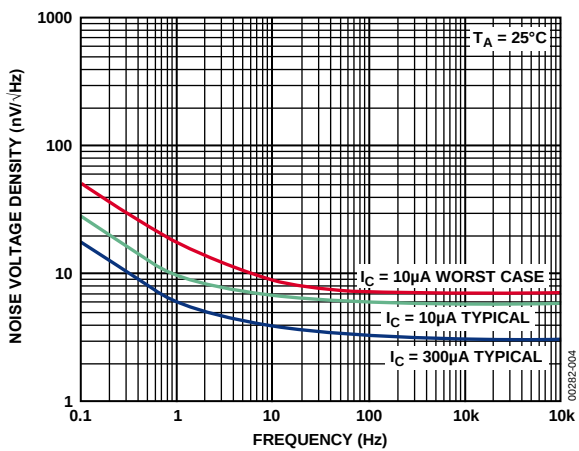


Figure 4. Noise Voltage Density vs. Frequency

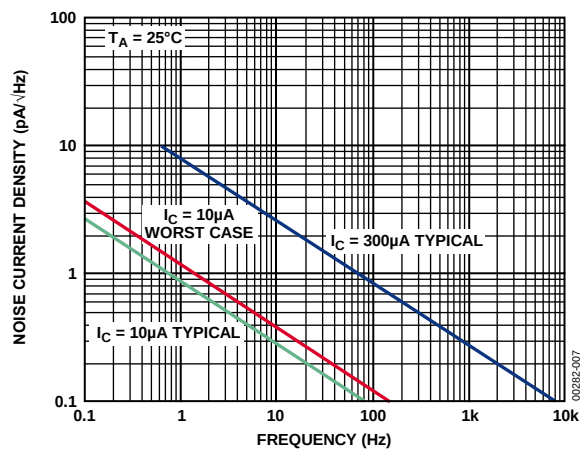


Figure 7. Noise Current Density vs. Frequency

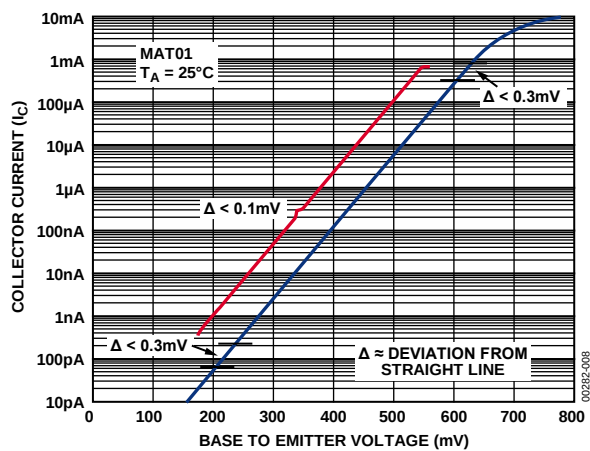


Figure 8. Collector Current vs. Base to Emitter Voltage

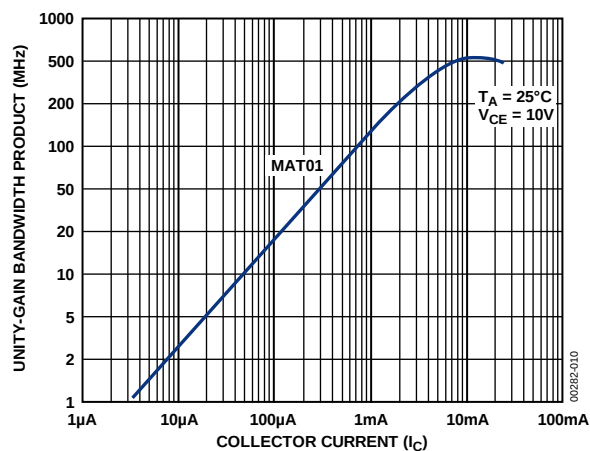


Figure 10. Unity-Gain Bandwidth vs. Collector Current

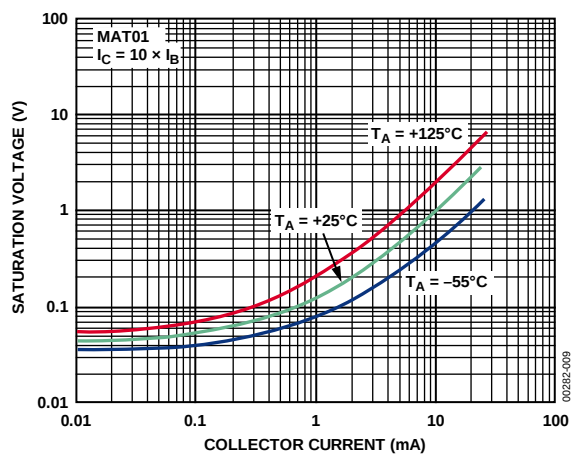


Figure 9. Saturation Voltage vs. Collector Current

TEST CIRCUITS

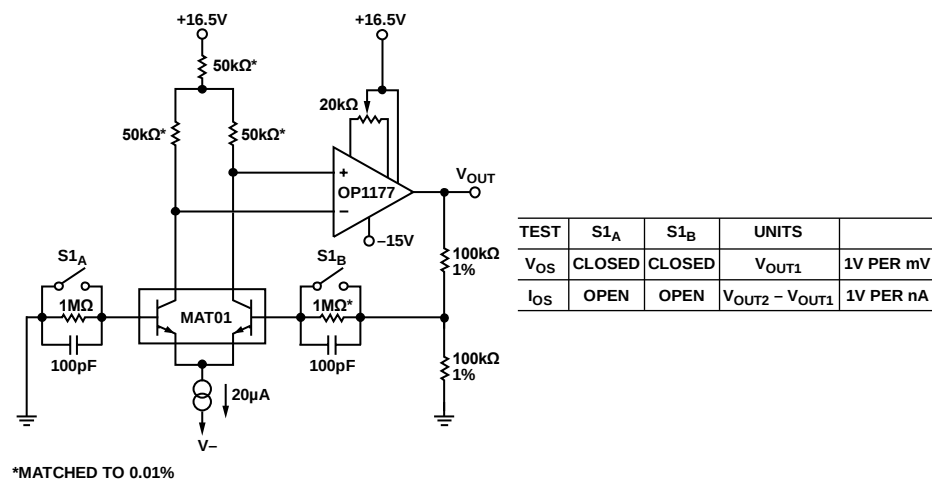


Figure 11. Matching Measurement Circuit

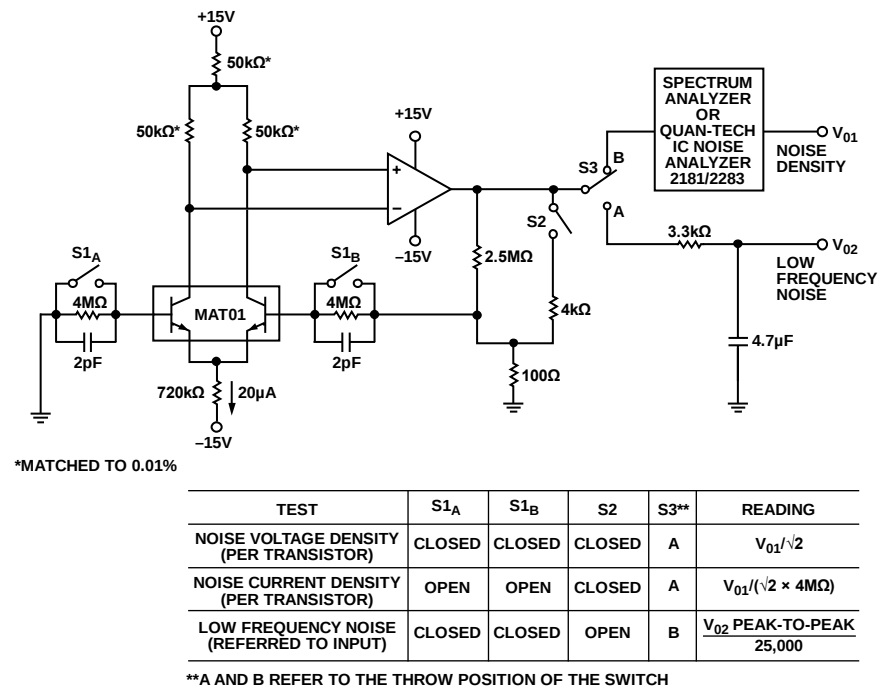


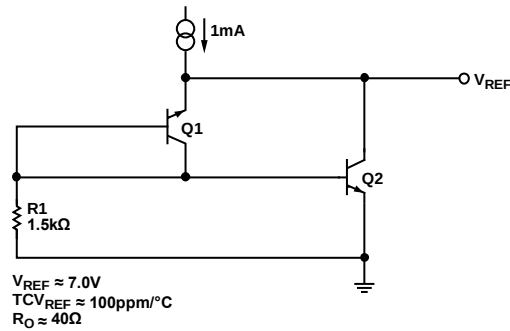
Figure 12. Noise Measurement Circuit

APPLICATIONS INFORMATION

Application of reverse bias voltages to the emitter to base junctions in excess of ratings (5 V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Check circuit designs to ensure that reverse bias voltages above 5 V cannot be applied during transient conditions, such as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Maintain both input terminals at the same temperature, preferably close to the temperature of the device package.

TYPICAL APPLICATIONS

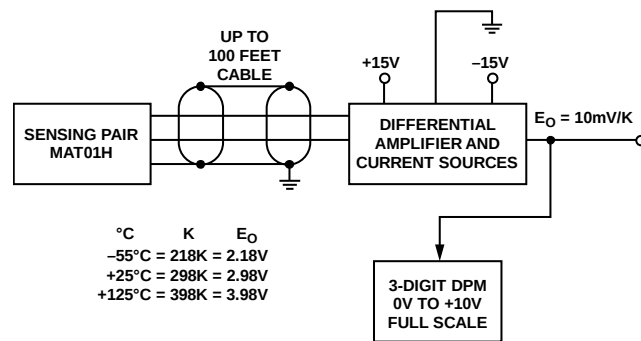


NOTES

1. R1 MAY BE ADJUSTED TO MINIMIZE TCV_{REF} . INCREASING R1 CAUSES A POSITIVE CHANGE IN TCV_{REF} .
2. h_{FE} OF Q1 IS REDUCED BY OPERATION OF BREAKDOWN MODE.

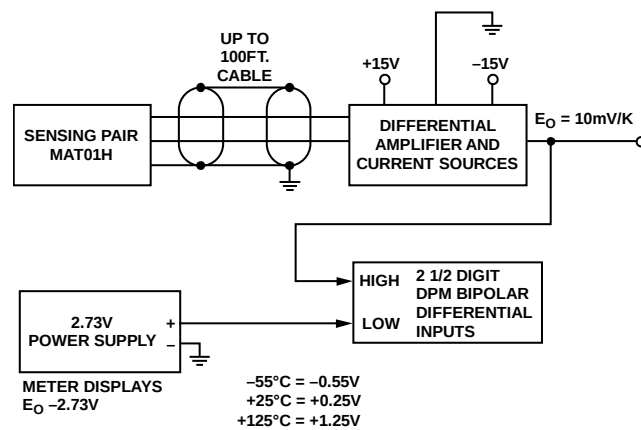
00282-013

Figure 13. Precision Reference



00282-014

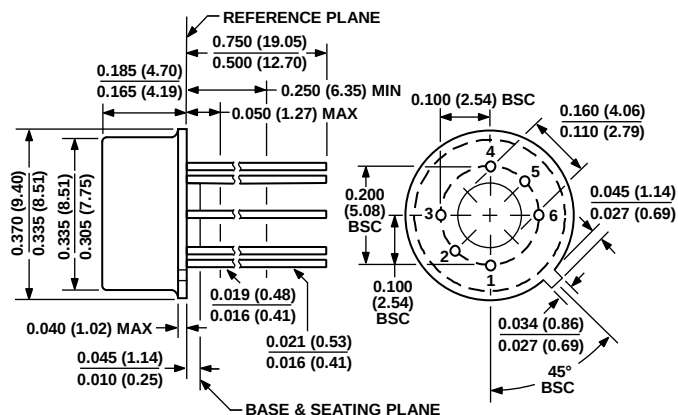
Figure 14. Basic Digital Thermometer Readout in Degrees Kelvin (K)



00282-015

Figure 15. Digital Thermometer with Readout in $^{\circ}C$

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 16. 6-Pin Metal Header Package [TO-78]
(H-06)

Dimensions shown in inches and (millimeters)

022306-A

ORDERING GUIDE

Model ¹	V _{OS} Maximum (T _A = 25°C)	Temperature Range	Package Description	Package Option
MAT01AH	0.1 mV	–55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06
MAT01AHZ	0.1 mV	–55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06
MAT01GH	0.5 mV	–55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06
MAT01GHZ	0.5 mV	–55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06

¹ Z = RoHS Compliant Part.

NOTES