

Single/Dual/Quad 220MHz, 1500V/ μ s Operational Amplifiers with Programmable Supply Current

FEATURES

- 220MHz Gain-Bandwidth Product
- 1500V/ μ s Slew Rate
- 6.5mA Supply Current per Amplifier
- Programmable Current Option
- 6nV/ $\sqrt{\text{Hz}}$ Input Noise Voltage
- Unity-Gain Stable
- 1.5mV Maximum Input Offset Voltage
- 8 μ A Maximum Input Bias Current
- 800nA Maximum Input Offset Current
- 50mA Minimum Output Current, $V_{\text{OUT}} = \pm 3\text{V}$
- $\pm 3.5\text{V}$ Minimum Input CMR, $V_S = \pm 5\text{V}$
- Specified at $\pm 5\text{V}$, Single 5V Supplies
- Operating Temperature Range: -40°C to 85°C
- Space Saving MSOP and SSOP Packages
- Low Profile (1mm) SOT-23 (ThinSOT™) and Leadless DFN Packages

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Communication Receivers
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

The LT®1815/LT1816/LT1817 are low power, high speed, very high slew rate operational amplifiers with excellent DC performance. The LT1815/LT1816/LT1817 feature higher bandwidth and slew rate, much lower input offset voltage and lower noise and distortion than other devices with comparable supply current. A programmable current option (LT1815 and LT1816A) allows power savings and flexibility by operating at reduced supply current and speed. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier.

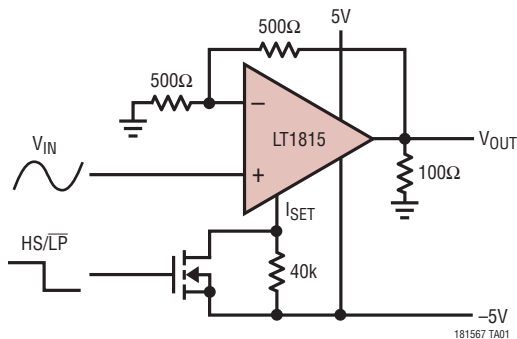
The output drives a 100 Ω load to $\pm 3.8\text{V}$ with $\pm 5\text{V}$ supplies. On a single 5V supply, the output swings from 1V to 4V with a 100 Ω load connected to 2.5V. Harmonic distortion is -70dB for a 5MHz, 2V_{P-P} output driving a 100 Ω load in a gain of -1 .

The LT1815/LT1816/LT1817 are manufactured on Linear Technology's advanced low voltage complementary bipolar process and are available in a variety of TSOT-23, SO, MSOP, SSOP and leadless DFN packages.

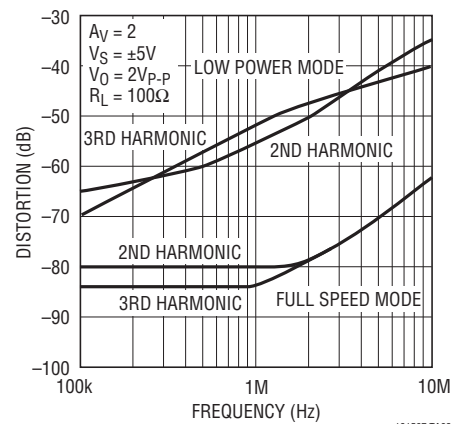
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TYPICAL APPLICATION

**Programmable Current Amplifier Switches
from Low Power Mode to Full Speed Mode**



Distortion vs Frequency



LT1815/LT1816/LT1817

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	12.6V	Specified Temperature Range (Note 8)	-40°C to 85°C
Differential Input Voltage (Transient Only, Note 2)	$\pm 6\text{V}$	Maximum Junction Temperature	150°C
Input Voltage	$\pm V_S$	(DD Package)	125°C
Output Short-Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-40°C to 85°C	(DD Package)	-65°C to 125°C
		Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION

LT1815 S5 PACKAGE 5-LEAD PLASTIC TSOT-23 $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$ (NOTE 9)	LT1815 S6 PACKAGE 6-LEAD PLASTIC TSOT-23 $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 230^{\circ}\text{C/W}$ (NOTE 9)	LT1815 S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$ (NOTE 9)
LT1816 DD PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$ (NOTE 9) UNDERSIDE METAL INTERNALLY CONNECTED TO V^-	LT1816 MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$ (NOTE 9)	LT1816 MS PACKAGE 10-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$ (NOTE 9)
LT1816 S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$ (NOTE 9)	LT1817 GN PACKAGE 16-LEAD PLASTIC SSOP NARROW $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 135^{\circ}\text{C/W}$	LT1817 S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 100^{\circ}\text{C/W}$

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1815CS5#PBF	LT1815CS5#TRPBF	LTUP	5-Lead Plastic TSOT-23	0°C to 70°C
LT1815IS5#PBF	LT1815IS5#TRPBF	LTVC	5-Lead Plastic TSOT-23	–40°C to 85°C
LT1815CS6#PBF	LT1815CS6#TRPBF	LTUL	6-Lead Plastic TSOT-23	0°C to 70°C
LT1815IS6#PBF	LT1815IS6#TRPBF	LTVD	6-Lead Plastic TSOT-23	–40°C to 85°C
LT1815CS8#PBF	LT1815CS8#TRPBF	1815	8-Lead Plastic SO	0°C to 70°C
LT1815IS8#PBF	LT1815IS8#TRPBF	1815I	8-Lead Plastic SO	–40°C to 85°C
LT1816CDD#PBF	LT1816CDD#TRPBF	LAAR	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1816IDD#PBF	LT1816IDD#TRPBF	LAAR	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 150°C
LT1816CMS8#PBF	LT1816CMS8#TRPBF	LTWA	8-Lead Plastic MSOP	0°C to 70°C
LT1816IMS8#PBF	LT1816IMS8#TRPBF	LTNQ	8-Lead Plastic MSOP	–40°C to 85°C
LT1816ACMS#PBF	LT1816ACMS#TRPBF	LYA	10-Lead Plastic MSOP	0°C to 70°C
LT1816AIMS#PBF	LT1816AIMS#TRPBF	LTX	10-Lead Plastic MSOP	–40°C to 85°C
LT1816CS8#PBF	LT1816CS8#TRPBF	1816	8-Lead Plastic SO	0°C to 70°C
LT1816IS8#PBF	LT1816IS8#TRPBF	1816I	8-Lead Plastic SO	–40°C to 85°C
LT1817CGN#PBF	LT1817CGN#TRPBF	1817	16-Lead Plastic SSOP	0°C to 70°C
LT1817IGN#PBF	LT1817IGN#TRPBF	1817I	16-Lead Plastic SSOP	–40°C to 85°C
LT1817CS#PBF	LT1817CS#TRPBF	LT1817CS	14-Lead Plastic SO	0°C to 70°C
LT1817IS#PBF	LT1817IS#TRPBF	LT1817IS	14-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 8). $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. For the programmable current option (LT1815S6 or LT1816A), the I_{SET} pin must be connected to V^- through 75Ω or less, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.2	1.5	mV
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●		2.0	mV
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		3.0	mV
	Input Offset Voltage (Low Power Mode) (Note 10)	LT1815S6/LT1816A, 40kΩ Between I_{SET} and V^-		2	7	mV
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●		9	mV
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		10	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ (Note 7)	●	10	15	μV/°C
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (Note 7)	●	10	30	μV/°C
I_{OS}	Input Offset Current	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		60	800	nA
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		1000	nA
			●		1200	nA
I_B	Input Bias Current	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		–2	±8	μA
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		±10	μA
			●		±12	μA

LT1815/LT1816/LT1817

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 8). $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. For the programmable current option (LT1815S6 or LT1816A), the I_{SET} pin must be connected to V^- through 75Ω or less, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1.3		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 3.5\text{V}$ Differential	1.5	5 750		$\text{M}\Omega$ $\text{k}\Omega$
C_{IN}	Input Capacitance			2		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR $T_A = -40^\circ\text{C}$ to 85°C	● ± 3.5 ± 3.5	± 4.2		V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 3.5\text{V}$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 75 73 72	85		dB dB dB
	Minimum Supply Voltage	Guaranteed by PSRR $T_A = -40^\circ\text{C}$ to 85°C	●	± 1.25	± 2 ± 2	V V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2\text{V}$ to $\pm 5.5\text{V}$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 78 76 75	97		dB dB dB
	Channel Separation	$V_{OUT} = \pm 3\text{V}$, $R_L = 100\Omega$, LT1816/LT1817 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 82 81 80	100		dB dB dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 3\text{V}$, $R_L = 500\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 1.5 1.0 0.8	3		V/mV V/mV V/mV
		$V_{OUT} = \pm 3\text{V}$, $R_L = 100\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 0.7 0.5 0.4	2.5		V/mV V/mV V/mV
V_{OUT}	Maximum Output Swing	$R_L = 500\Omega$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 3.8 ± 3.7 ± 3.6	± 4.1		V V V
		$R_L = 100\Omega$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 3.50 ± 3.25 ± 3.15	± 3.8		V V V
I_{OUT}	Maximum Output Current	$V_{OUT} = \pm 3\text{V}$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 50 ± 45 ± 40	± 80		mA mA mA
	Maximum Output Current (Low Power Mode) (Note 10)	LT1815S6/LT1816A; $40\text{k}\Omega$ Between I_{SET} and V^- ; $V_{OUT} = \pm 3\text{V}$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 50 ± 40 ± 30	± 75		mA mA mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0\text{V}$, 1V Overdrive (Note 3) $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 100 ± 90 ± 70	± 200		mA mA mA
SR	Slew Rate	$A_V = -1$ (Note 5) $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 900 750 600	1500		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$6V_{P-P}$ (Note 6)		80		MHz

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 8). $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. For the programmable current option (LT1815S6 or LT1816A), the I_{SET} pin must be connected to V^- through 75Ω or less, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GBW	Gain-Bandwidth Product	$f = 200\text{kHz}$, $R_L = 500\Omega$, LT1815 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 150 ● 140 ● 130	220		MHz MHz MHz
		$f = 200\text{kHz}$, $R_L = 500\Omega$, LT1816/LT1817 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 140 ● 130 ● 120	220		MHz MHz MHz
	Gain-Bandwidth Product (Low Power Mode) (Note 10)	LT1815S6/LT1816A; $40\text{k}\Omega$ Between I_{SET} and V^- ; $f = 200\text{kHz}$, $R_L = 500\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 35 ● 30 ● 25	55		MHz MHz MHz
-3dB BW	-3dB Bandwidth	$A_V = 1$, $R_L = 500\Omega$		350		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V , $R_L = 100\Omega$		1		ns
t_{PD}	Propagation Delay	$A_V = 1$, 50% to 50%, 0.1V , $R_L = 100\Omega$		1.4		ns
OS	Overshoot	$A_V = 1$, 0.1V ; $R_L = 100\Omega$		25		%
t_S	Settling Time	$A_V = -1$, 0.1%, 5V		15		ns
THD	Total Harmonic Distortion	$A_V = 2$, $f = 5\text{MHz}$, $V_{OUT} = 2V_{P-P}$, $R_L = 500\Omega$		-70		dB
dG	Differential Gain	$A_V = 2$, $V_{OUT} = 2V_{P-P}$, $R_L = 150\Omega$		0.08		%
dP	Differential Phase	$A_V = 2$, $V_{OUT} = 2V_{P-P}$, $R_L = 150\Omega$		0.04		Deg
R_{OUT}	Output Resistance	$A_V = 1$, $f = 1\text{MHz}$		0.20		Ω
I_S	Supply Current	LT1815 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	6.5	7 9 10	mA mA mA
		LT1816/LT1817, per Amplifier $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	6.5	7.8 10.5 11.5	mA mA mA
	Supply Current (Low Power Mode) (Note 10)	LT1815S6/LT1816A, $40\text{k}\Omega$ Between I_{SET} and V^- , per Amplifier $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	1	1.5 1.8 2.0	mA mA mA
I_{SET}	I_{SET} Pin Current (Note 10)	LT1815S6/LT1816A $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	-150 -175 -200	-100	μA μA μA

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 8). $V_S = 5\text{V}$, 0V ; $V_{CM} = 2.5\text{V}$, R_L to 2.5V , unless otherwise noted. For the programmable current option (LT1815S6 or LT1816A), the I_{SET} pin must be connected to V^- through 75Ω or less, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.4	2.0	mV
		$T_A = 0^\circ\text{C}$ to 70°C	●		2.5	mV
		$T_A = -40^\circ\text{C}$ to 85°C	●		3.5	mV
	Input Offset Voltage (Low Power Mode) (Note 10)	LT1815S6/LT1816A, $40\text{k}\Omega$ Between I_{SET} and V^-		2	7	mV
		$T_A = 0^\circ\text{C}$ to 70°C	●		9	mV
		$T_A = -40^\circ\text{C}$ to 85°C	●		10	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift	$T_A = 0^\circ\text{C}$ to 70°C (Note 7)	●	10	15	$\mu\text{V}/^\circ\text{C}$
		$T_A = -40^\circ\text{C}$ to 85°C (Note 7)	●	10	30	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	$T_A = 0^\circ\text{C}$ to 70°C	●	60	800	nA
		$T_A = -40^\circ\text{C}$ to 85°C	●		1000	nA
			●		1200	nA
I_B	Input Bias Current	$T_A = 0^\circ\text{C}$ to 70°C	●	-2.4	± 8	μA
		$T_A = -40^\circ\text{C}$ to 85°C	●		± 10 ± 12	μA μA
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1.3		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = 1.5\text{V}$ to 3.5V Differential		1.5	5	$\text{M}\Omega$
					750	$\text{k}\Omega$
C_{IN}	Input Capacitance			2		pF
V_{CM}	Input Voltage Range (High)	Guaranteed by CMRR		3.5	4.1	V
		$T_A = -40^\circ\text{C}$ to 85°C	●	3.5		V
	Input Voltage Range (Low)	Guaranteed by CMRR		0.9	1.5	V
		$T_A = -40^\circ\text{C}$ to 85°C	●		1.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5\text{V}$ to 3.5V		73	82	dB
		$T_A = 0^\circ\text{C}$ to 70°C	●	71		dB
		$T_A = -40^\circ\text{C}$ to 85°C	●	70		dB
	Channel Separation	$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 100\Omega$, LT1816/LT1817		81	100	dB
		$T_A = 0^\circ\text{C}$ to 70°C	●	80		dB
		$T_A = -40^\circ\text{C}$ to 85°C	●	79		dB
	Minimum Supply Voltage	Guaranteed by PSRR		2.5	4	V
		$T_A = -40^\circ\text{C}$ to 85°C	●		4	V
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 500\Omega$		1.0	2	V/mV
		$T_A = 0^\circ\text{C}$ to 70°C	●	0.7		V/mV
		$T_A = -40^\circ\text{C}$ to 85°C	●	0.6		V/mV
		$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 100\Omega$		0.7	1.5	V/mV
		$T_A = 0^\circ\text{C}$ to 70°C	●	0.5		V/mV
		$T_A = -40^\circ\text{C}$ to 85°C	●	0.4		V/mV
V_{OUT}	Maximum Output Swing (High)	$R_L = 500\Omega$, 30mV Overdrive		3.9	4.2	V
		$T_A = 0^\circ\text{C}$ to 70°C	●	3.8		V
		$T_A = -40^\circ\text{C}$ to 85°C	●	3.7		V
		$R_L = 100\Omega$, 30mV Overdrive		3.7	4	V
		$T_A = 0^\circ\text{C}$ to 70°C	●	3.6		V
		$T_A = -40^\circ\text{C}$ to 85°C	●	3.5		V
V_{OUT}	Maximum Output Swing (Low)	$R_L = 500\Omega$, 30mV Overdrive		0.8	1.1	V
		$T_A = 0^\circ\text{C}$ to 70°C	●		1.2	V
		$T_A = -40^\circ\text{C}$ to 85°C	●		1.3	V
		$R_L = 100\Omega$, 30mV Overdrive		1	1.3	V
		$T_A = 0^\circ\text{C}$ to 70°C	●		1.4	V
		$T_A = -40^\circ\text{C}$ to 85°C	●		1.5	V

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 8). $V_S = 5\text{V}$, 0V ; $V_{CM} = 2.5\text{V}$, R_L to 2.5V , unless otherwise noted. For the programmable current option (LT1815S6 or LT1816A), the I_{SET} pin must be connected to V^- through 75Ω or less, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{OUT}	Maximum Output Current	$V_{OUT} = 1.5\text{V}$ or 3.5V , 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	± 30 ± 25 ± 20	± 50	mA mA mA
	Maximum Output Current (Low Power Mode) (Note 10)	LT1815S6/LT1816A; $40\text{k}\Omega$ Between I_{SET} and V^- ; $V_{OUT} = 1.5\text{V}$ or 3.5V , 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	± 30 ± 25 ± 20	± 50	mA mA mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 2.5\text{V}$, 1V Overdrive (Note 3) $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	± 80 ± 70 ± 50	± 140	mA mA mA
SR	Slew Rate	$A_V = -1$ (Note 5) $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	450 375 300	750	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$2V_{P-P}$ (Note 6)		120		MHz
GBW	Gain-Bandwidth Product	$f = 200\text{kHz}$, $R_L = 500\Omega$, LT1815 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	140 130 120	200	MHz MHz MHz
		$f = 200\text{kHz}$, $R_L = 500\Omega$, LT1816/LT1817 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	130 110 100	200	MHz MHz MHz
	Gain-Bandwidth Product (Low Power Mode) (Note 10)	LT1815S6/LT1816A; $40\text{k}\Omega$ Between I_{SET} and V^- ; $f = 200\text{kHz}$, $R_L = 500\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	30 25 20	50	MHz MHz MHz
-3dB BW	-3dB Bandwidth	$A_V = 1$, $R_L = 500\Omega$		300		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90% , 0.1V , $R_L = 100\Omega$		1.2		ns
t_{PD}	Propagation Delay	$A_V = 1$, 50% to 50% , 0.1V , $R_L = 100\Omega$		1.5		ns
OS	Overshoot	$A_V = 1$, 0.1V ; $R_L = 100\Omega$		25		%
t_S	Settling Time	$A_V = -1$, 0.1% , 2V		15		ns
THD	Total Harmonic Distortion	$A_V = 2$, $f = 5\text{MHz}$, $V_{OUT} = 2V_{P-P}$, $R_L = 500\Omega$		-65		dB
dG	Differential Gain	$A_V = 2$, $V_{OUT} = 2V_{P-P}$, $R_L = 150\Omega$		0.08		%
dP	Differential Phase	$A_V = 2$, $V_{OUT} = 2V_{P-P}$, $R_L = 150\Omega$		0.13		Deg
R_{OUT}	Output Resistance	$A_V = 1$, $f = 1\text{MHz}$		0.24		Ω
I_S	Supply Current	LT1815 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	6.3	8 10 11	mA mA mA
		LT1816/LT1817, per Amplifier $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	6.3	9 12 13	mA mA mA
	Supply Current (Low Power Mode) (Note 10)	LT1815S6/LT1816A, $40\text{k}\Omega$ Between I_{SET} and V^- , per Amplifier $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ●	0.9	1.5 1.8 2.0	mA mA mA
I_{SET}	I_{SET} Pin Current (Note 10)	LT1815S6/LT1816A $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	-150 -175 -200	-100	μA μA μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Differential inputs of $\pm 6\text{V}$ are appropriate for transient operation only, such as during slewing. Large sustained differential inputs can cause excessive power dissipation and may damage the part.

ELECTRICAL CHARACTERISTICS

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between $\pm 2V$ at the output with $\pm 3V$ input for $\pm 5V$ supplies and $2V_{P-P}$ at the output with a $3V_{P-P}$ input for single 5V supplies.

Note 6: Full-power bandwidth is calculated from the slew rate:

$$FPBW = SR/2\pi V_P$$

Note 7: This parameter is not 100% tested.

Note 8: The LT1815C/LT1816C/LT1817C are guaranteed to meet specified performance from $0^\circ C$ to $70^\circ C$ and are designed, characterized and

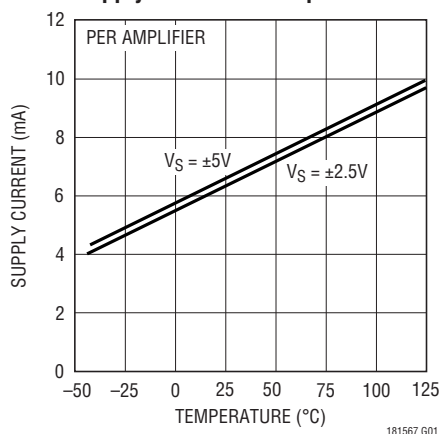
expected to meet the extended temperature limits, but are not tested at $-40^\circ C$ and $85^\circ C$. The LT1815I/LT1816I/LT1817I are guaranteed to meet the extended temperature limits.

Note 9: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be substantially reduced by connecting Pin 2 of the TSOT-23, Pin 4 of the SO-8 and MS8, Pin 5 of the MS10 or the underside metal of the DD package to a large metal area.

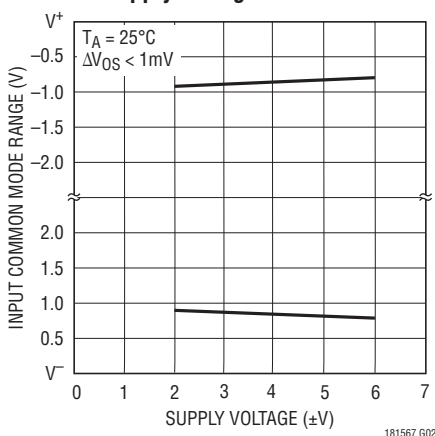
Note 10: A resistor of 40k or less is required between the I_{SET} and V^- pins of the LT1815S6 and the LT1816AMS. See the Applications Information section for information on selecting a suitable resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

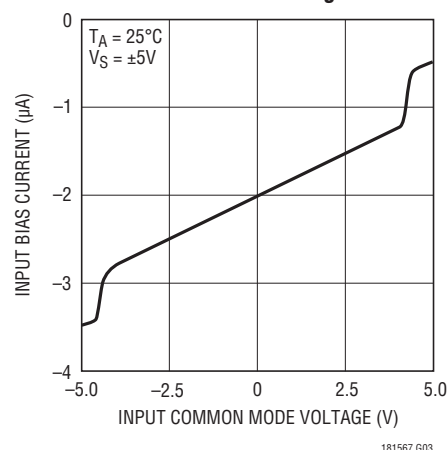
Supply Current vs Temperature



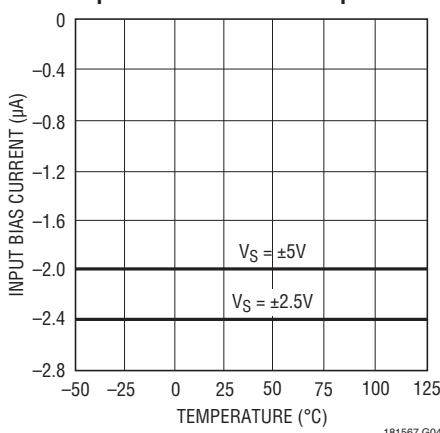
Input Common Mode Range vs Supply Voltage



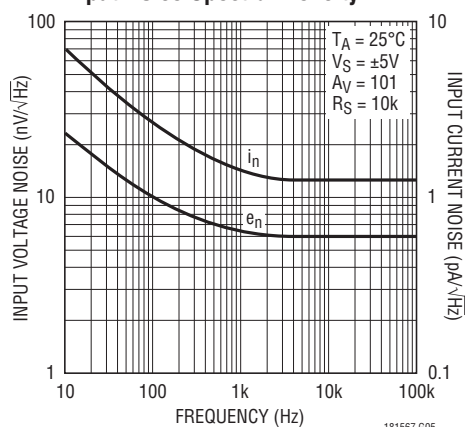
Input Bias Current vs Common Mode Voltage



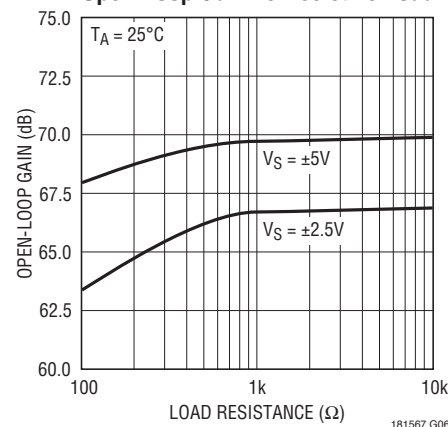
Input Bias Current vs Temperature



Input Noise Spectral Density

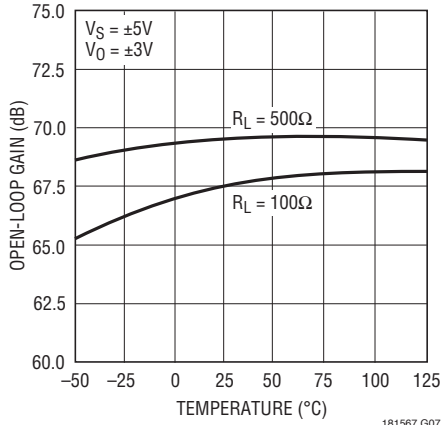


Open-Loop Gain vs Resistive Load

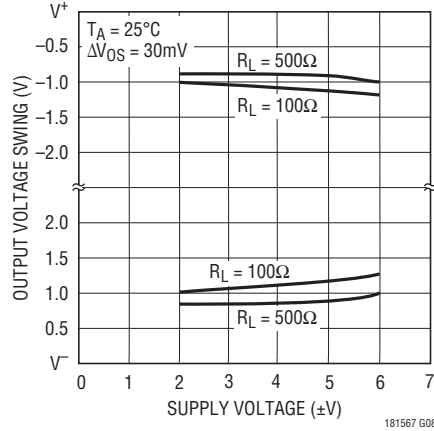


TYPICAL PERFORMANCE CHARACTERISTICS

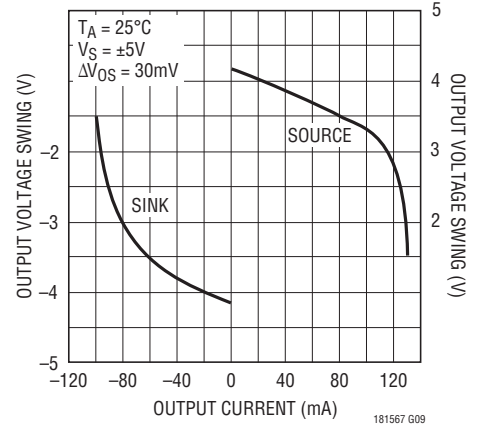
Open-Loop Gain vs Temperature



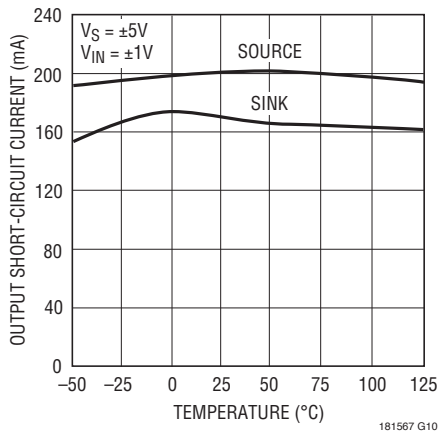
Output Voltage Swing vs Supply Voltage



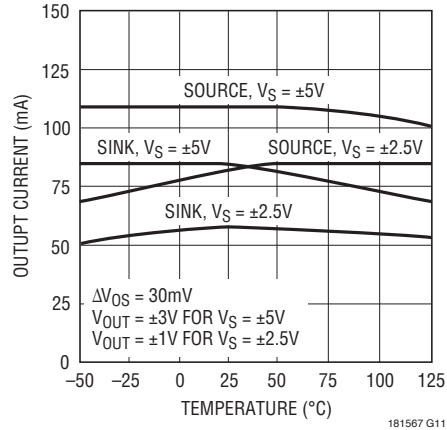
Output Voltage Swing vs Load Current



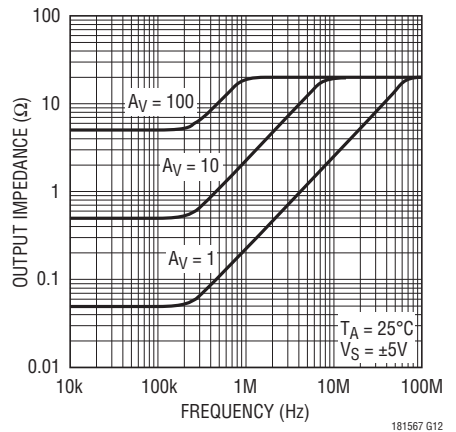
Output Short-Circuit Current vs Temperature



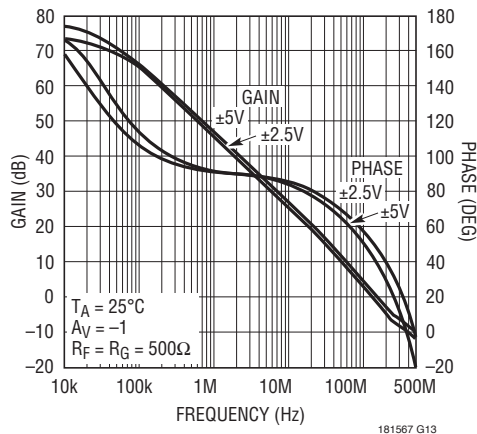
Output Current vs Temperature



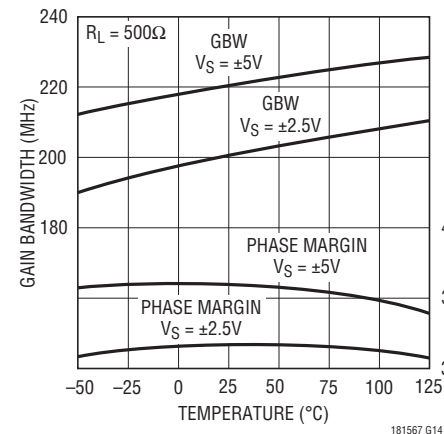
Output Impedance vs Frequency



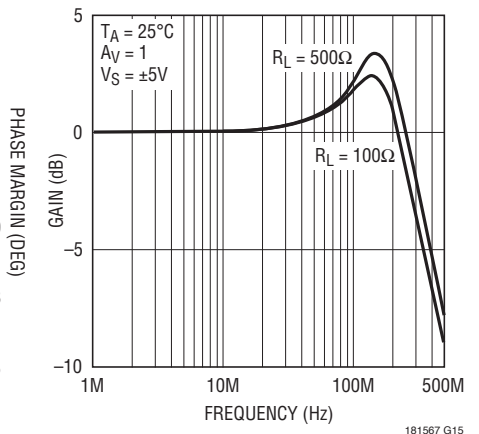
Gain and Phase vs Frequency



Gain Bandwidth and Phase Margin vs Temperature

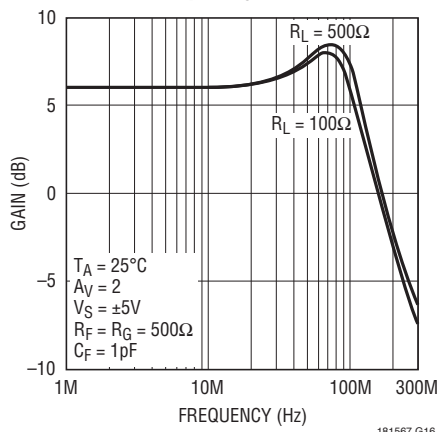


Gain vs Frequency, $A_V = 1$

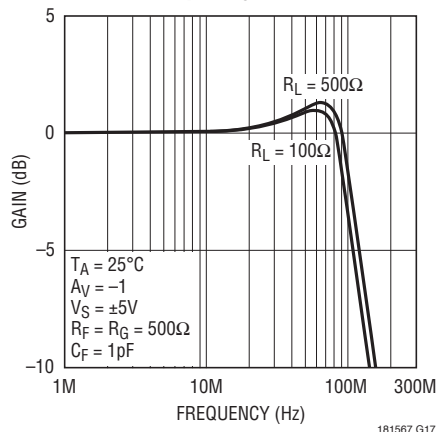


TYPICAL PERFORMANCE CHARACTERISTICS

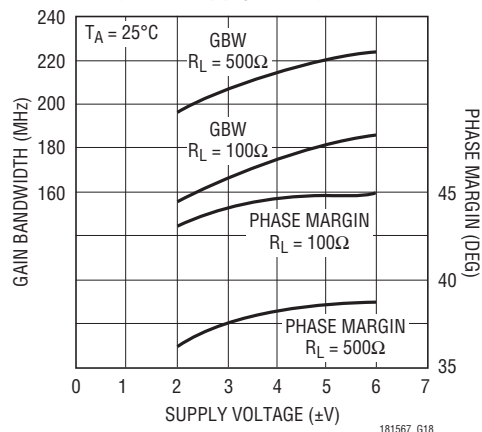
Gain vs Frequency, $A_V = 2$



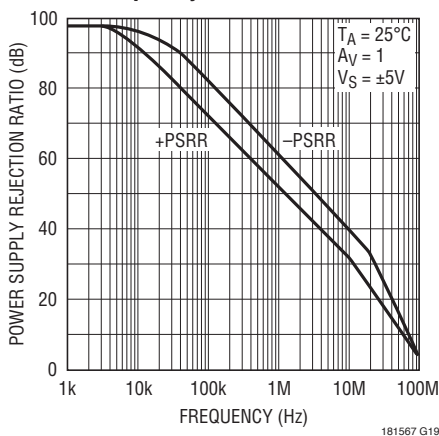
Gain vs Frequency, $A_V = -1$



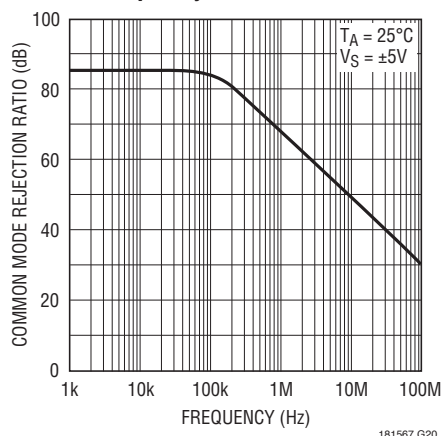
Gain Bandwidth and Phase Margin vs Supply Voltage



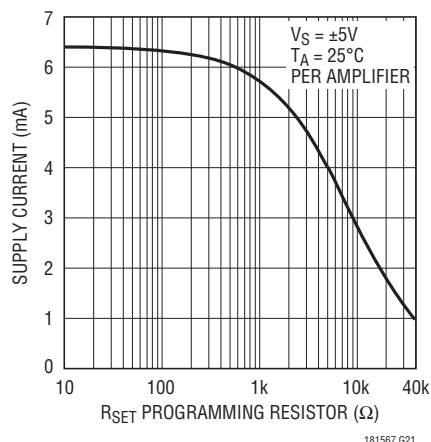
Power Supply Rejection Ratio vs Frequency



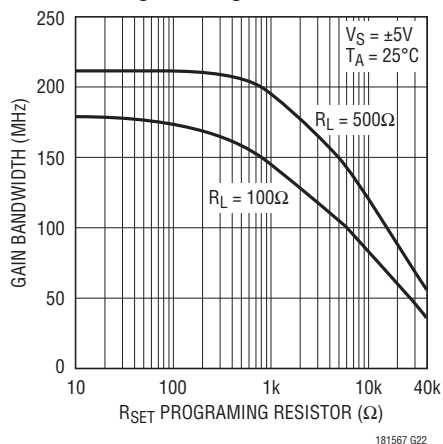
Common Mode Rejection Ratio vs Frequency



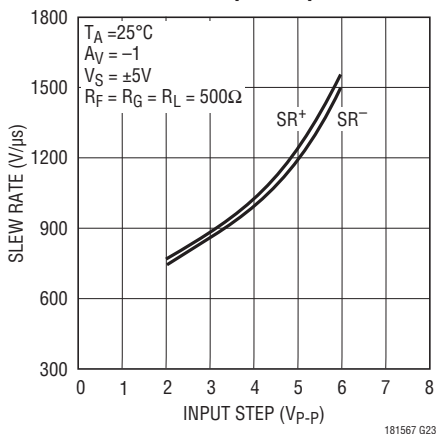
Supply Current vs Programming Resistor



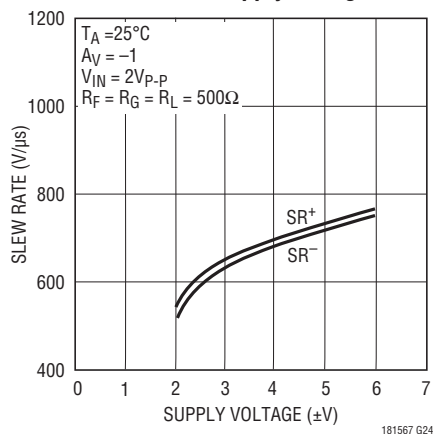
Gain Bandwidth Product vs Programming Resistor



Slew Rate vs Input Step

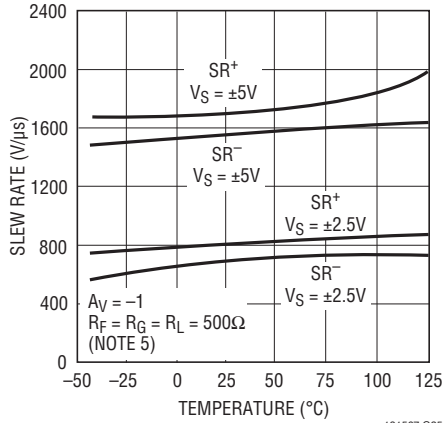


Slew Rate vs Supply Voltage

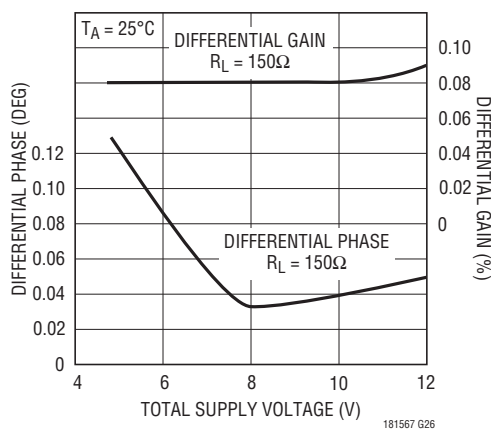


TYPICAL PERFORMANCE CHARACTERISTICS

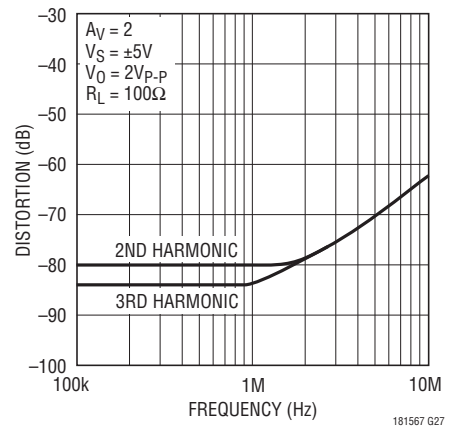
Slew Rate vs Temperature



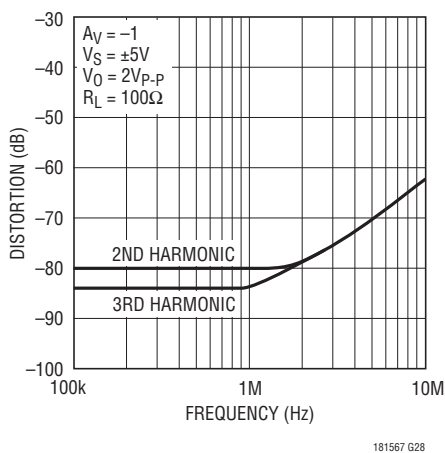
Differential Gain and Phase vs Supply Voltage



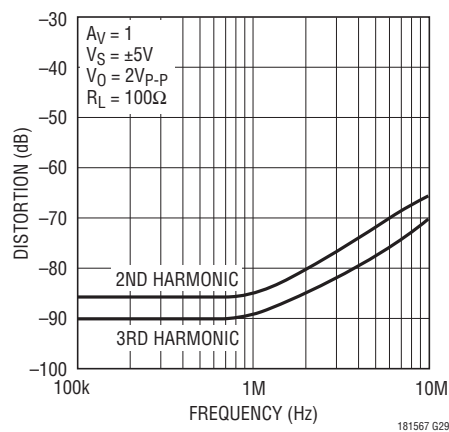
Distortion vs Frequency, $A_V = 2$



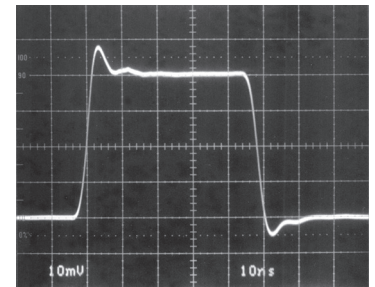
Distortion vs Frequency, $A_V = -1$



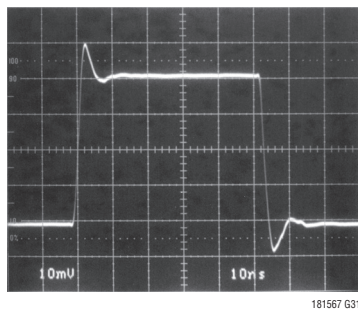
Distortion vs Frequency, $A_V = 1$



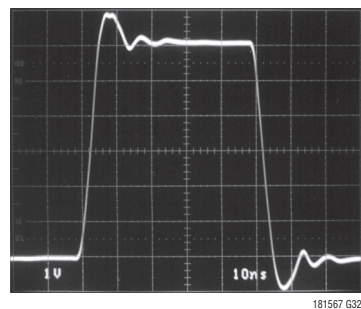
Small-Signal Transient, $A_V = -1$



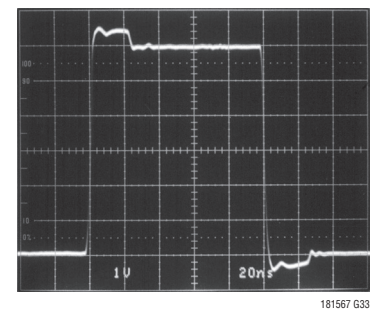
Small-Signal Transient, $A_V = 1$



Large-Signal Transient, $A_V = -1$, $V_S = ±5V$



Large-Signal Transient, $A_V = 1$, $V_S = ±5V$



APPLICATIONS INFORMATION

Layout and Passive Components

As with all high speed amplifiers, the LT1815/LT1816/LT1817 require some attention to board layout. A ground plane is recommended and trace lengths should be minimized, especially on the negative input lead.

Low ESL/ESR bypass capacitors should be placed directly at the positive and negative supply (0.01μF ceramics are recommended). For high drive current applications, additional 1μF to 10μF tantalums should be added.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. If feedback resistors greater than 1k are used, a parallel capacitor of value:

$$C_F > R_G \cdot C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is 1 and a large feedback resistor is used, C_F should be greater than or equal to C_{IN} . An example would be an I-to-V converter.

Input Considerations

The inputs of the LT1815/LT1816/LT1817 amplifiers are connected to the base of an NPN and PNP bipolar transistor in parallel. The base currents are of opposite polarity and provide first-order bias current cancellation. Due to variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current, however, does not depend on beta matching and is tightly controlled. Therefore, the use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. For example, with a 100Ω source resistance at each input, the 800nA maximum offset current results in only 80μV of extra offset, while without balance the 8μA maximum input bias current could result in a 0.8mV offset contribution.

The inputs can withstand differential input voltages of up to 6V without damage and without needing clamping or series resistance for protection. This differential input voltage generates a large internal current (up to 80mA), which results in the high slew rate. In normal transient

closed-loop operation, this does not increase power dissipation significantly because of the low duty cycle of the transient inputs. Sustained differential inputs, however, will result in excessive power dissipation and therefore **this device should not be used as a comparator.**

Capacitive Loading

The LT1815/LT1816/LT1817 are optimized for high bandwidth and low distortion applications. They can drive a capacitive load of 10pF in a unity-gain configuration and more with higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability.

Slew Rate

The slew rate of the LT1815/LT1816/LT1817 is proportional to the differential input voltage. Therefore, highest slew rates are seen in the lowest gain configurations. For example, a 5V output step in a gain of 10 has a 0.5V input step, whereas in unity gain there is a 5V input step. The LT1815/LT1816/LT1817 are tested for a slew rate in a gain of -1. Lower slew rates occur in higher gain configurations.

Programmable Supply Current (LT1815/LT1816A)

In order to operate the LT1815S6 or LT1816A at full speed (and full supply current), connect the I_{SET} pin to the negative supply through a resistance of 75Ω or less.

To adjust or program the supply current and speed of the LT1815S6 or LT1816A, connect an external resistor (R_{SET}) between the I_{SET} pin and the negative supply, as shown in Figure 1. The amplifiers are fully functional with $0 \leq R_{SET} \leq 40k$. Figures 2 and 3 show how the gain bandwidth and supply current vary with the value of the programming resistor R_{SET} . In addition, the Electrical Characteristics section of the data sheet specifies maximum supply current and offset voltage, as well as minimum gain bandwidth and output current at the maximum R_{SET} value of 40k.

APPLICATIONS INFORMATION

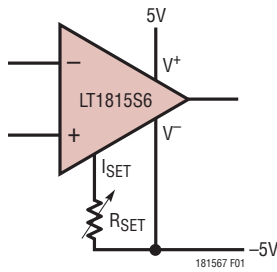


Figure 1. Programming Resistor Between I_{SET} and V^-

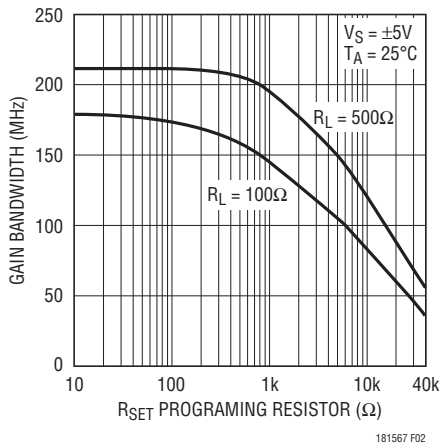


Figure 2. Gain Bandwidth Product vs R_{SET} Programming Resistor

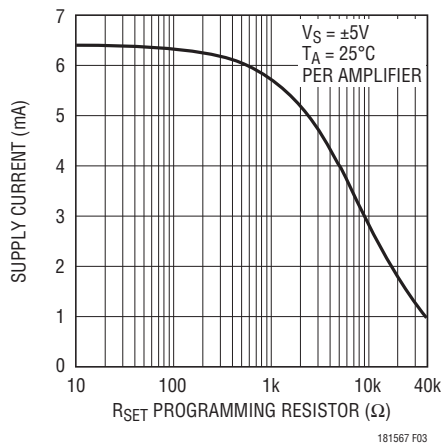


Figure 3. Supply Current vs R_{SET} Programming Resistor

Power Dissipation

The LT1815/LT1816/LT1817 combine high speed and large output drive in small packages. It is possible to exceed the maximum junction temperature specification (150°C) under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A), power dissipation per amplifier (P_D) and number of amplifiers (n) as follows:

$$T_J = T_A + (n \cdot P_D \cdot \theta_{JA})$$

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current. The worst-case load induced power occurs when the output voltage is at one-half of either supply voltage (or the maximum swing if less than one-half the supply voltage). Therefore, P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-) \cdot (I_{SMAX}) + (V^+/2)^2/R_L \text{ or}$$

$$P_{DMAX} = (V^+ - V^-) \cdot (I_{SMAX}) + (V^+ - V_{OMAX}) \cdot (V_{OMAX}/R_L)$$

Example: LT1816IS8 at 85°C, $V_S = \pm 5V$, $R_L = 100\Omega$

$$P_{DMAX} = (10V) \cdot (11.5mA) + (2.5V)^2/100\Omega = 178mW$$

$$T_{JMAX} = 85^\circ C + (2 \cdot 178mW) \cdot (150^\circ C/W) = 138^\circ C$$

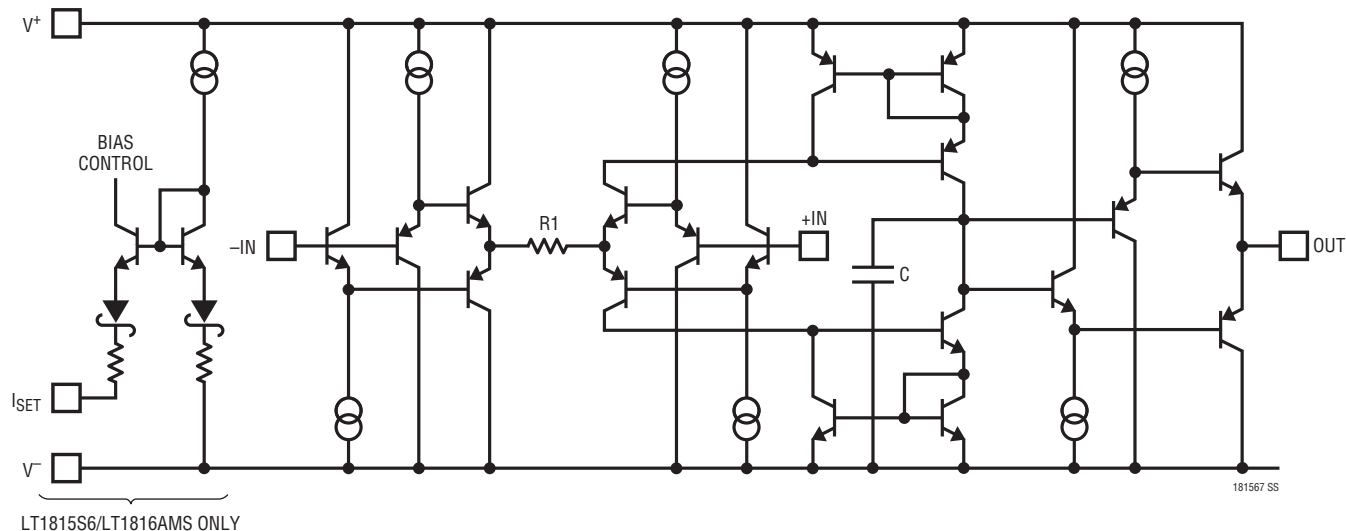
Circuit Operation

The LT1815/LT1816/LT1817 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. Complementary NPN and PNP emitter followers buffer the inputs and drive an internal resistor. The input voltage appears across the resistor, generating current that is mirrored into the high impedance node.

Complementary followers form an output stage that buffers the gain node from the load. The input resistor, input stage transconductance and the capacitor on the high impedance node determine the bandwidth. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R_1 , so the slew rate is proportional to the input step. Highest slew rates are therefore seen in the lowest gain configurations.

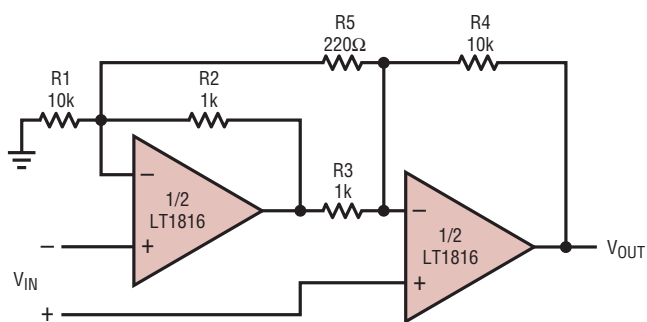
LT1815/LT1816/LT1817

SIMPLIFIED SCHEMATIC (One Amplifier)



TYPICAL APPLICATIONS

Two Op Amp Instrumentation Amplifier



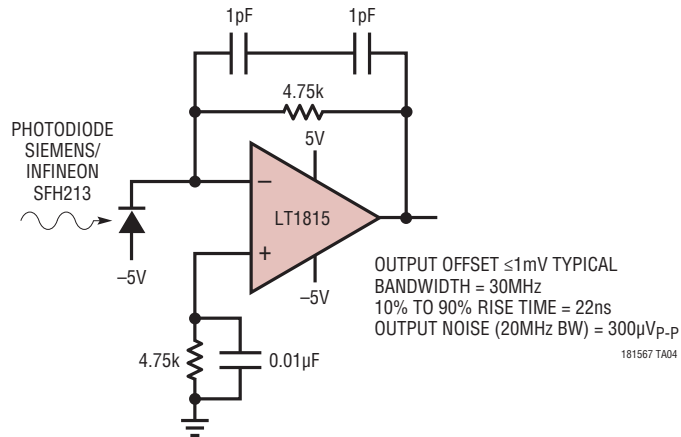
$$\text{GAIN} = \left[\frac{R4}{R3} \right] \left[1 + \left(\frac{1}{2} \right) \left(\frac{R2}{R1} + \frac{R3}{R4} \right) + \frac{(R2 + R3)}{R5} \right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 2MHz

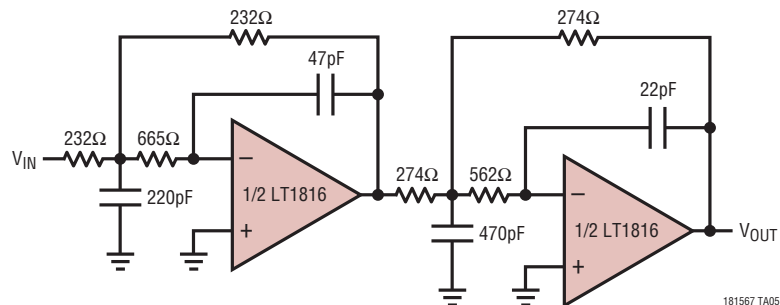
181567 TA03

TYPICAL APPLICATIONS

Photodiode Transimpedance Amplifier

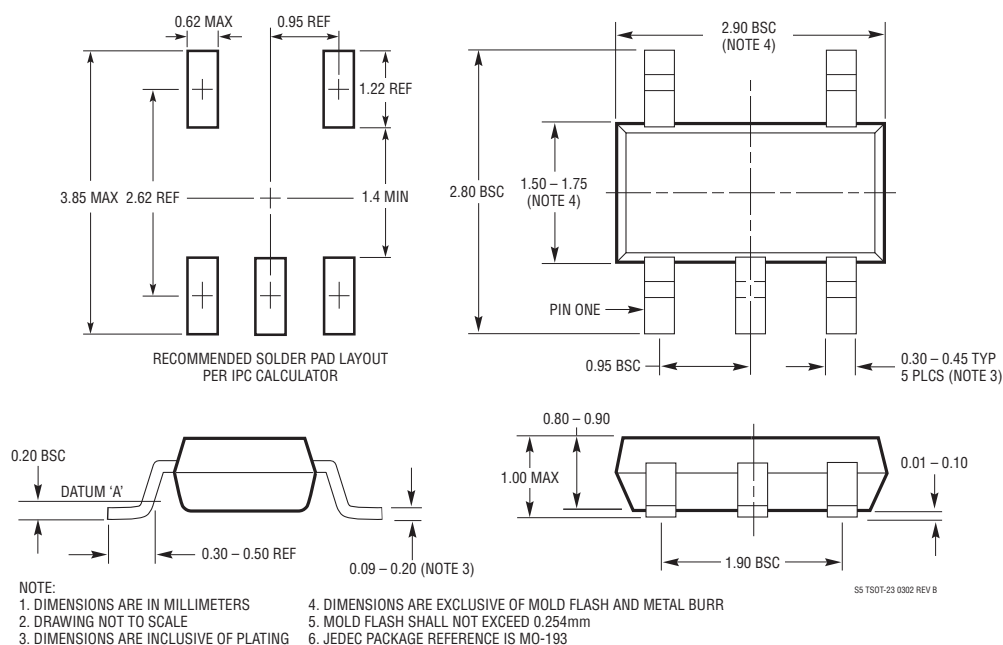


4MHz, 4th Order Butterworth Filter

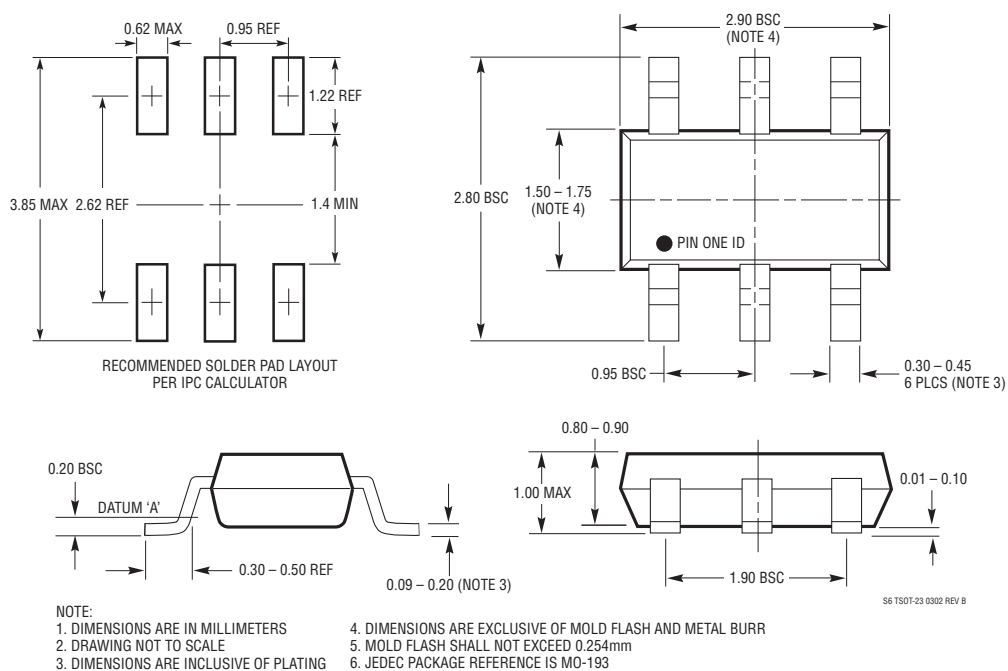


PACKAGE DESCRIPTION

S5 Package 5-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1635)

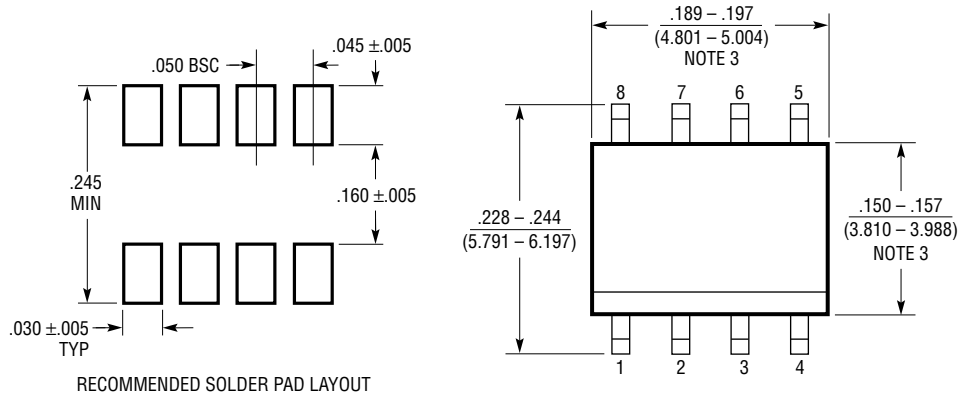


S6 Package 6-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1636)



PACKAGE DESCRIPTION

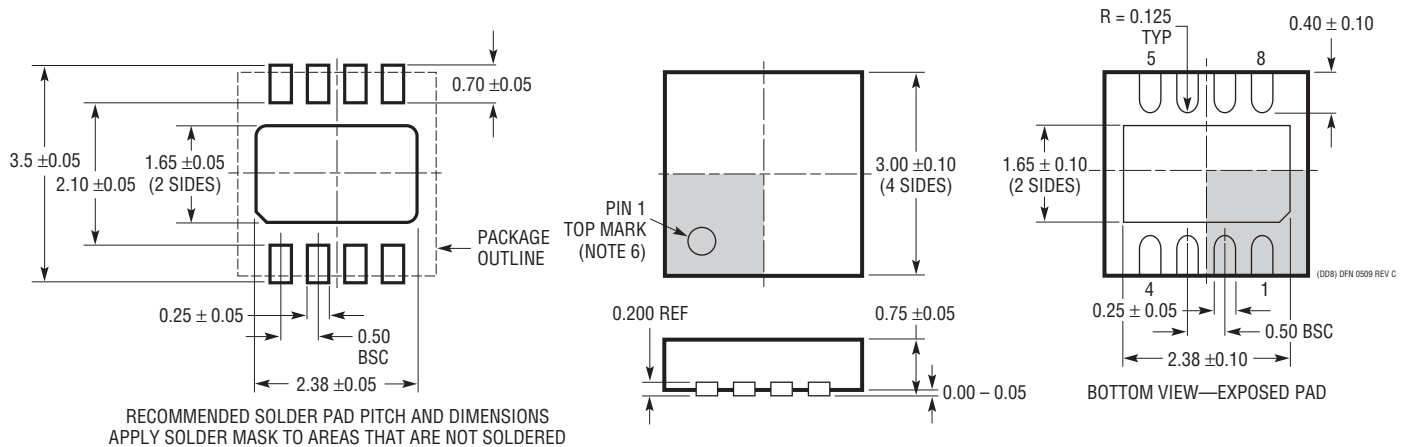
S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

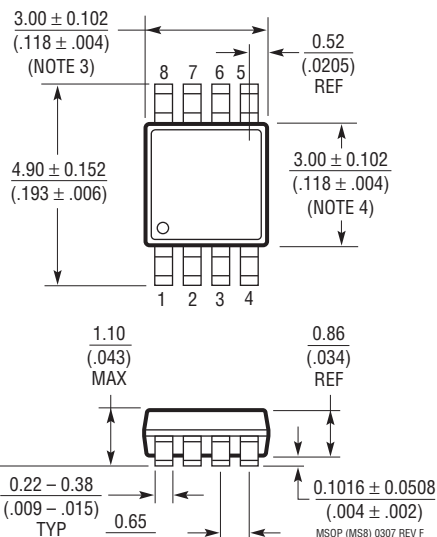
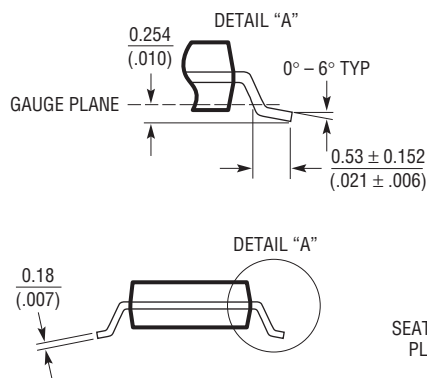
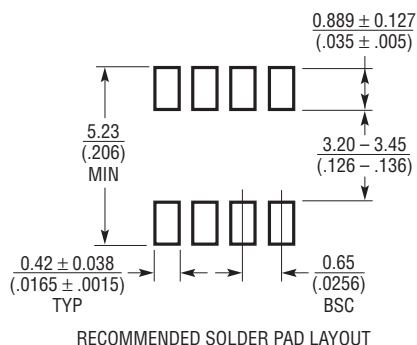
DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698 Rev C)



PACKAGE DESCRIPTION

MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev F)



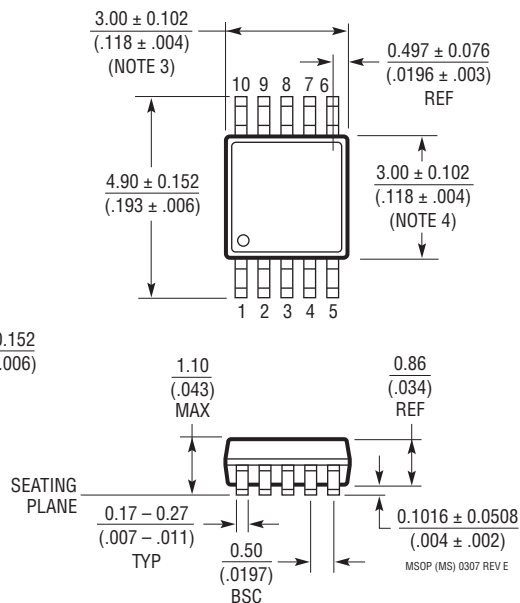
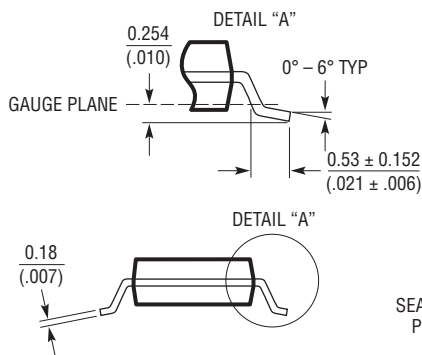
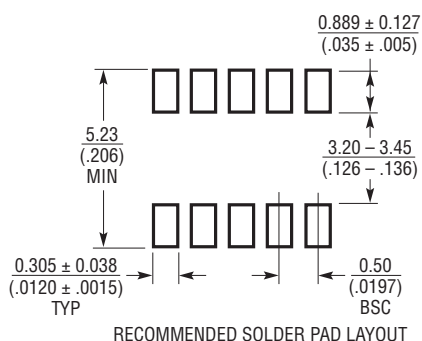
NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm ($.004$) MAX

MS Package 10-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1661 Rev E)



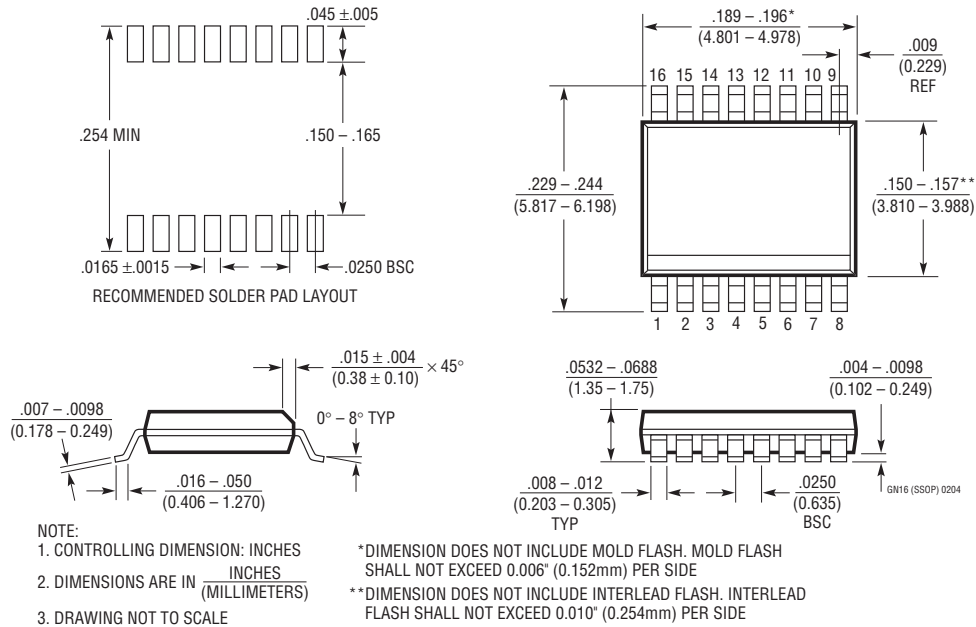
NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE

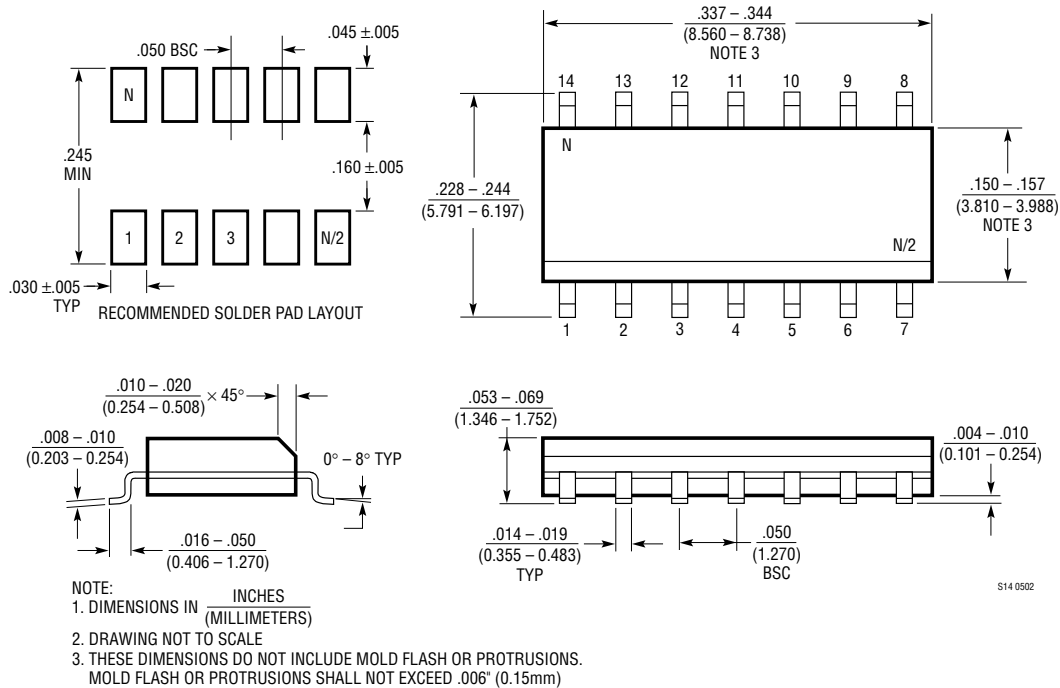
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm ($.004$) MAX

PACKAGE DESCRIPTION

GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



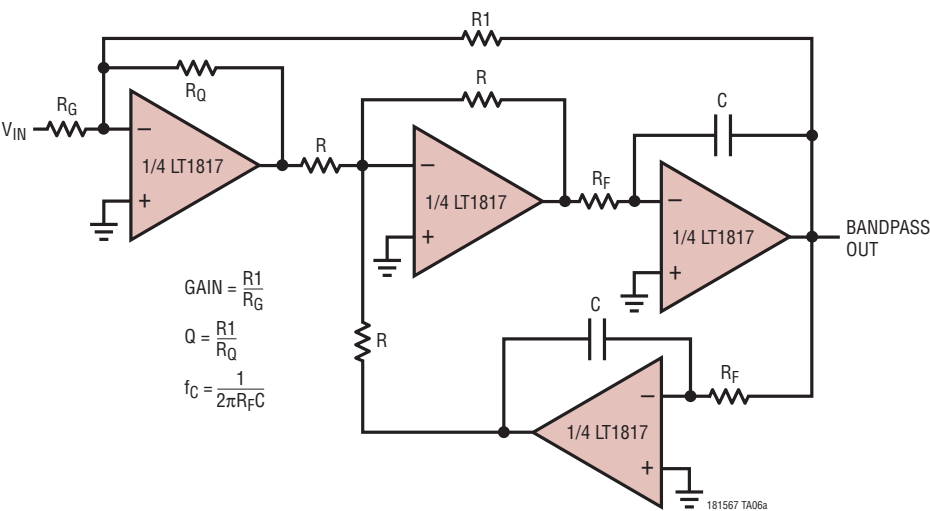
S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



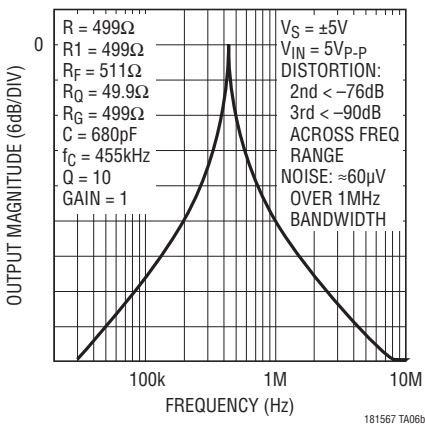
LT1815/LT1816/LT1817

TYPICAL APPLICATION

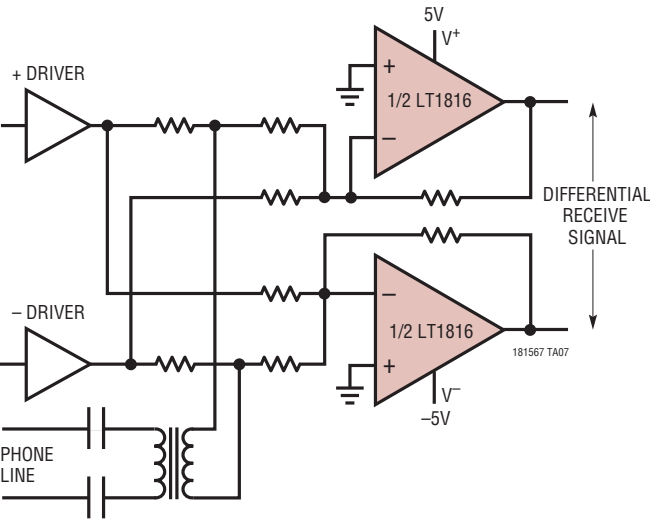
Bandpass Filter with Independently Settable Gain, Q and f_c



455kHz Filter Frequency Response



Differential DSL Receiver



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1363/LT1364/LT1365	Single/Dual/Quad 70MHz, 1V/ns, C-Load™ Op Amps	Wide Supply Range: $\pm 2.5V$ to $\pm 15V$
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	4.6mA Supply Current, 800V/ μs , 80mA Output Current
LT1806/LT1807	Single/Dual 325MHz, 140V/ μs Rail-to-Rail I/O Op Amps	Low Noise: 3.5nV/ $\sqrt{Hz}$
LT1809/LT1810	Single/Dual 180MHz, 350V/ μs Rail-to-Rail I/O Op Amps	Low Distortion: 90dBc at 5MHz
LT1812/LT1813/LT1814	Single/Dual/Quad 3mA, 100MHz, 750V/ μs Op Amps	Low Power: 3.6mA Max at $\pm 5V$

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