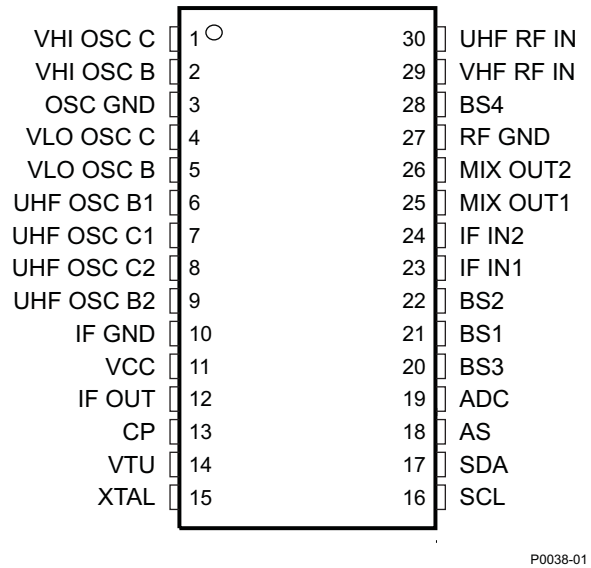
## FEATURES

- **Single-Chip Mixer/Oscillator and Phase-Locked Loop (PLL) Synthesizer**
- **Three-Band Local Oscillator**
- **I²C Bus Protocol (Bidirectional Data Transmission)**
- **30-V Tuning Voltage Output**
- **Four NPN-Type Band-Switch Drivers**
- **Programmable Reference Divider Ratio (512, 640, or 1024)**
- **External 4-Pin Intermediate Frequency (IF) Filter Between Mixer Output and IF Amplifier Input**
- **5-V Power Supply**
- **30-Pin Thin Shrink Small-Outline Package (TSSOP)**

**DBT PACKAGE**
**(TOP VIEW)**




P0038-01

## APPLICATIONS

- **TVs**
- **VCR/DVD Recorders**
- **Set-Top Boxes**

## DESCRIPTION

The SN761678B is a synthesized tuner IC designed for TV tuning systems. The circuit consists of a phase-locked loop (PLL) synthesizer, three-band local oscillator and mixer, 30-V output tuning amplifier, and four NPN band-switch drivers. The device is available in a small-outline package. A 15-bit programmable counter and reference divider are controlled by I²C bus protocol. Tuning step frequency is selectable by this reference divider ratio for a crystal oscillator.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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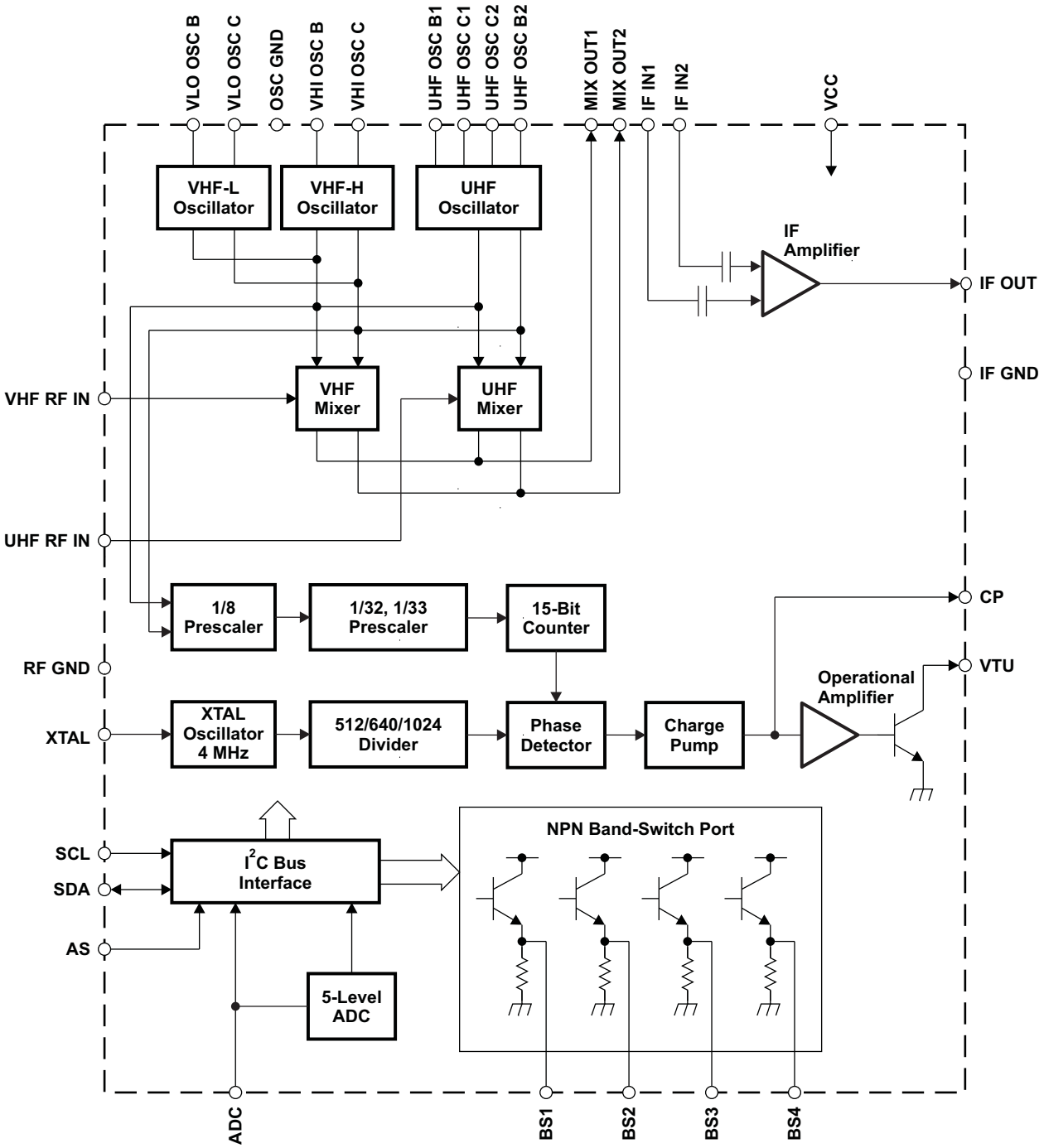
## FUNCTIONAL BLOCK DIAGRAM

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## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | DESCRIPTION | SCHEMATIC |
|---|---|---|---|
| ADC | 19 | ADC input | Figure 1 |
| AS | 18 | Address selection input | Figure 2 |
| BS1 | 21 | Band-switch 1 output (NPN emitter follower) | Figure 4 |
| BS2 | 22 | Band-switch 2 output (NPN emitter follower) | Figure 4 |
| BS3 | 20 | Band-switch 3 output (NPN emitter follower) | Figure 4 |
| BS4 | 28 | Band-switch 4 output (NPN emitter follower) | Figure 4 |
| CP | 13 | Charge-pump output | Figure 5 |
| IF GND | 10 | IF ground | |
| IF IN1 | 23 | IF amplifier input 1 | Figure 3 |
| IF IN2 | 24 | IF amplifier input 2 | Figure 3 |
| IF OUT | 12 | IF output | Figure 6 |
| MIX OUT1 | 25 | Mixer output 1 | Figure 7 |
| MIX OUT2 | 26 | Mixer output 2 | Figure 7 |
| OSC GND | 3 | Oscillator ground | |
| RF GND | 27 | RF ground | |
| SCL | 16 | Serial clock input | Figure 8 |
| SDA | 17 | Serial data input/output | Figure 9 |
| UHF OSC B1 | 6 | UHF oscillator base 1 | Figure 10 |
| UHF OSC B2 | 9 | UHF oscillator base 2 | Figure 10 |
| UHF OSC C1 | 7 | UHF oscillator collector 1 | Figure 10 |
| UHF OSC C2 | 8 | UHF oscillator collector 2 | Figure 10 |
| UHF RF IN | 30 | UHF RF input | Figure 11 |
| VCC | 11 | Supply voltage for mixer/oscillator/PLL: 5 V | |
| VHF RF IN | 29 | VHF RF input | Figure 12 |
| VHI OSC B | 2 | VHF HIGH oscillator base | Figure 13 |
| VHI OSC C | 1 | VHF HIGH oscillator collector | Figure 13 |
| VLO OSC B | 5 | VHF LOW oscillator base | Figure 14 |
| VLO OSC C | 4 | VHF LOW oscillator collector | Figure 14 |
| VTU | 14 | Tuning voltage amplifier output | Figure 15 |
| XTAL | 15 | 4-MHz crystal oscillator input | Figure 16 |

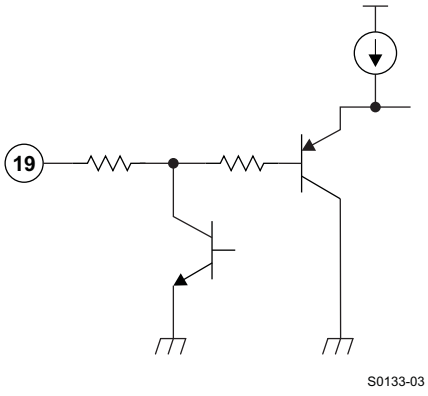



**Figure 1.**

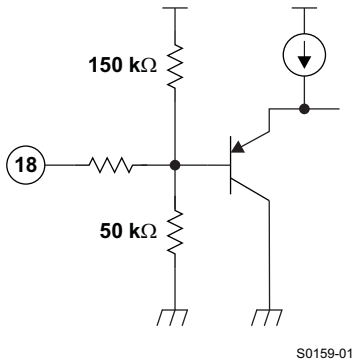
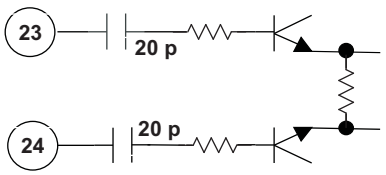



**Figure 2.**

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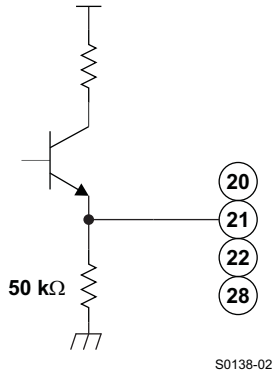



Figure 4.

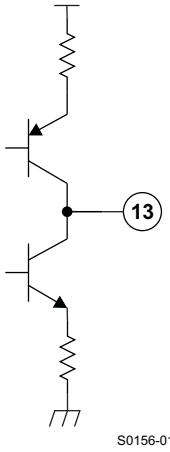



Figure 5.

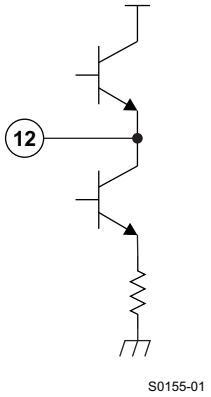



Figure 6.

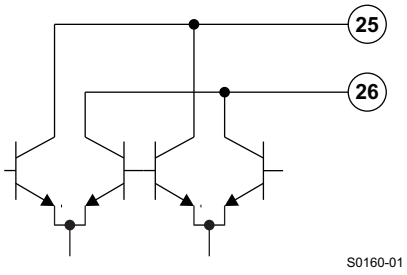



Figure 7.

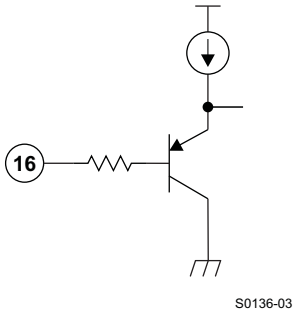



Figure 8.

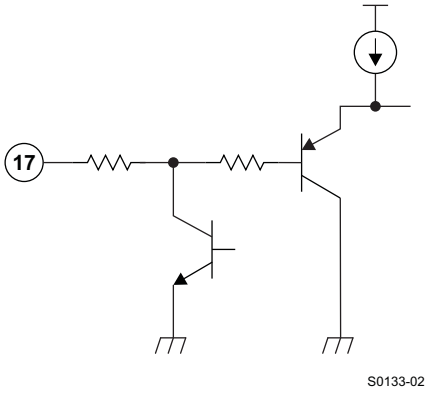



Figure 9.

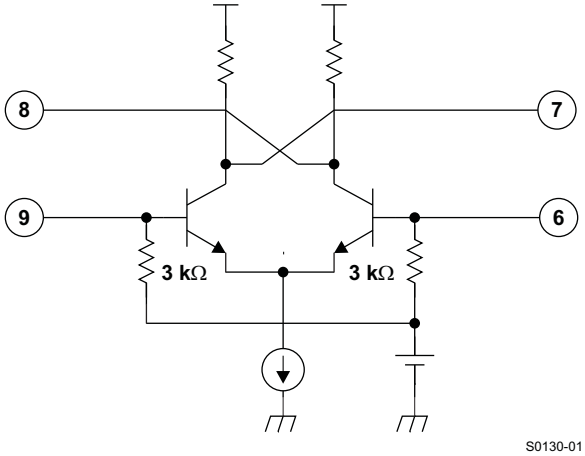



Figure 10.

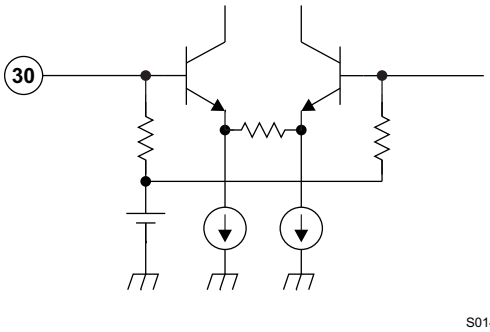



Figure 11.

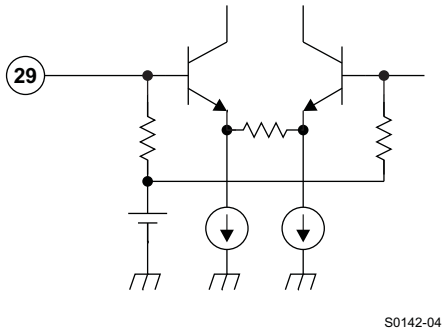



Figure 12.

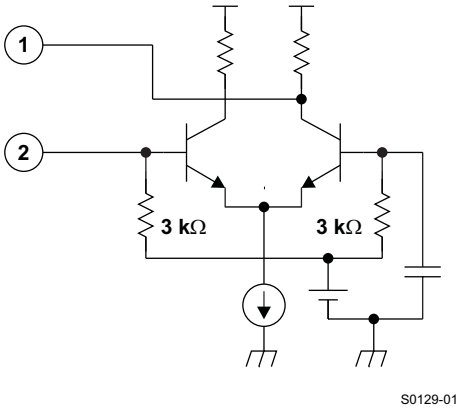



Figure 13.

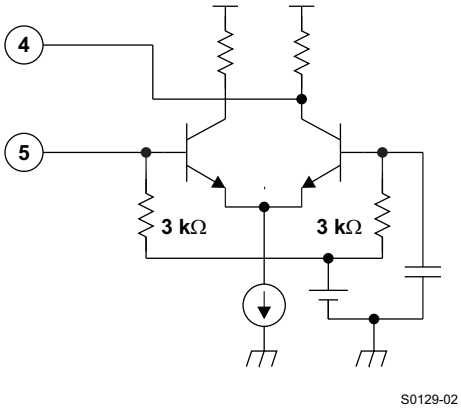



Figure 14.

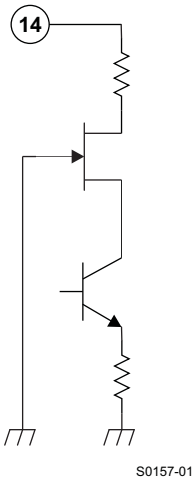



Figure 15.

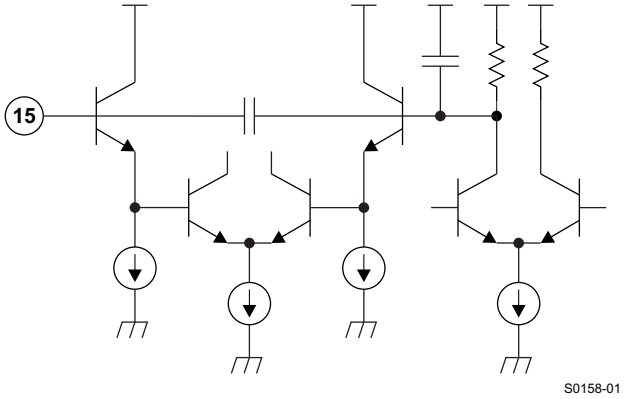



Figure 16.

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ (2) | VCC (pin 11) | –0.4 V to 6.5 V |
| Input voltage 1, $V_{GND}$ (2) | OSC GND, RF GND (pins 3, 27) | –0.4 V to 0.4 V |
| Input voltage 2, $V_{VTU}$ (2) | VTU (pin 14) | –0.4 V to 35 V |
| Input voltage 3, $V_{IN}$ (2) | Other pins (1, 2, 4–9, 12, 13, 15–26, 28–30) | –0.4 V to 6.5 V |
| Continuous total dissipation, $P_D$ (3) | $T_A \leq 25°C$ | 1071 mW |
| Operating free-air temperature range, $T_A$ | | –20°C to 85°C |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |
| Maximum junction temperature, $T_J$ | | 150°C |
| Maximum short-circuit time, $t_{SC(max)}$ | Each pin to $V_{CC}$ or to GND | 10 s |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 8.57 mW/°C for $T_A \geq 25°C$.

## Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | V |
| Tuning supply voltage, $V_{TU}$ | | | 30 | 33 | V |
| Output current of band switch, $I_{BS}$ | One port on | | | 10 | mA |
| Operating free-air temperature, $T_A$ | | –20 | | 85 | °C |

## Electrical Characteristics – Total Device and Serial Interface

$V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –20°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}1$ | Supply current 1 | | | 60 | | mA |
| $I_{CC}2$ | Supply current 2 | One band switch on ($I_{BS}$ = 10 mA) | | 70 | | mA |
| $V_{IH}$ | High-level input voltage (SCL, SDA) | | 2.8 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (SCL, SDA) | | | | 1.4 | V |
| $I_{IH}$ | High-level input current (SCL, SDA) | | | | 10 | µA |
| $I_{IL}$ | Low-level input current (SCL, SDA) | | –10 | | | µA |
| $V_{POR}$ | Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode) | | 2.1 | 2.8 | 3.6 | V |
| **I²C Interface** | | | | | | |
| $V_{ASH}$ | Address-select high-input voltage (AS) | $V_{CC}$ = 5 V | 4.5 | | 5 | V |
| $V_{ASM1}$ | Address-select mid1-input voltage (AS) | $V_{CC}$ = 5 V | 2 | | 3 | V |
| $V_{ASM2}$ | Address-select mid2-input voltage (AS) | $V_{CC}$ = 5 V | 1 | | 1.5 | V |
| $V_{ASL}$ | Address-select low-input voltage (AS) | $V_{CC}$ = 5 V | | | 0.5 | V |
| $I_{ASH}$ | Address-select high-input current (AS) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | 140 | µA |
| $I_{ASL}$ | Address-select low-input current (AS) | $V_{CC}$ = 5 V, $T_A$ = 25°C | –50 | | | µA |
| $V_{ADC}$ | ADC input voltage | See Table 8 | 0 | | $V_{CC}$ | V |
| $I_{ADH}$ | ADC high-level input current | $V_{ADC}$ = $V_{CC}$ | | | 10 | µA |
| $I_{ADL}$ | ADC low-level input current | $V_{ADC}$ = 0 V | –50 | | | µA |
| $V_{OL}$ | Low-level output voltage (SDA) | $V_{CC}$ = 5 V, $I_{OL}$ = 3 mA | | | 0.4 | V |
| $I_{SDAH}$ | High-level output leakage current (SDA) | $V_{SDA}$ = 5.5 V | | | 10 | µA |
| $f_{SCL}$ | Clock frequency (SCL) | | | 100 | 400 | kHz |
| | **I²C Timing (see Figure 17)** | | | | | |
| $t_{hd(DAT)}$ | Data hold time | | 0 | | | µs |
| $t_{(BUF)}$ | Bus free time | | 1.3 | | | µs |
| $t_{hd(STA)}$ | Start hold time | | 0.6 | | | µs |
| $t_{(Low)}$ | SCL-low hold time | | 1.3 | | | µs |
| $t_{(High)}$ | SCL-high hold time | | 0.6 | | | µs |
| $t_{su(STA)}$ | Start setup time | | 0.6 | | | µs |
| $t_{su(DAT)}$ | Data setup time | | 0.1 | | | µs |
| $t_r$ | SCL, SDA rise time | | | | 0.3 | µs |
| $t_f$ | SCL, SDA fall time | | | | 0.3 | µs |
| $t_{su(STO)}$ | Stop setup time | | 0.6 | | | µs |

## Electrical Characteristics – PLL and Band Switch

$V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –20°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| N | Divider ratio | 15-bit frequency word | 256 | | 32767 | |
| $f_{XTAL}$ | Crystal oscillator frequency | $R_{XTAL}$ = 25 Ω to 300 Ω | 3.2 | 4 | 4.48 | MHz |
| $Z_{XTAL}$ | Crystal oscillator input impedance | | | 1.6 | | kΩ |
| $V_{IXTAL2}$ | Minimum reference input sensitivity (XTAL) | 4 MHz, ac coupling with 0.1-µF capacitor | | | 100 | mVp-p |
| $V_{VTUL}$ | Tuning amplifier low-level output voltage | $R_L$ = 22 kΩ, $V_{TU}$ = 33 V | | 0.4 | 0.5 | V |
| $I_{VTUOFF}$ | Tuning amplifier leakage current (off) | OS = 1, $V_{TU}$ = 33 V | | | 10 | µA |
| $I_{CPH}$ | Charge-pump high-level input current | CP = 1 | | 280 | | µA |
| $I_{CPL}$ | Charge-pump low-level input current | CP = 0 | | 60 | | µA |
| $V_{CP}$ | Charge-pump output voltage | PLL locked | | 1.95 | | V |
| $I_{CPOFF}$ | Charge-pump leakage current | T2 = 0, T1 = 1, $V_{CP}$ = 2 V, $T_A$ = 25°C | –15 | | 15 | nA |
| $I_{BS}$ | Band-switch driver output current | | | | 10 | mA |
| $V_{BS1}$ | Band-switch driver output voltage | $I_{BS}$ = 10 mA | 3 | | | V |
| $V_{BS2}$ | | $I_{BS}$ = 10 mA, $V_{CC}$ = 5 V, $T_A$ = 25°C | 3.5 | 3.9 | | |
| $I_{BSOFF}$ | Band-switch driver leakage current | $V_{BS}$ = 0 V | | | 3 | µA |

## Electrical Characteristics – Mixer, Oscillator, IF Amplifier

$V_{CC}$ = 5 V, $T_A$ = 25°C, measured in Figure 18 reference measurement circuit at 50-Ω system, IF filter characteristics: $f_{peak}$ = 43 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $G_{c11}$ | Conversion gain 1 (mixer-IF amplifier), VHF-LOW | $f_{in}$ = 58 MHz (1) | 22 | 25 | 28 | dB |
| $G_{c13}$ | | $f_{in}$ = 130 MHz (1) | 22 | 25 | 28 | |
| $G_{c14}$ | Conversion gain 1 (mixer-IF amplifier), VHF-HIGH | $f_{in}$ = 136 MHz (1) | 22 | 25 | 28 | dB |
| $G_{c16}$ | | $f_{in}$ = 364 MHz (1) | 22 | 25 | 28 | |
| $G_{c17}$ | Conversion gain 1 (mixer-IF amplifier), UHF | $f_{in}$ = 370 MHz (1) | 26 | 29 | 32 | dB |
| $G_{c19}$ | | $f_{in}$ = 804 MHz (1) | 25 | 28 | 31 | |
| $G_{c21}$ | Conversion gain 2 (mixer-IF amplifier), VHF-LOW | $f_{in}$ = 58 MHz (2) | 16 | 19 | 22 | dB |
| $G_{c23}$ | | $f_{in}$ = 130 MHz (2) | 16 | 19 | 22 | |
| $G_{c24}$ | Conversion gain 2 (mixer-IF amplifier), VHF-HIGH | $f_{in}$ = 136 MHz (2) | 16 | 19 | 22 | dB |
| $G_{c26}$ | | $f_{in}$ = 364 MHz (2) | 16 | 19 | 22 | |
| $G_{c27}$ | Conversion gain 2 (mixer-IF amplifier), UHF | $f_{in}$ = 370 MHz (2) | 20 | 23 | 26 | dB |
| $G_{c29}$ | | $f_{in}$ = 804 MHz (2) | 19 | 22 | 25 | |
| $NF_1$ | Noise figure, VHF-LOW | $f_{in}$ = 55.25 MHz | | 9.5 | | dB |
| $NF_3$ | | $f_{in}$ = 127.25 MHz | | 9.5 | | |
| $NF_4$ | Noise figure, VHF-HIGH | $f_{in}$ = 133.25 MHz | | 10 | | dB |
| $NF_6$ | | $f_{in}$ = 361.25 MHz | | 10 | | |
| $NF_7$ | Noise figure, UHF | $f_{in}$ = 367.25 MHz | | 11 | | dB |
| $NF_9$ | | $f_{in}$ = 801.25 MHz | | 11 | | |
| $CM_1$ | 1% cross-modulation distortion, VHF-LOW | $f_{in}$ = 55.25 MHz (3) | | 89 | | dBµV |
| $CM_3$ | | $f_{in}$ = 127.25 MHz (3) | | 89 | | |
| $CM_4$ | 1% cross-modulation distortion, VHF-HIGH | $f_{in}$ = 133.25 MHz (3) | | 86 | | dBµV |
| $CM_6$ | | $f_{in}$ = 361.25 MHz (3) | | 86 | | |
| $CM_7$ | 1% cross-modulation distortion, UHF | $f_{in}$ = 367.25MHz (3) | | 87 | | dBµV |
| $CM_9$ | | $f_{in}$ = 801.25 MHz (3) | | 87 | | |
| $V_{IFO1}$ | IF output voltage, VHF-LOW | $f_{in}$ = 55.25 MHz (4) | | 117 | | dBµV |
| $V_{IFO3}$ | | $f_{in}$ = 127.25 MHz (4) | | 117 | | |
| $V_{IFO4}$ | IF output voltage, VHF-HIGH | $f_{in}$ = 133.25 MHz (4) | | 117 | | dBµV |
| $V_{IFO6}$ | | $f_{in}$ = 361.25 MHz (4) | | 117 | | |
| $V_{IFO7}$ | IF output voltage, UHF | $f_{in}$ = 367.25MHz (4) | | 117 | | dBµV |
| $V_{IFO9}$ | | $f_{in}$ = 801.25 MHz (4) | | 117 | | |
| $\Phi_{OSC1}$ | Phase noise, VHF-LOW | $f_{in}$ = 55.25 MHz (5) | | 88 | | dBc/Hz |
| $\Phi_{OSC3}$ | | $f_{in}$ = 127.25 MHz (5) | | 88 | | |
| $\Phi_{OSC4}$ | Phase noise, VHF-HIGH | $f_{in}$ = 133.25 MHz (5) | | 86 | | dBc/Hz |
| $\Phi_{OSC6}$ | | $f_{in}$ = 361.25 MHz (5) | | 86 | | |
| $\Phi_{OSC7}$ | Phase noise, UHF | $f_{in}$ = 367.25MHz (5) | | 84 | | dBc/Hz |
| $\Phi_{OSC9}$ | | $f_{in}$ = 801.25 MHz (5) | | 84 | | |
| | Prescaler beat (6) | | | | 25 | dBµV |

(1) IF = 43 MHz, RF input level = 80 dBµV (see Figure 19)
(2) IF = 43 MHz, RF input level = 80 dBµV (see Figure 20)
(3) $f_{undes} = f_{des} \pm 6$ MHz, $P_{in}$ = 80 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(4) IF = 45.75 MHz
(5) Offset = 10 kHz, RF input level = 70 dBµV
(6) Design parameter, not tested

# FUNCTIONAL DESCRIPTION

## I²C Bus Mode

### I²C Write Mode (R/$\overline{W}$ = 0)

**Table 1. Write Data Format**

| | MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|
| Address byte (ADB) | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/$\overline{W}$ = 0 | A(1) |
| Divider byte 1 (DB1) | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A(1) |
| Divider byte 2 (DB2) | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | A(1) |
| Control byte (CB) | 1 | CP | T2 | T1 | T0 | RSA | RSB | OS | A(1) |
| Band-switch byte (BB) | X | X | X | X | BS4 | BS3 | BS2 | BS1 | A(1) |

(1) A = Acknowledge

**Table 2. Write Data Symbol Description**

| SYMBOL | DESCRIPTION | DEFAULT |
|---|---|---|
| MA[1:0] | Address-set bits (see Table 3) | |
| N[14:0] | Programmable counter set bits<br>$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$<br>Oscillation frequency = $f_r \times 8 \times N$<br>$f_r$ = Reference frequency = 4 MHz/Reference divider | N14 = N13 = N12 = ... = N0 = 0 |
| CP | Charge-pump current-set bit<br>60 µA (CP = 0), 280 µA (CP = 1) | CP = 1 |
| T[2:0] | Test bits (see Table 4)<br>Normal mode: T2 = 0, T1 = 0, T0 = 1/0 | T[2:0] = 001 |
| RSA, RSB | Reference divider ratio selection bits (see Table 5) | RSA = 0, RSB = 1 |
| OS | Tuning amplifier control bit<br>Tuning voltage on (OS = 0)<br>Tuning voltage off, high impedance (OS = 1) | OS = 0 |
| BS[4:1] | Band-switch control bits<br>BSn = 0: Tr = OFF BSn = 1: Tr = ON<br>Band selection by BS1, BS2, BS4<br>**BS1(VL) BS2(VH) BS4(U)**<br>1 0 0 VHF-LO<br>X 1 0 VHF-HI<br>X X 1 UHF | BSn = 0 |
| X | Don't care | |

### Table 3. Address Selection

| MA1 | MA0 | VOLTAGE APPLIED ON AS INPUT |
|---|---|---|
| 0 | 0 | LOW: 0 V to 0.1 $V_{CC}$ |
| 0 | 1 | MID2: open, or 0.2 $V_{CC}$ to 0.3 $V_{CC}$ |
| 1 | 0 | MID1: 0.4 $V_{CC}$ to 0.6 $V_{CC}$ |
| 1 | 1 | HIGH: 0.9 $V_{CC}$ to $V_{CC}$ |

### Table 4. Test Bits (1)

| T2 | T1 | T0 | DEVICE OPERATION | NOTE |
|---|---|---|---|---|
| 0 | 0 | 0 | Normal operation | |
| 0 | 0 | 1 | Normal operation | Default |
| 0 | 1 | X | Charge pump is off. | |
| 1 | 1 | 0 | Charge pump is sink. | |
| 1 | 1 | 1 | Charge pump is source. | |
| 1 | 0 | X | Test mode | ADC not available |

(1) Not used for other bit patterns

### Table 5. Reference Divider Ratio

| RSA | RSB | REFERENCE DIVIDER RATIO |
|---|---|---|
| X | 0 | 640 |
| 0 | 1 | 1024 |
| 1 | 1 | 512 |

## $I^2C$ Read Mode (R/W = 1)

### Table 6. Read Data Format

| | MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|
| Address byte (ADB) | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/$\overline{W}$ = 1 | A (1) |
| Status byte (SB) | POR | FL | 1 | 1 | 1 | A2 | A1 | A0 | – |

(1) A = Acknowledge

### Table 7. Read Data Symbol Description

| SYMBOL | DESCRIPTION | DEFAULT |
|---|---|---|
| MA[1:0] | Address-set bits (see Table 3) | |
| POR | Power-on-reset flag<br>POR set: Power on<br>POR reset: End-of-data transmission procedure | POR = 1 |
| FL | In-lock flag<br>PLL locked (FL = 1), PLL unlocked (FL = 0) | |
| A[2:0] | Digital data of ADC (see Table 8) | |

**Table 8. ADC Level**

| A2 | A1 | A0 | VOLTAGE APPLIED ON ADC INPUT(1) |
|---|---|---|---|
| 1 | 0 | 0 | 0.6 $V_{CC}$ to $V_{CC}$ |
| 0 | 1 | 1 | 0.45 $V_{CC}$ to 0.6 $V_{CC}$ |
| 0 | 1 | 0 | 0.3 $V_{CC}$ to 0.45 $V_{CC}$ |
| 0 | 0 | 1 | 0.15 $V_{CC}$ to 0.3 $V_{CC}$ |
| 0 | 0 | 0 | 0 V to 0.15 $V_{CC}$ |

(1) Accuracy is $0.03 \times V_{CC}$.

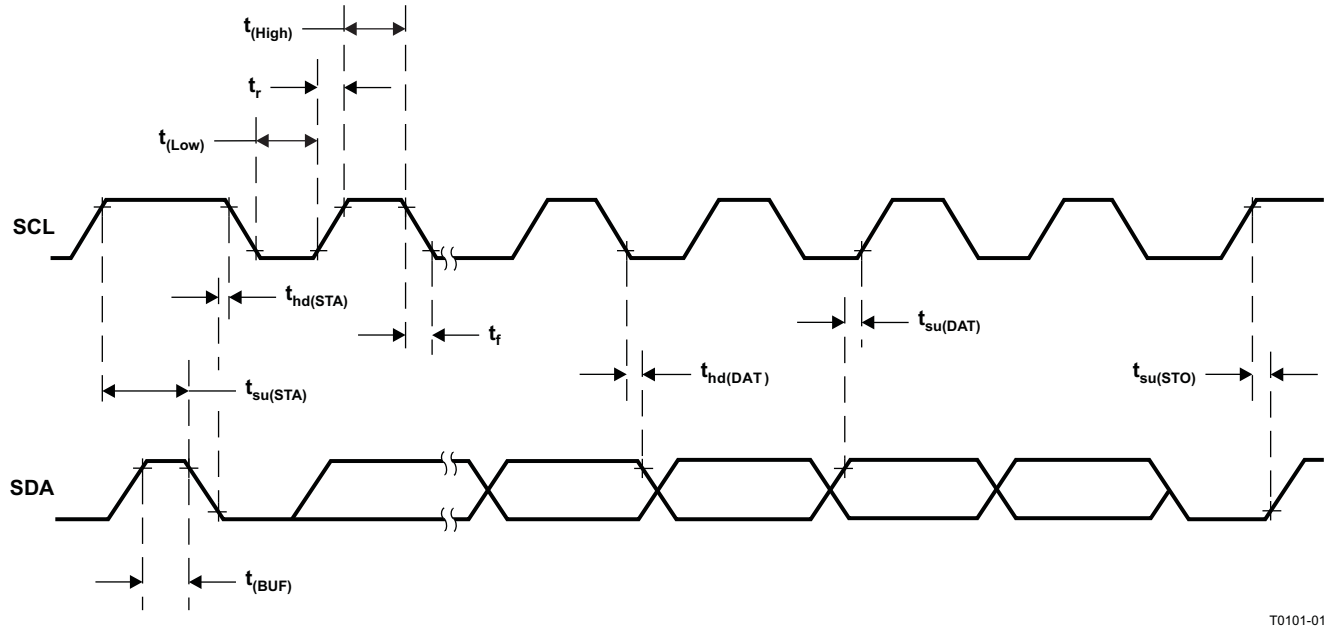
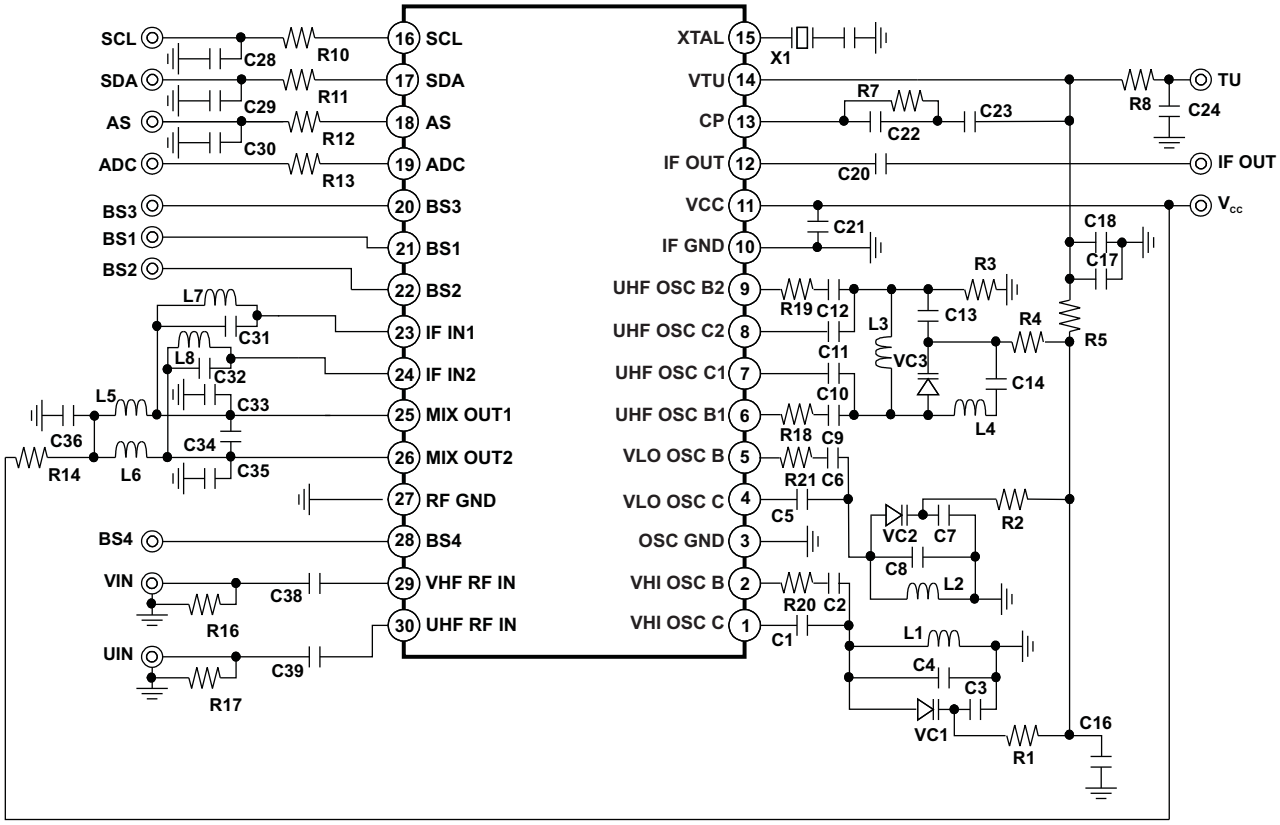



**Figure 17. I²C Timing Chart**

## APPLICATION INFORMATION




NOTE: This application information is advisory and a performance check is required for actual application circuits. TI assumes no responsibility for the consequences of the use of this circuit, nor for any infringement of patent or patent rights of third parties that may result from its use.

**Figure 18. Reference Measurement Circuit**

## APPLICATION INFORMATION (continued)

### Component Values for Measurement Circuit

| PART NAME | VALUE | | PART NAME | VALUE |
|---|---|---|---|---|
| C1 | 2 p | | L1 | ϕ2.4 mm 4T 0.4 mm |
| C2 | 2 p | | L2 | ϕ3.0 mm 8T 0.32 mm |
| C3 | 82 p | | L3 | ϕ3.0 mm 2T 0.4 mm |
| C4 | Open | | L4 | ϕ2.0 mm 3T 0.4 mm |
| C5 | 2 p | | L5 | ϕ2.4 mm 16T 0.26 mm |
| C6 | 2 p | | L6 | ϕ2.4 mm 16T 0.26 mm |
| C7 | 47 p | | L7 | Open |
| C8 | 3 p | | L8 | Open |
| C9 | 1.5 p | | | |
| C10 | 1 p | | R1 | 33 k |
| C11 | 1 p | | R2 | 33 k |
| C12 | 1.5 p | | R3 | 22 k |
| C13 | 12 p | | R4 | 33 k |
| C14 | 100 p | | R5 | 22 k |
| C16 | 2.2 nF/50 V | | R7 | 22 k |
| C17 | 2.2 n/50 V | | R8 | 22 k |
| C18 | 2.2 n/50 V | | R10 | 330 |
| C20 | 2.2 n | | R11 | 330 |
| C21 | 4.7 n | | R12 | 330 |
| C22 | 2.2 n | | R13 | Short |
| C23 | 0.1 µ/50 V | | R14 | Short |
| C24 | 2.2 n/50 V | | R16 | Open |
| C27 | 68 p | | R17 | Open |
| C28 | Open | | R18 | 20 |
| C29 | Open | | R19 | 20 |
| C30 | Open | | R20 | 20 |
| C31 | Short | | | |
| C32 | Short | | | |
| C33 | Open | | U1 | SN761678B |
| C34 | 22 pF | | | |
| C35 | Open | | VC1 | 1T363A |
| C36 | 4.7 n | | VC2 | 1T363A |
| C38 | 2.2 n | | VC3 | 1T363A |
| C39 | 2.2 n | | | |
| | | | X1 | 4 MHz |

## APPLICATION INFORMATION (CONTINUED)

### Test Circuits

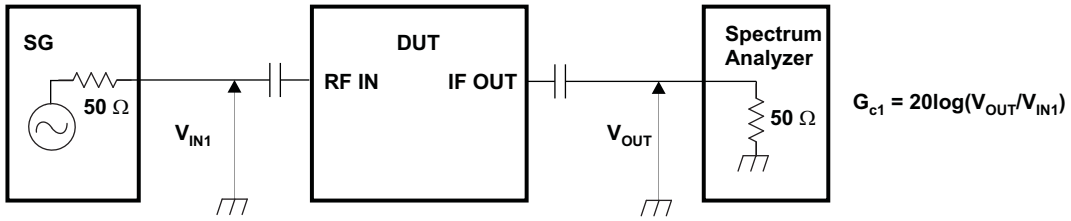



**Figure 19. Measurement Circuit of Conversion Gain 1**

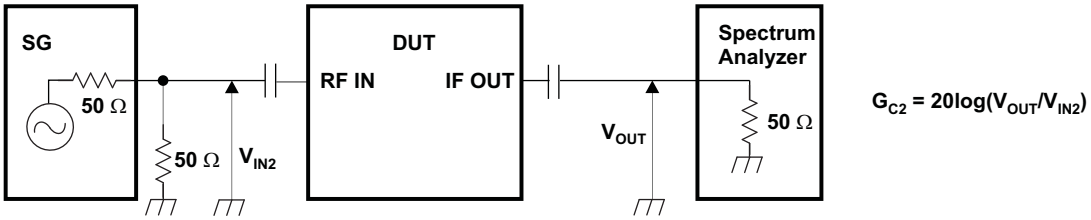



**Figure 20. Measurement Circuit of Conversion Gain 2**

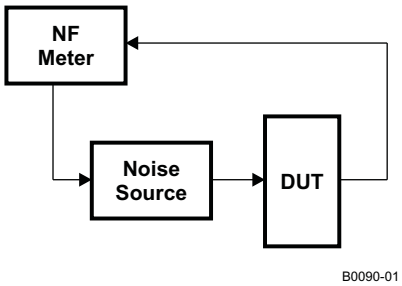



**Figure 21. Noise-Figure Measurement Circuit**

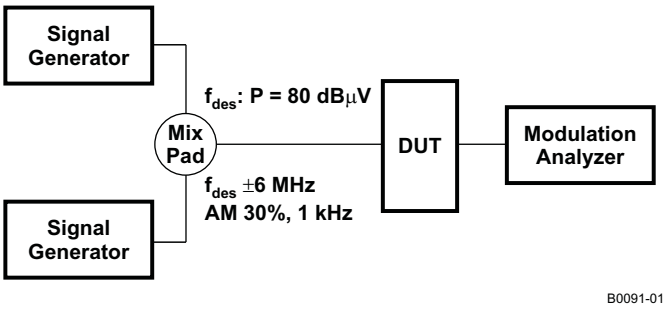



**Figure 22. 1% Cross-Modulation-Distortion Measurement Circuit**

## TYPICAL CHARACTERISTICS

### Band-Switch Driver Output Voltage (BS1–BS4)

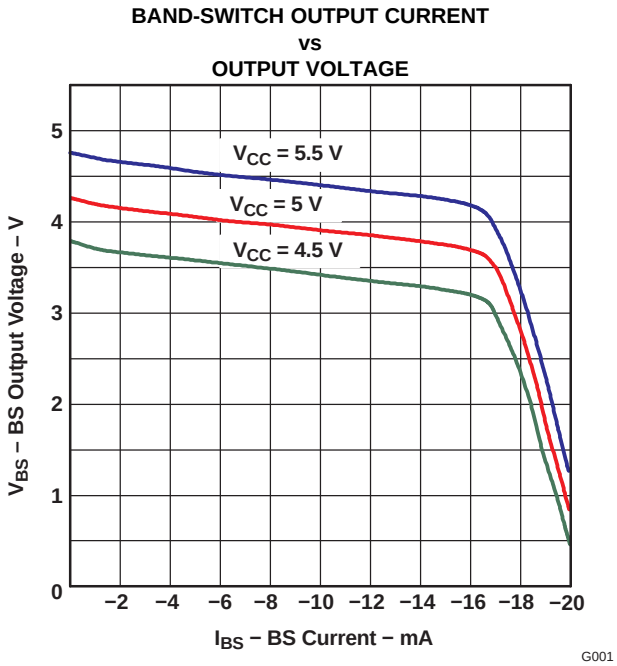



Figure 23. Band-Switch Driver Output Voltage

### S-Parameter

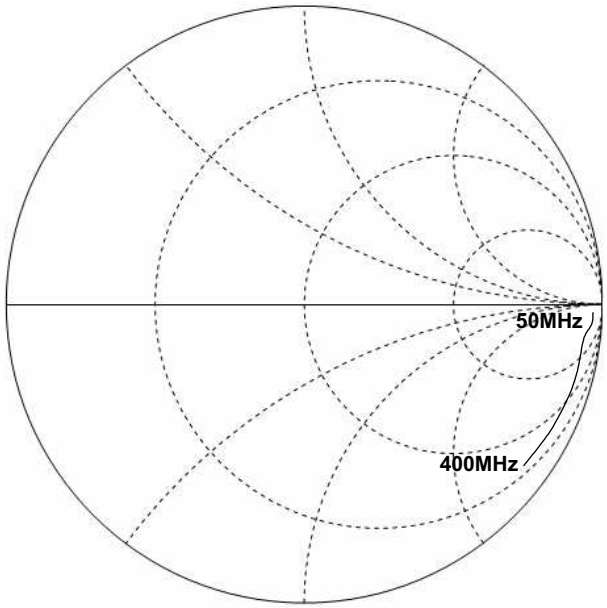



Figure 24. VHF Input

## TYPICAL CHARACTERISTICS (continued)

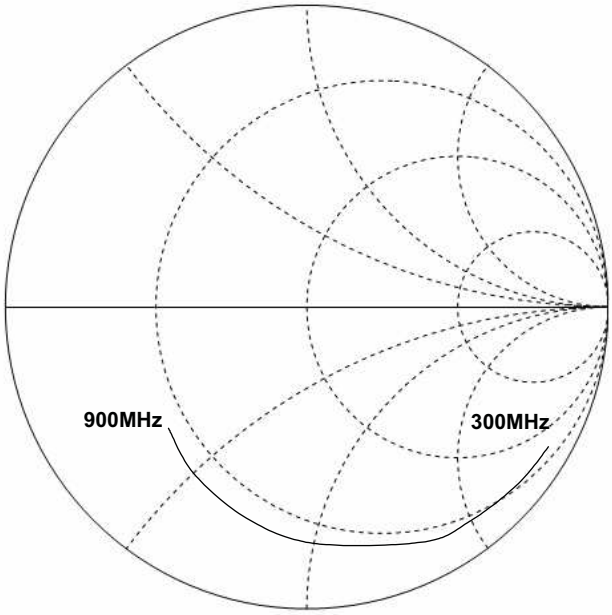



**Figure 25. UHF Input**

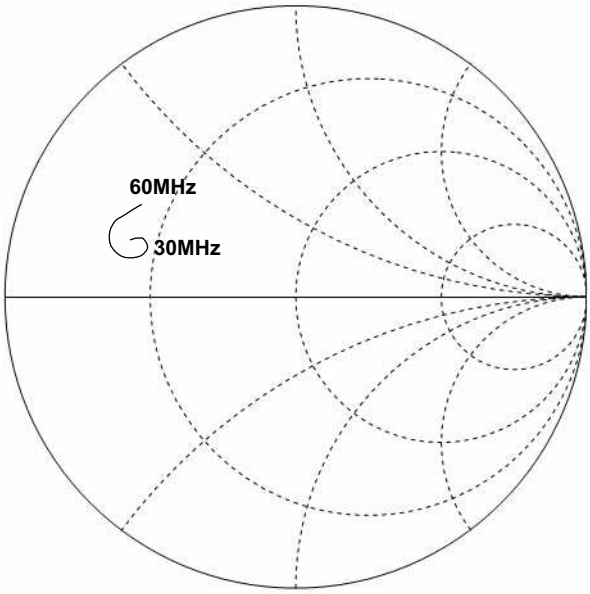



**Figure 26. IF Output**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN761678BDBTR | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN761678BDBTRG4 | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN761678BDCHR | ACTIVE | TSSOP | DCH | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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