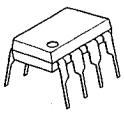
TONE DECODER/PHASE LOCKED LOOP

■ GENERAL DESCRIPTION

The NJM567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth cebter frequency, and output delay are independently determined by means of four external components.

■ PACKAGE OUTLINE



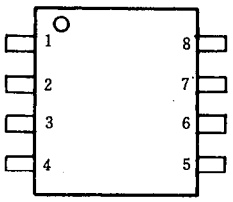
NJM567D

NJM567M

■ FEATURES

- Operating Voltage (4.75V~9.0V)
- Wide frequency range (0.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14 percent)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Frequency adjustment over a 20 to 1 range with an external resistor
- Package Outline DIP8, DMP8
- Bipolar Technology

■ PIN CONFIGURATION

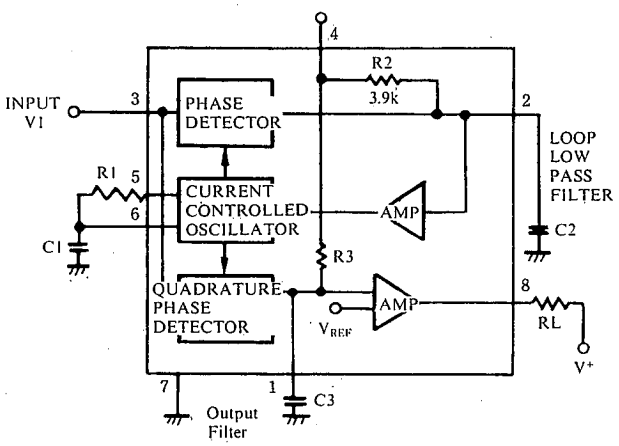


NJM567D
NJM567M

PIN FUNCTION

1	OUTPUT FILTER
2	LOW-PASS FILTER
3	INPUT
4	V+
5	TIMING R
6	TIMING CR
7	GROUND
8	OUTPUT

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Input Positive Voltage	V_{IP}	$V^+ + 0.5$	V
Input Negative Voltage	V_{IN}	−10	Vdc
Output Voltage	V_8	15 (Pin8)	Vdc
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−40～+85	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

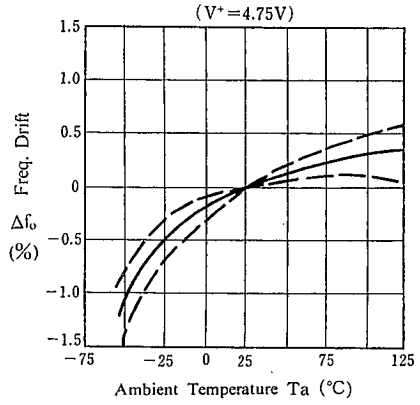
■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=5.0V)

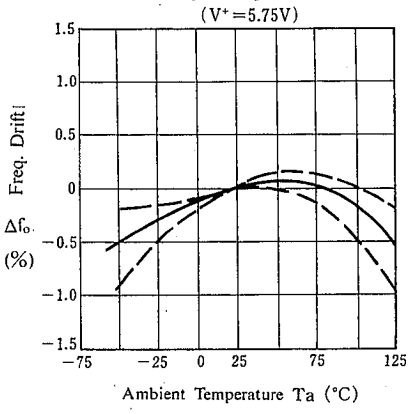
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Highest Center Frequency	f_{OH}		100	500	—	kHz
Center Frequency Stability	$\Delta fo/\Delta T$	−20～+75°C	—	35±60	—	PPM/°C
Center Frequency Shift with Supply Voltage	$\Delta fo/\Delta V$	fo=100kHz	—	0.7	2	%/V
Largest Detection Bandwidth	B_{WM}	fo=100kHz	10	14	18	%×fo
Largest Detection Bandwidth Skew	B_{WS}		—	2	3	%×fo
Largest Detection Bandwidth Variation with Temperature	$\Delta B_W/\Delta T$	Vi=300mVrms	—	±0.1	—	%/°C
Largest Detection Bandwidth Variation with Supply Voltage	$\Delta B_W/\Delta V$	Vi=300mVrms	—	±2	—	%/V
Input Resistance	R_{IN}		—	20	—	kΩ
Smallest Detectable Input Voltage		I_L=100mA, fi=fo	—	20	25	mVrms
Largest No-Output Input Voltage		I_L=100mA, fi=fo	10	15	—	mVrms
Greatest Simultaneous Outband Signal to Inband Signal Ratio			—	+6	—	dB
Minimum Input Signal to Wideband Noise Ratio		B_n=140kHz	—	−6	—	dB
Fastest ON-OFF Cycling Rate			—	fo/20	—	
"1" Output Leakage Current			—	0.01	25	μA
"0" Output Voltage		I_L=30mA	—	0.2	0.4	V
		I_L=100mA	—	0.6	1.0	V
Output Fall Time		R_L=50Ω	—	30	—	ns
Output Rise Time		R_L=50Ω	—	150	—	ns
Operating Voltage	V^+_{opr}		4.75	—	9.0	V
Operating Current Quiescent	$I_{CC}I$		—	7	10	mA
Operating Current – Activated	$I_{CC}II$	R_L=20kΩ	—	12	15	mA
Quiescent Power Dissipation	P_D		—	35	—	mW

■ TYPICAL CHARACTERISTICS

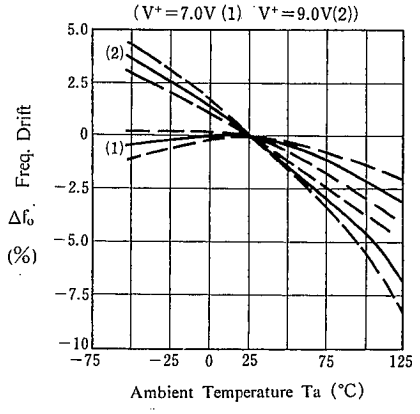
Frequency Drift
(V^+=4.75V)



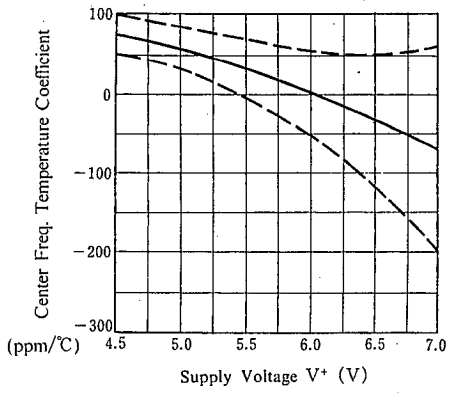
Frequency Drift
(V^+=5.75V)



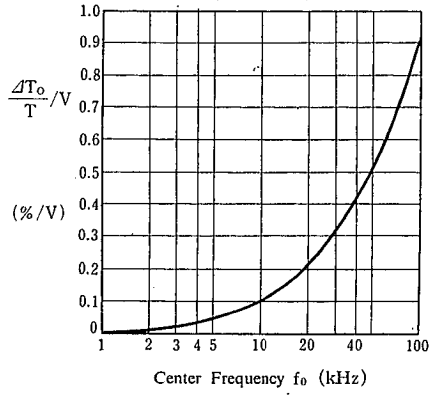
Frequency Drift
(V^+=7.0V (1) V^+=9.0V(2))



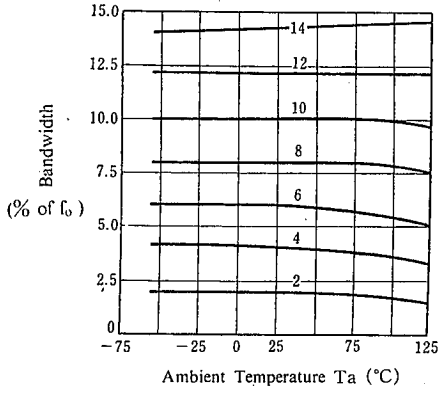
Center Frequency Temperature Coefficient (ΔT=0°C~70°C)



Center Frequency Shift
(Ta=25°C)

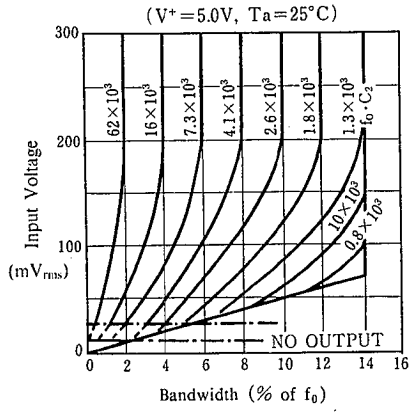


Detection Bandwidth
(V^+=5.0V)

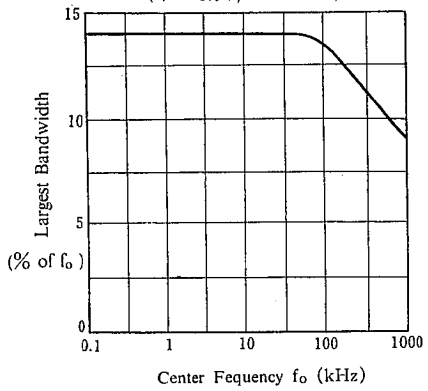


■ TYPICAL CHARACTERISTICS

Bandwidth
(V⁺=5.0V, Ta=25°C)



Largest Detection Bandwidth
(V⁺=5.0V, Ta=25°C)



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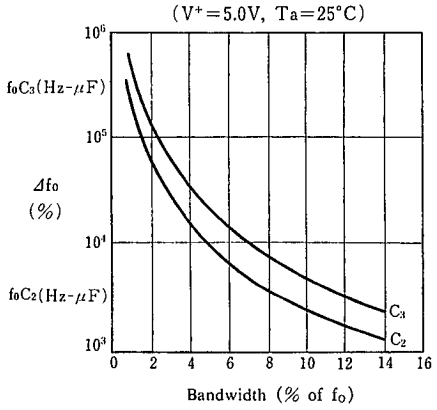
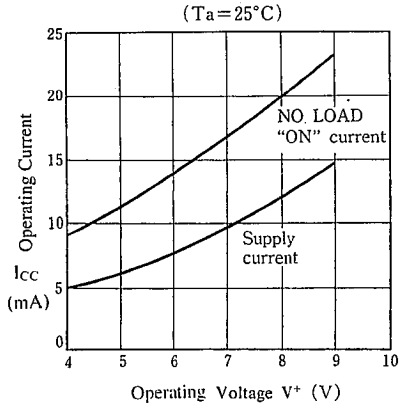
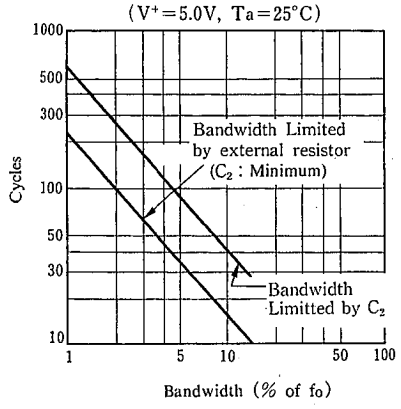
Detection Bandwidth vs. C2, C3
(V⁺=5.0V, Ta=25°C)



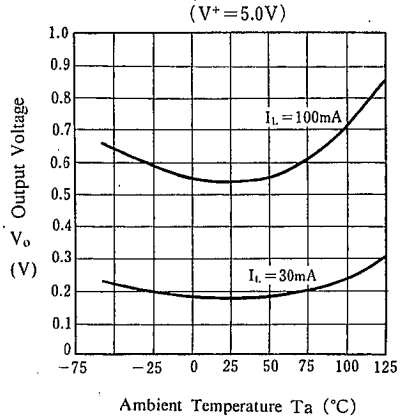
Operating Current
(Ta=25°C)



Greatest Number of Cycles
(V⁺=5.0V, Ta=25°C)



Output Voltage
(V⁺=5.0V)



■ DESIGN FORMULAS

$$f_o = \frac{1}{1.07\,R_1C_1} \quad (V_{IN} = 0mV)$$

$$BW \simeq 1070\sqrt{\frac{V_{IN}}{f_oC_2}} \text{ in \% of } f_O,\ V_{IN} \leqq 200mVrms$$

where V_{IN} : Input Voltage (Vrms)
C_2 : LPF Capacitor (μF)

■ PLL WORDS EXPLANATIONS

☆ **Center Frequency (f_o)**
The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

☆ **Detection Bandwidth (BW)**
The frequency range, centered about f_o, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

☆ **Lock Range**
The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

☆ **Detection Band Skew**
A measure of how well the detection band is centered about the center frequency, f_o. The skew is defined as $(f_{max} + f_{min} - 2f_o)/2f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

◎ **Operating Instructions**
Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

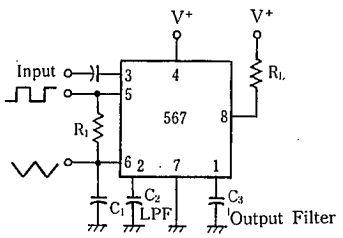


Figure 1

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_oC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_oC_2 product (f_o (Hz), C_2 (μfd)).
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

◎ **Output Terminal** (Fig. 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_o with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

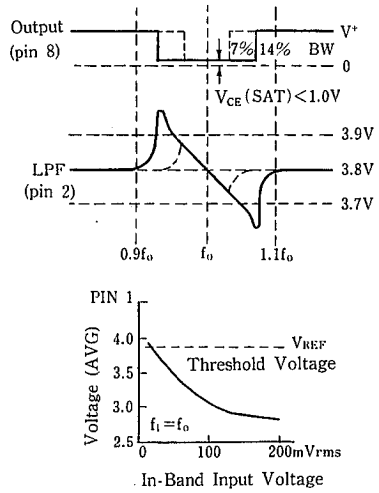


Figure 2

■ OPERATING PRECAUTINS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.
2. The 567 will lock onto signals near $(2n + 1)\ f_o$, and will give an output for signals near $(4n + 1)\ f_o$ where n=0, 1, 2, etc. Thus, signals at $5f_o$ and $9f_o$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and outband signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into an out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

◎ **Speed of Operation**

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

◎ **Optional Controls** (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

◎ **Sensitivity Adjustment** (Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for Lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most usefu when, to obtain maximum operating speed. C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

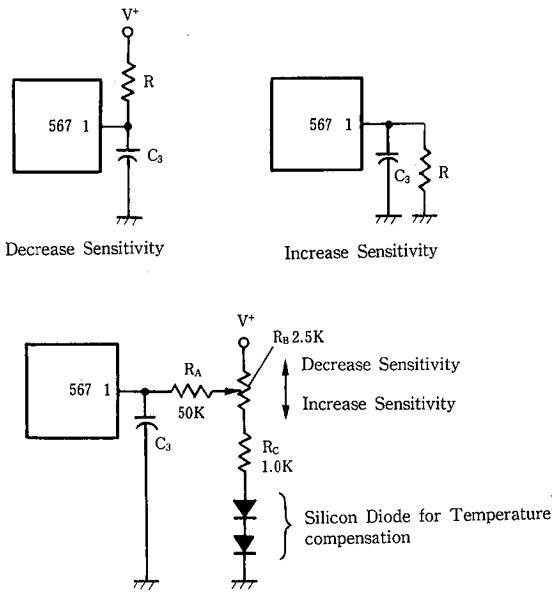


Figure 3

◎ **Chatter Prevention** (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

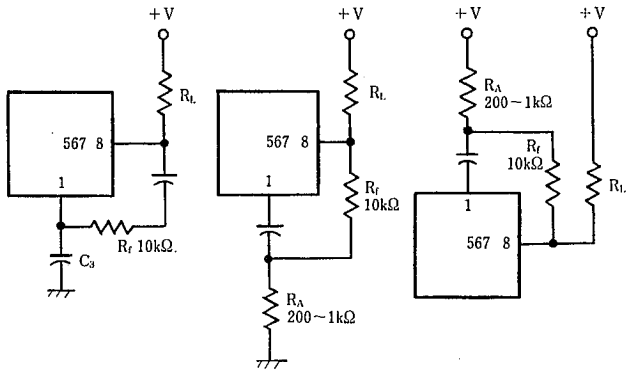


Figure 4

◎ **Detection Band Centering (or Skew) Adjustment** (Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

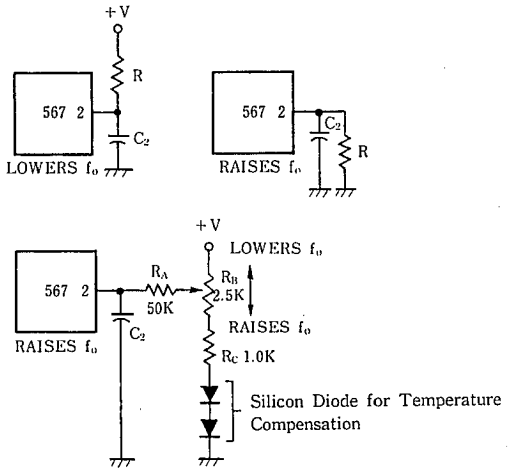


Figure 5

◎ **Alternate Method of Bandwidth Reduction** (Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve camping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

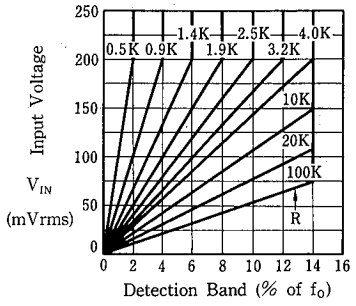
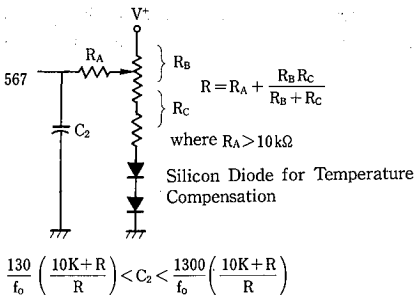


Figure 6

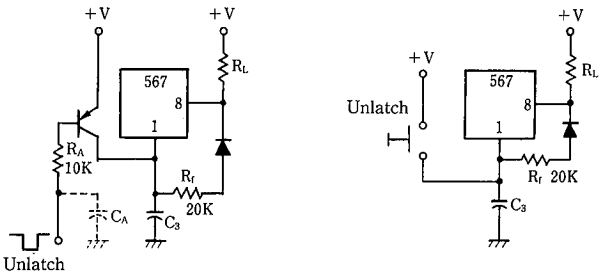


(note) Adjust control for symmetry of detection band edges about f_0.

◎ **Output Latching** (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

Output Latching



C_A prevents latch-up when power supply is turned on.

Figure 7

◎ **Reduction of C_1 Value** (Figure 8)

For precision very low-frequency applictions, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and lower value of C_1 for a given frequency.

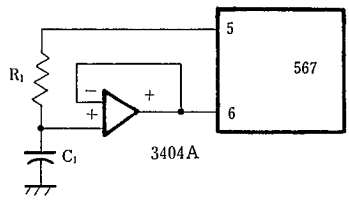


Figure 8

◎ **Programming**

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

MEMO

[CAUTION]
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