

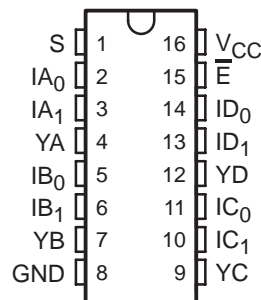
TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

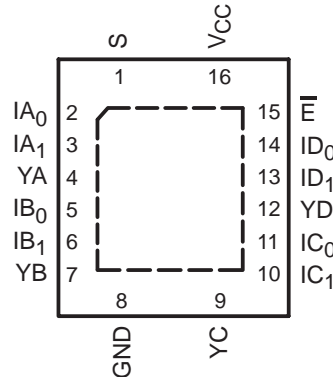
SCDS161A – MAY 2004 – REVISED OCTOBER 2004

- Wide Bandwidth (BW = 350 MHz Min)
- Low Differential Crosstalk ($X_{TALK} = -68$ dB Typ)
- Low Power Consumption ($I_{CC} = 10$ μ A Max)
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ($r_{on} = 5$ Ω Typ)
- Rail-to-Rail Switching on Data I/O Ports (0 to V_{CC})
- V_{CC} Operating Range From 3 V to 3.6 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Data and Control Inputs Have Undershoot Clamp Diodes
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Suitable for Both 10 Base-T/100 Base-T Signaling

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The TI TS3L100 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable (\bar{E}) input. When \bar{E} is low, the switch is enabled and the I port is connected to the Y port. When \bar{E} is high, the switch is disabled and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN – RGY	Tape and reel	TS3L100RGYR	TK100
	SOIC – D	Tube	TS3L100D	TS3L100
		Tape and reel	TS3L100DR	
	SSOP (QSOP) – DBQ	Tape and reel	TS3L100DBQR	TK100
	TSSOP – PW	Tube	TS3L100PW	TK100
		Tape and reel	TS3L100PWR	
	TVSOP – DGV	Tape and reel	TS3L100DGV	TK100

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

description/ordering information (continued)

This device can be used to replace mechanical relays in LAN applications. This device has low r_{on} , wide bandwidth, and low differential crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \bar{E} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS		INPUT/OUTPUT YX	FUNCTION
\bar{E}	S		
L	L	IX_0	$YX = IX_0$
L	H	IX_1	$YX = IX_1$
H	X	Z	Disconnect

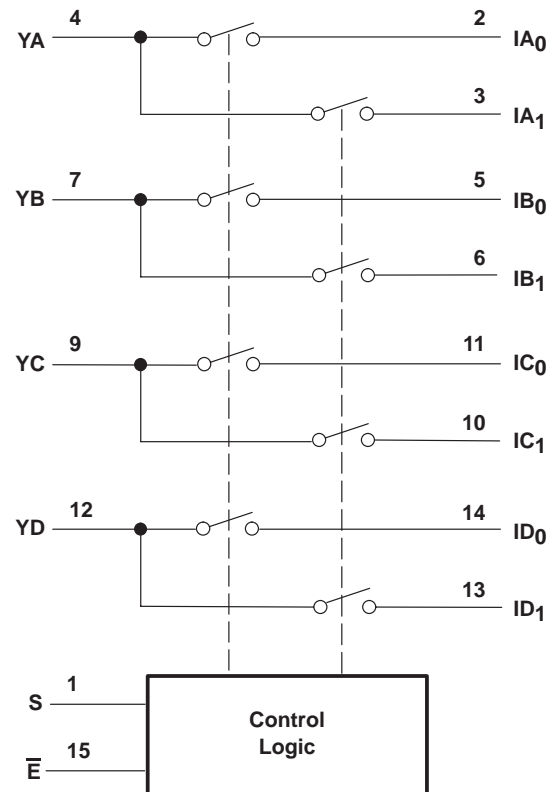
PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
$I_{An}-I_{Dn}$	Data I/Os
S	Select input
\bar{E}	Enable input
Y_A-Y_D	Data I/Os

TS3L100
QUAD SPDT WIDE-BANDWIDTH LAN SWITCH
WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

logic diagram (positive logic)



TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	–0.5 V to 4.6 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 4.6 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	–50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	73°C/W
DB package	82°C/W
DBQ package	90°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (\bar{E} , S)	2	V_{CC}	V
V_{IL}	Low-level control input voltage (\bar{E} , S)	0	0.8	V
T_A	Operating free-air temperature	0	70	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TS3L100
QUAD SPDT WIDE-BANDWIDTH LAN SWITCH
WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

**electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	\bar{E}, S	$V_{CC} = 3\text{ V}, I_{IN} = -18\text{ mA}$			-1.8	V
V_{hys}	\bar{E}, S			150		mV
I_{IH}	\bar{E}, S	$V_{CC} = 3.6\text{ V}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	\bar{E}, S	$V_{CC} = 3.6\text{ V}, V_{IN} = \text{GND}$			± 1	μA
I_{OZ}^\ddagger		$V_{CC} = 3.6\text{ V}, V_O = 0\text{ to }3.6\text{ V}, V_I = 0,$ Switch OFF			± 1	μA
I_{OS}^\S		$V_{CC} = 3.6\text{ V}, V_O = 0\text{ to }0.5 V_{CC}, V_I = 0,$ Switch ON	50			mA
I_{off}		$V_{CC} = 0, V_O = 0\text{ to }3.6\text{ V}, V_I = 0$			15	μA
I_{CC}		$V_{CC} = 3.6\text{ V}, I_{I/O} = 0,$ Switch ON or OFF		0.1	10	μA
ΔI_{CC}	\bar{E}, S	$V_{CC} = 3.6\text{ V},$ One input at $V_{CC} - 0.6\text{ V},$ Other inputs at V_{CC} or GND			750	μA
I_{CCD}		$V_{CC} = 3.6\text{ V},$ I and Y ports open, V_{IN} input switching 50% duty cycle			0.45	mA/ MHz
C_{IN}	\bar{E}, S	$f = 1\text{ MHz}$		3		pF
C_{OFF}	I port	$V_I = 0, f = 1\text{ MHz},$ Outputs open, Switch OFF		5		pF
	Y port			10		
C_{ON}		$V_I = 0, f = 1\text{ MHz},$ Outputs open, Switch ON		17		pF
r_{on}		$V_{CC} = 3\text{ V}, V_I = 0\text{ V}, I_O = 48\text{ mA}$	5	7		Ω
		$V_I = 2\text{ V}, I_O = 15\text{ mA}$	10	15		
Δr_{on}		$V_I = 3\text{ V},$ Switch ON, $I_O = 15\text{ mA}$		1		Ω

$V_I, V_O, I_I,$ and I_O refer to I/O pins. V_{IN} refers to the control inputs.

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ The I_{OS} test is applicable to only one ON channel at a time. The duration of this test is less than one second.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}, R_L = 100\ \Omega, C_L = 35\text{ pF}$ (unless otherwise noted) (see Figure 4)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{ON}	S	Y	1	7.5	ns
t_{OFF}	S	Y	1	3.5	ns

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

**dynamic characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TYP†	UNIT
$X_{TALK}(\text{Diff})$	$R_L = 100\ \Omega, f = 10\text{ MHz},$ see Figure 8, $t_r = t_f = 2\text{ ns}$	-55	dB
X_{TALK}	$R_L = 100\ \Omega, f = 30\text{ MHz},$ see Figure 6	-68	dB
O_{IRR}	$R_L = 100\ \Omega, f = 30\text{ MHz},$ see Figure 7	-42	dB
BW	$R_L = 100\ \Omega,$ see Figure 5	350	MHz

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.



TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

OPERATING CHARACTERISTICS

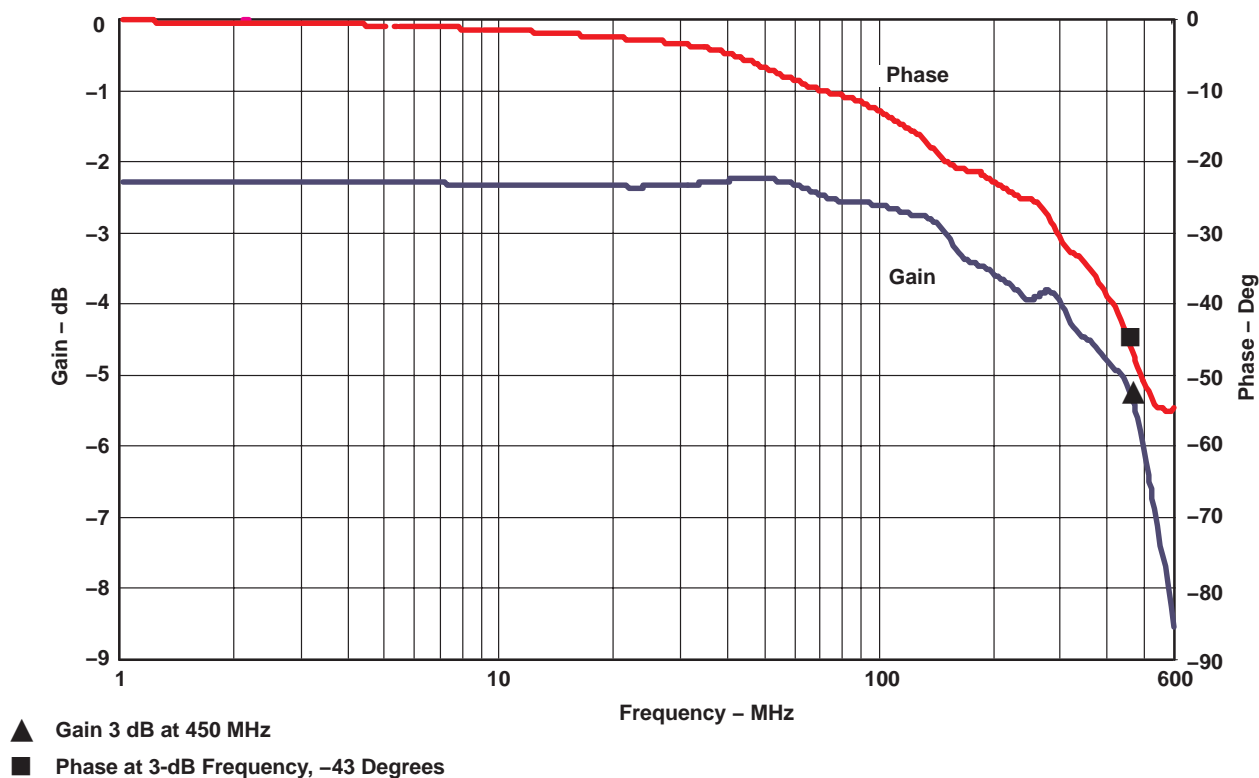


Figure 1. Gain/Phase vs Frequency

OPERATING CHARACTERISTICS

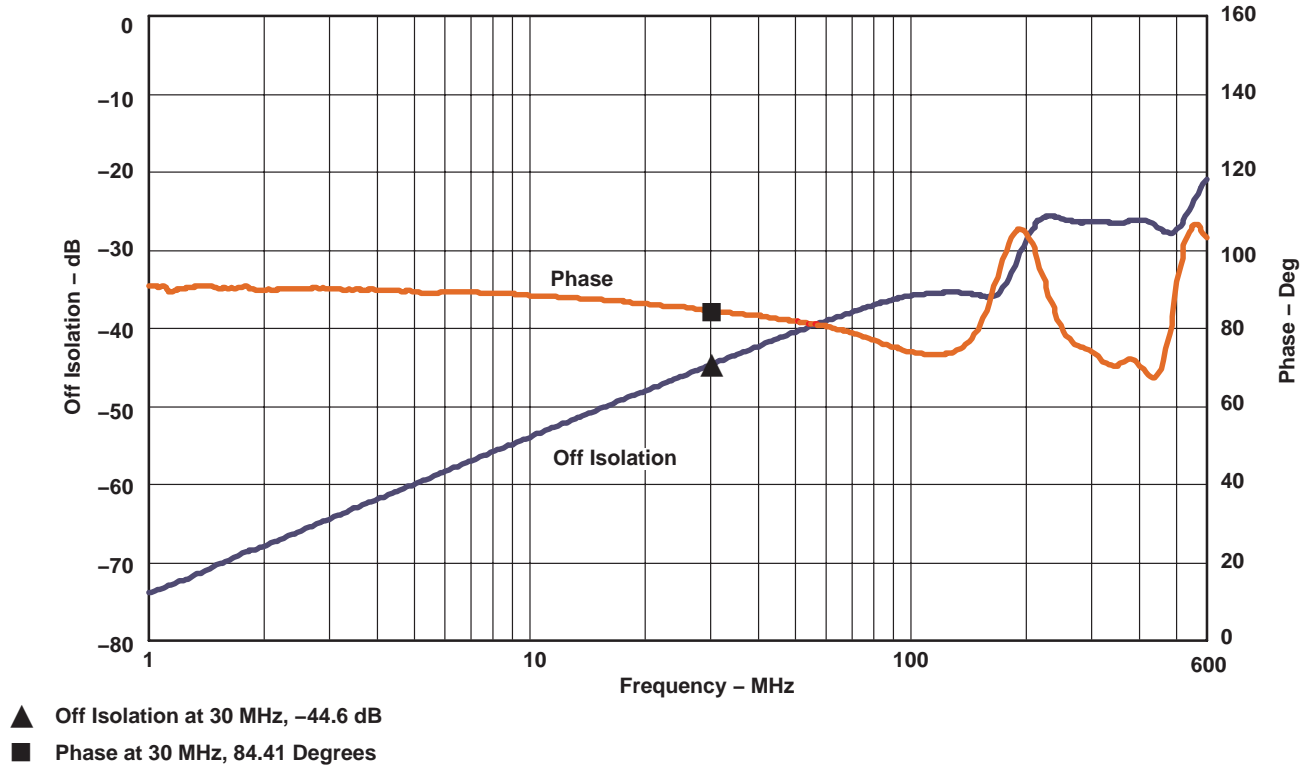


Figure 2. Off Isolation vs Frequency

TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

OPERATING CHARACTERISTICS

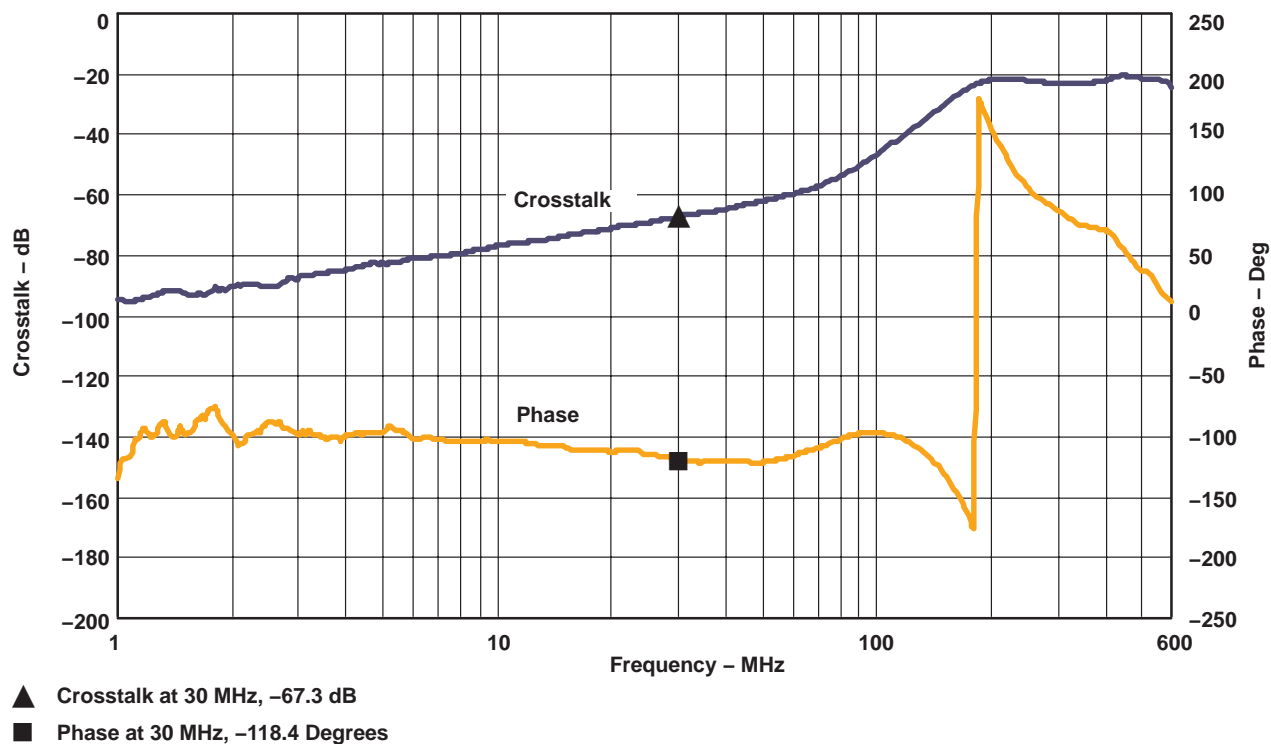


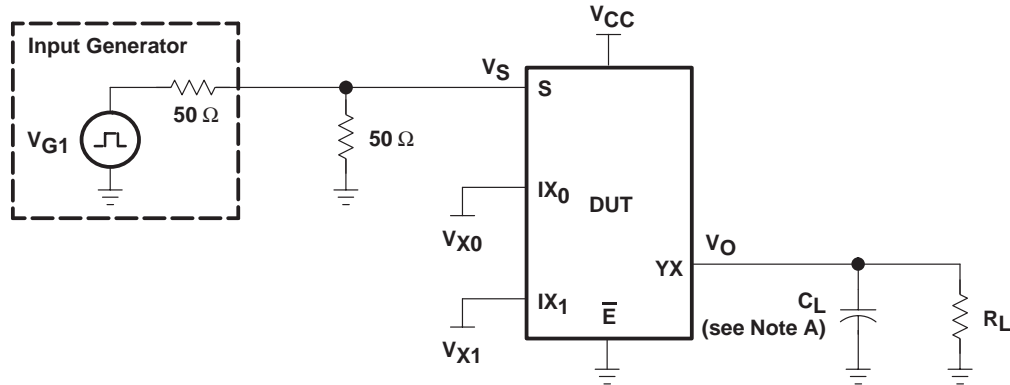
Figure 3. Crosstalk vs Frequency

TS3L100

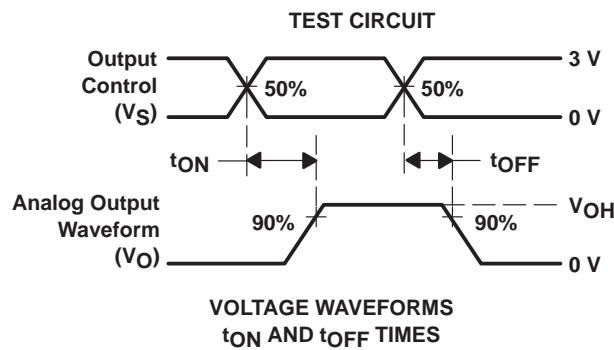
QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	R _L	C _L	V _{X0}	V _{X1}
t _{ON}	3.3 V ± 0.3 V	100 Ω	35 pF	GND	3 V
	3.3 V ± 0.3 V	100 Ω	35 pF	3 V	GND
t _{OFF}	3.3 V ± 0.3 V	100 Ω	35 pF	GND	3 V
	3.3 V ± 0.3 V	100 Ω	35 pF	3 V	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 C. The outputs are measured one at a time, with one transition per measurement.

Figure 4. Test Circuit and Voltage Waveforms

TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

PARAMETER MEASUREMENT INFORMATION

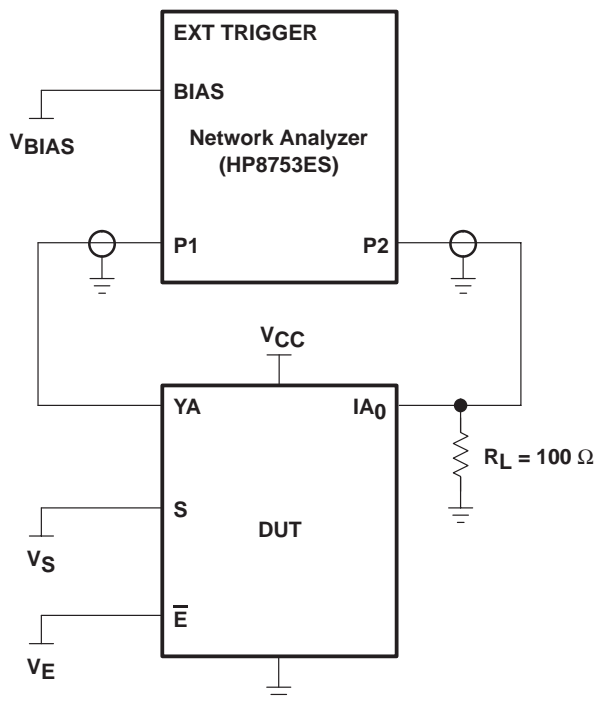


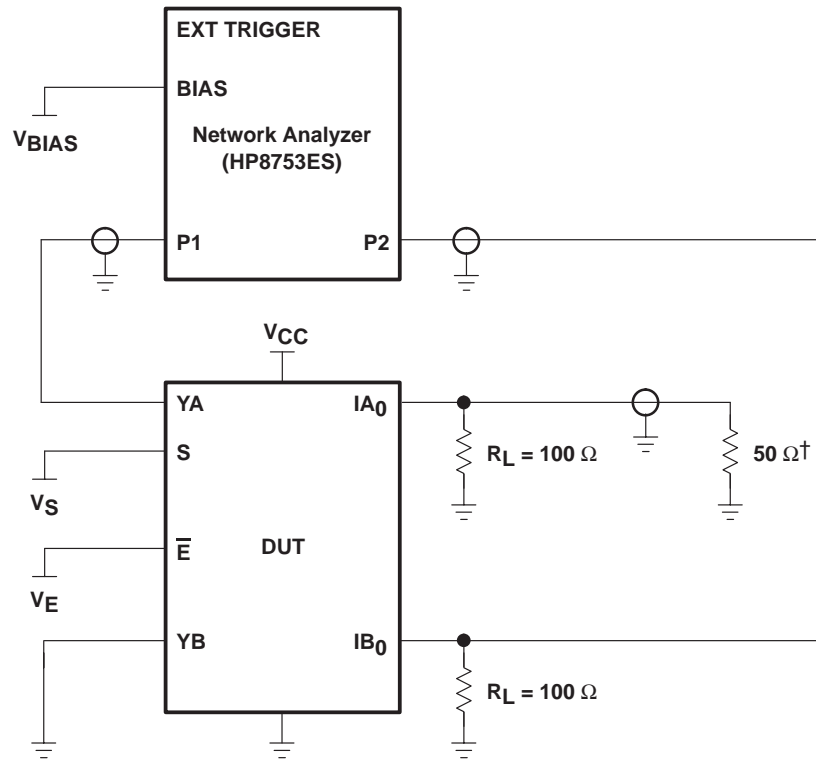
Figure 5. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_S = 0$, $V_E = 0$, and YA is the input, the output is measured at IA₀. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION



† A 50- Ω termination resistor is needed for the network analyzer.

Figure 6. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_S = 0$, $V_E = 0$, and YA is the input, the output is measured at IB_0 . All unused analog input (Y) ports are connected to GND and output (I) ports are connected to GND through 50- Ω pulldown resistors.

HP8753ES setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
 ST = 2 s
 P1 = 0 dBm

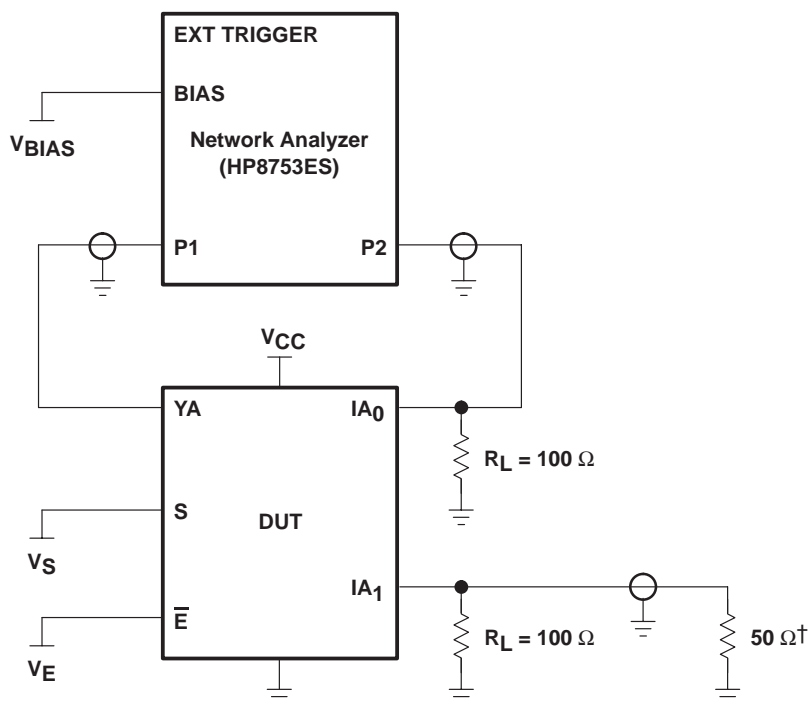
TS3L100

QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

WITH LOW ON-STATE RESISTANCE

SCDS161A – MAY 2004 – REVISED OCTOBER 2004

PARAMETER MEASUREMENT INFORMATION



† A 50- Ω termination resistor is needed for the network analyzer.

Figure 7. Test Circuit for Off Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at IA_0 . All unused analog input (Y) ports are left open and output (I) ports are connected to GND through 50- Ω pulldown resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION

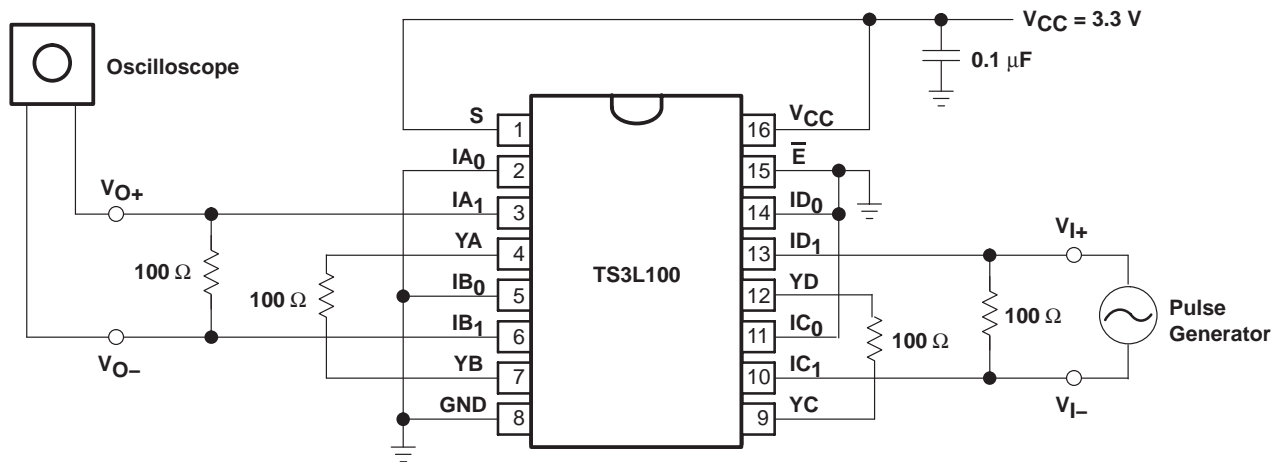


Figure 8. Differential Crosstalk Measurement

Differential crosstalk is a measure of coupling noise between a transmit and receive pair in the LAN application. Differential crosstalk depends on the edge rate, frequency, and load. This is calculated from the equation, $X_{TALK}(Diff) \text{ db} = 20 \log V_O(Diff)/V_I(Diff)$, where $V_O(Diff)$ is the differential output voltage and $V_I(Diff)$ is the differential input voltage.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TS3L100DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L100DBQRE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L100DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L100DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L100RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L100RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

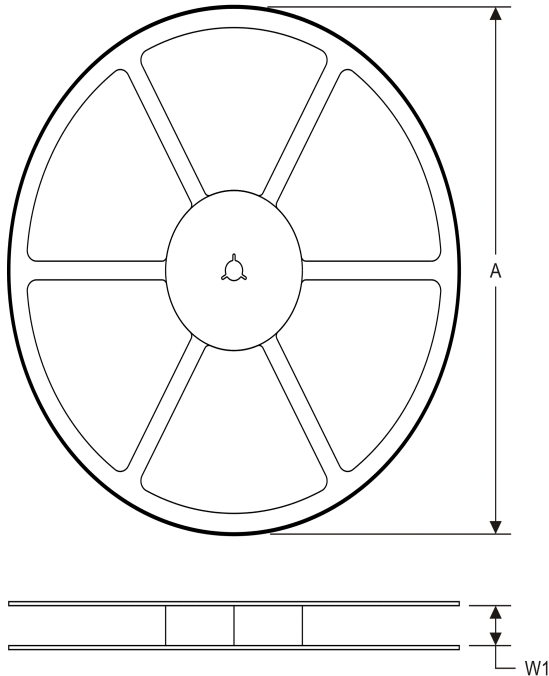
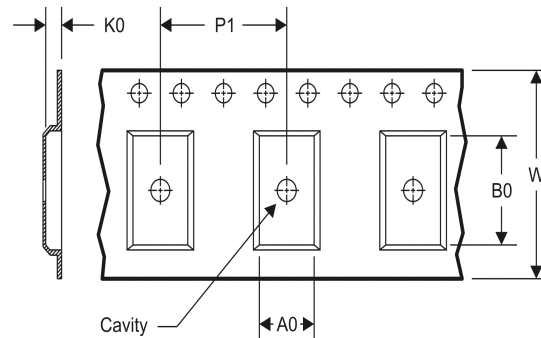
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L100DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3L100DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3L100PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3L100RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L100DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
TS3L100DR	SOIC	D	16	2500	333.2	345.9	28.6
TS3L100PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TS3L100RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

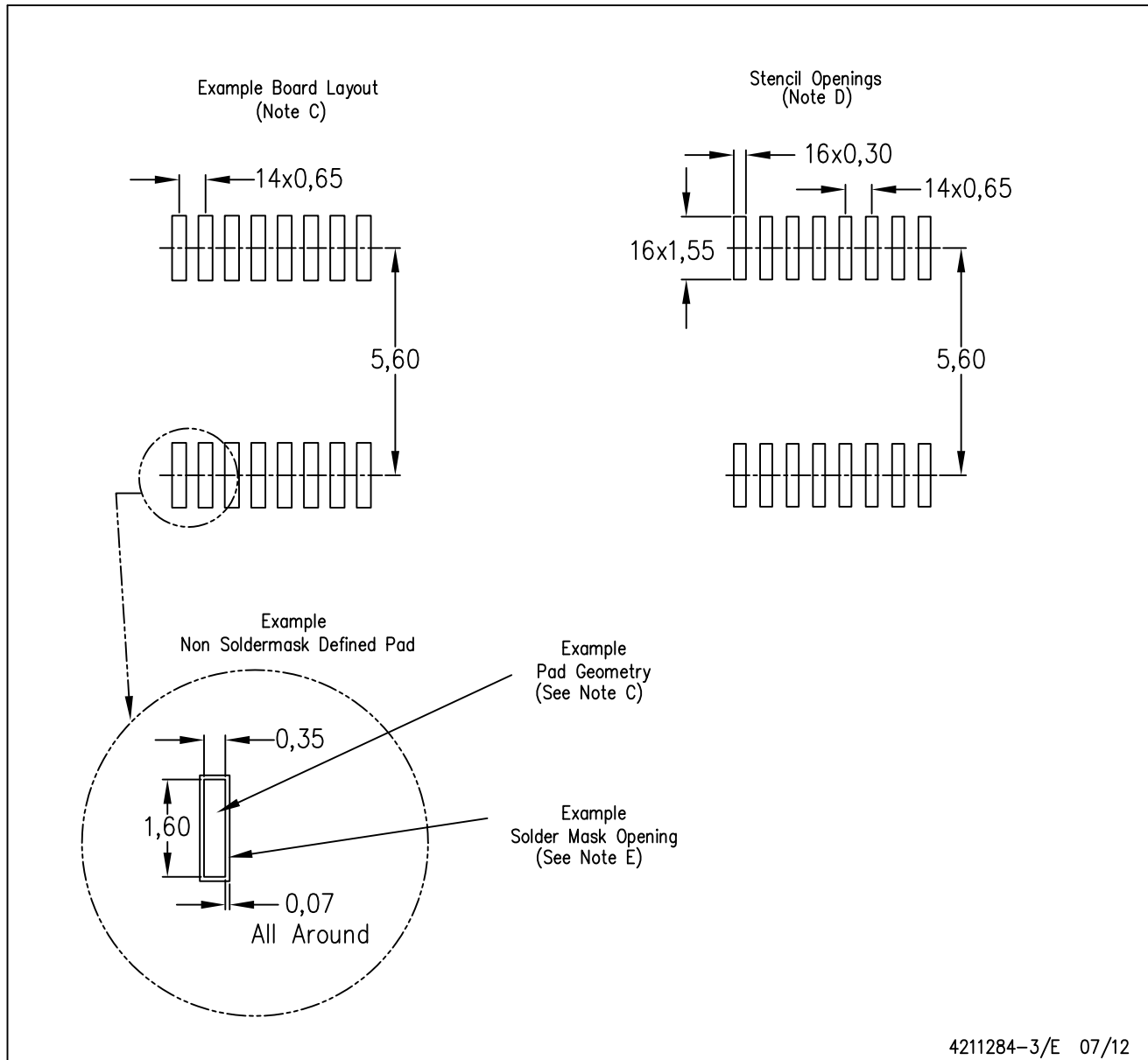
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

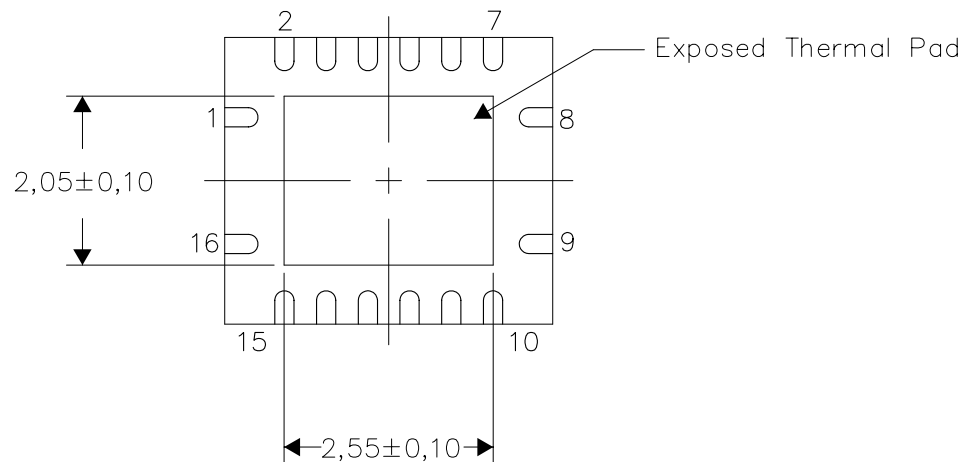
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

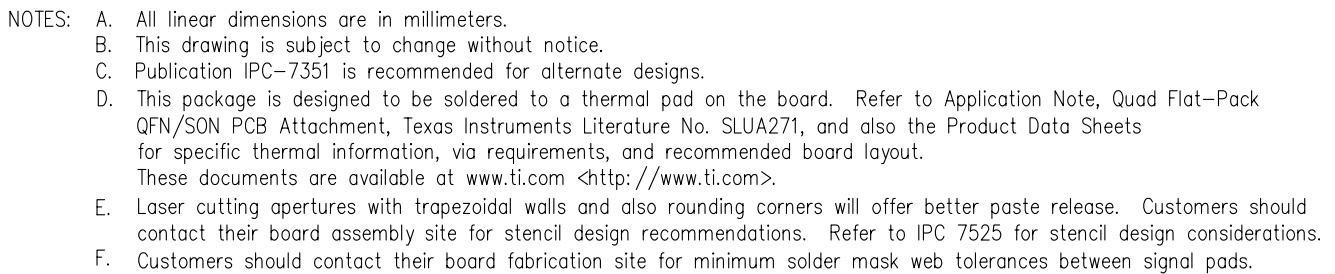


Bottom View

Exposed Thermal Pad Dimensions

4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters



DBQ (R-PDSO-G16)

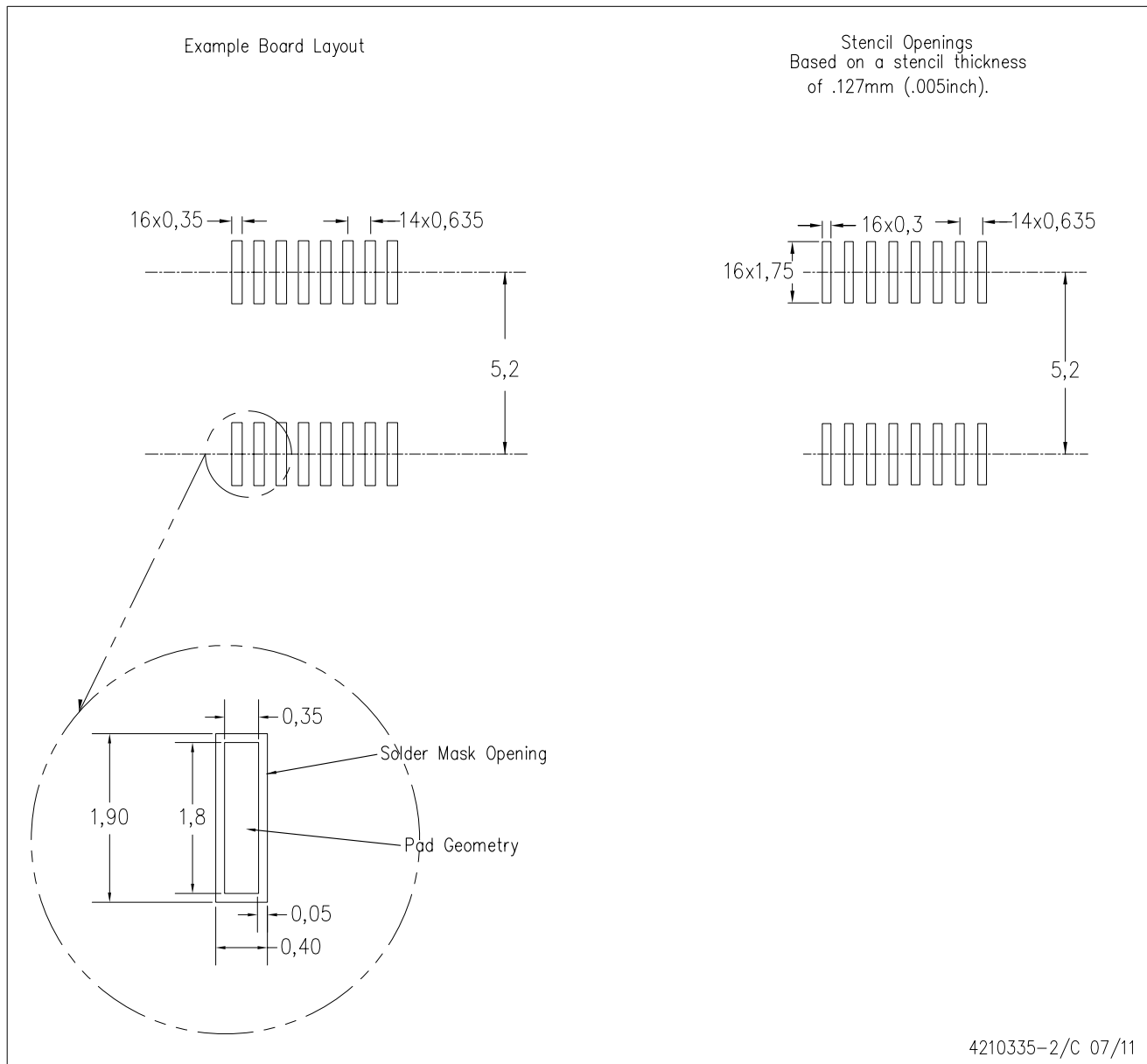
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com