



155Mbps to 2.5Gbps Burst-Mode Laser Driver

MAX3656

General Description

The MAX3656 is a burst-mode laser driver that operates at data rates from 155Mbps up to 2.5Gbps. The laser driver accepts either positive-referenced emitter-coupled logic (PECL) or current-mode logic (CML) data inputs and provides bias and modulation current for the laser diode. The device can switch the laser diode from a completely dark (off) condition to a full (on) condition (with proper bias and modulation currents) in less than 2ns. The MAX3656 incorporates DC-coupling between laser driver and laser diode and operates with a single-supply voltage as low as +3.0V.

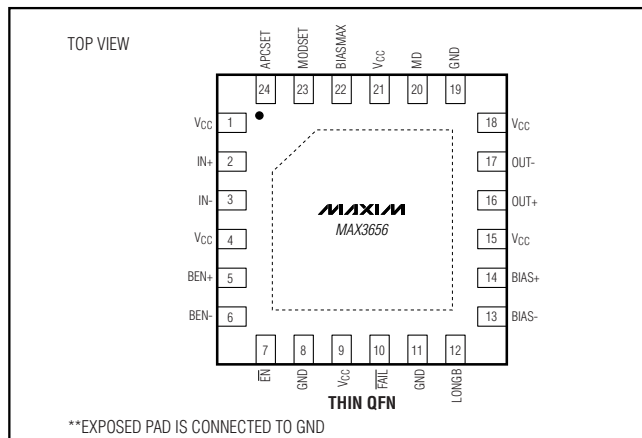
A digital automatic power-control (APC) loop is provided to maintain the average optical power over the full temperature range and lifetime. The APC loop is functional for a minimum burst on-time of 576ns and minimum burst off-time of 96ns, with no limit on the maximum burst on- or off-time. A fail monitor is provided to indicate when the APC loop can no longer maintain the average power. The MAX3656 can be configured for nonburst-mode applications (continuous mode) by connecting burst enable (BEN) high. For power saving, the MAX3656 provides enabling and disabling functionality. The modulation current can be set from 10mA to 85mA and the bias current can be set from 1mA to 70mA.

The MAX3656 is packaged in a small, 24-pin, 4mm x 4mm thin QFN package and consumes only 132mW (typ), excluding bias and modulation currents.

Applications

Fiber-to-the-Home (FTTH) and Fiber-to-the-Business (FTTB) Broadband Access Systems
Passive Optical Network (PON) Transmitters
APON, EPON, and GPON Upstream Transmitters

Pin Configuration



Features

- ◆ Multirate Operation from 155Mbps to 2.5Gbps
- ◆ Burst Enable/Disable Delay <2ns
- ◆ Burst On-Time of 576ns to Infinity
- ◆ Infinite Bias-Current Hold Time Between Bursts
- ◆ DC-Coupled Operation with Single +3.3V Power Supply
- ◆ 40mA Typical Supply Current
- ◆ Programmable Bias Current from 1mA to 70mA
- ◆ Programmable Modulation Current from 10mA to 85mA
- ◆ Automatic Average Power Control with Failure Monitor (No CAPC Capacitor Needed)
- ◆ APC Loop Initialization ≤3 Bursts

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3656E/D	—	Dice*	—
MAX3656ETG	-40°C to +85°C	24 Thin QFN-EP**	T2444-1
MAX3656ETG+	-40°C to +85°C	24 Thin QFN-EP**	T2444-1

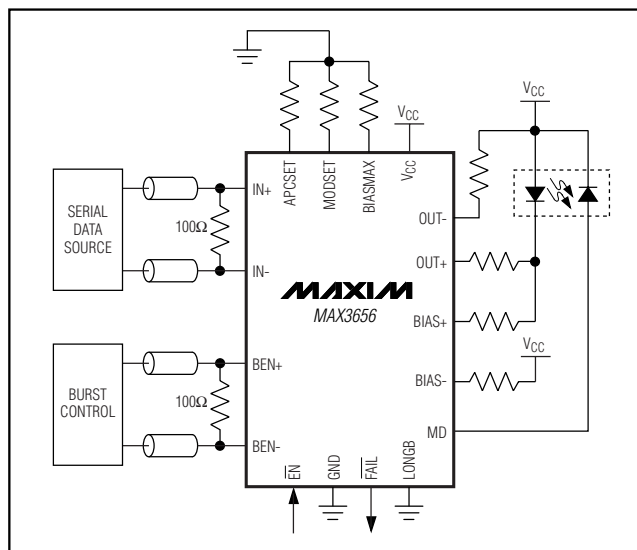
+ Denotes lead-free package.

*Dice are designed to operate from $T_J = -40^\circ\text{C}$ to $+120^\circ\text{C}$, but are only tested and guaranteed at $T_A = +25^\circ\text{C}$.

**EP = Exposed pad.

Functional Diagram appears at end of data sheet.

Typical Application Circuit



155Mbps to 2.5Gbps Burst-Mode Laser Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} -0.5V to +6.0V
 Current into BIAS+, BIAS-, OUT+, OUT- -20mA to +150mA
 Current into MD -5mA to +5mA
 Current into FAIL -10mA to +10mA
 Voltage at IN+, IN-, BEN+, BEN-, $\overline{EN}$,
 LONGB -0.5V to ($V_{CC} + 0.5V$)
 Voltage at MODSET, APCSET, BIASMAX -0.5V to +3.0V
 Voltage at OUT+, OUT- +0.5V to ($V_{CC} + 1.5V$)
 Voltage at BIAS+, BIAS- +0.5V to ($V_{CC} + 0.5V$)

Continuous Power Dissipation ($T_A = +85^\circ\text{C}$)
 24-Lead Thin QFN-EP
 (derate 27.8mW/ $^\circ\text{C}$ above $+85^\circ\text{C}$) 1805mW
 Operating Ambient Temperature
 Range (T_A) -40°C to $+85^\circ\text{C}$
 Operating Junction Temperature
 Range (T_J) -55°C to $+150^\circ\text{C}$
 Storage Ambient Temperature
 Range (T_{STG}) -55°C to $+150^\circ\text{C}$
 Processing Temperature (die) $+400^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Turn-On Time		10% to 90%	0.001		10	ms
Ambient Temperature			-40		+85	$^\circ\text{C}$
Data Mark Density		Average		50		%
Consecutive Identical Digits	CID				80	Bits
Data Rate			155		2500	Mbps
Monitor Diode Capacitance	C_{MD}	For minimum burst on-time (Note 1)			15	pF
Laser-to-Monitor Diode Gain	A_{LMD}	Δ (monitor current)/ Δ (laser current (above I_{TH})) (Notes 2, 3)	0.005		0.050	A/A
Extinction Ratio	r_e	$10 \log (P_1/P_0)$ (Note 3)	8.2		12.0	dB

Note 1: Larger MD capacitance increases the minimum burst on-time.

Note 2: Laser-to-monitor gain equals the laser slope efficiency multiplied by the photodiode responsivity multiplied by the losses due to laser-to-monitor diode coupling ($A_{LMD} = \eta_{LASER} \times \rho_{MONITORDIODE} \times L_{LASER-TO-MONITORDIODE}$), where L = laser-to-monitor diode coupling loss. A_{LMD} can also be calculated by:

$$A_{LMD} = \left(\frac{2 \times I_{MD}}{I_{MOD}} \right) \left(\frac{r_e - 1}{r_e + 1} \right)$$

where I_{MD} , I_{MOD} , and r_e (extinction ratio) are set externally.

Note 3: Operation outside this range degrades APC loop performance.

ELECTRICAL CHARACTERISTICS

(Typical values are at $V_{CC} = +3.3V$, $I_{BIAS} = 20mA$, $I_{MOD} = 25mA$, extinction ratio = 10dB, and $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	(Note 1)		40	70	mA
INPUT SPECIFICATIONS						
Differential Input Voltage	V_{IN} , V_{BEN}		0.2		1.6	V_{P-P}
Common-Mode Input Voltage	V_{CM}		$V_{CC} - 1.49$	$V_{CC} - 1.32$	$V_{CC} - V_{IN}/4$	V

155Mbps to 2.5Gbps Burst-Mode Laser Driver

MAX3656

ELECTRICAL CHARACTERISTICS (continued)

(Typical values are at $V_{CC} = +3.3V$, $I_{BIAS} = 20mA$, $I_{MOD} = 25mA$, extinction ratio = 10dB, and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Single-Ended Input Voltage	V _{BEN+} , V _{BEN-}			0.8			V
$\overline{EN}$ Input High Voltage	V _{IH}			2.0			V
$\overline{EN}$ Input Low Voltage	V _{IL}			0.8			V
FAIL Output High Voltage	V _{OH}	Sourcing 50μA, V _{CC} = 3.0V		2.4			V
FAIL Output Low Voltage	V _{OL}	Sinking 100μA, V _{CC} = 3.6V		0.4			V
BIAS GENERATOR							
Bias-On Current Range	I _{BIAS}	Voltage at BIAS pin ≥ 0.6V		1		70	mA
Bias-Off Current Range	I _{BIAS-OFF}	$\overline{EN}$ = high or BEN = low, V _{BIAS} ≤ 2.6V (Note 2)			5	100	μA
Bias-Current Temperature Stability		APC open loop	I _{BIAS} = 70mA	148			ppm/°C
			I _{BIAS} = 15mA	98			
Bias-Current Absolute Accuracy		APC open-loop I _{BIAS} > 20mA (Note 3)		-15		+15	%
BIASMAX Current-Setting Range				15		70	mA
APC LOOP							
MD Reverse-Bias Voltage	V _{MD}	With respect to V _{CC}		1.6			V
MD Bias-Setting Stability (Note 4)		I _{MD} = 50μA		-750		+750	ppm/°C
		I _{MD} = 1500μA		-480		+480	
MD Bias-Setting Accuracy (Note 3)		I _{MD} = 50μA		-25		+25	%
		I _{MD} = 1500μA		-15		+15	
MD DC-Current Range	I _{MD}	Average current into MD pin		50		1500	μA
APC Loop Initialization Time (Note 4)	t _{INIT}	Case 1 (Note 5) (LONGB = 0)		12			μs
		Case 2 (Note 6) (LONGB = 0)		2.12			
		Case 3 (Note 7) (LONGB = 0)		1.60	1.92		
LASER MODULATOR							
Modulation ON Current Range	I _{MOD}	Data rate ≤1.25Gbps		10		85	mA
		Data rate >1.25Gbps		10		60	
Modulation OFF Current	I _{MOD-OFF}	$\overline{EN}$ = high or BEN = low, I _N = low (Note 2)			16	150	μA
Modulation-Current Stability		(Note 13)		-480		+480	ppm/°C
Modulation-Current Absolute Accuracy		I _{MOD} > 15mA (Note 3)		-15		+15	%
Instantaneous Voltage at Modulator Output (OUT+)		10mA ≤ I _{MOD} < 60mA		0.6			V
		60mA ≤ I _{MOD} ≤ 85mA		0.75			
Modulation-Current Rise Time	t _R	10mA ≤ I _{MOD} ≤ 85mA (Notes 8, 13)			40	85	ps
Modulation-Current Fall Time	t _F	10mA ≤ I _{MOD} ≤ 85mA (Notes 8, 13)			40	85	ps
Output Over-/Undershoot					20		%
Deterministic Jitter (Notes 9, 13)	DJ	155Mbps to 1.25Gbps, 10mA ≤ I _{MOD} ≤ 85mA			17	45	psp-P
		1.25Gbps to 2.5Gbps, 10mA ≤ I _{MOD} ≤ 60mA			17	40	
Random Jitter	RJ	(Note 13)			0.8	1.4	psRMS

155Mbps to 2.5Gbps Burst-Mode Laser Driver

ELECTRICAL CHARACTERISTICS (continued)

(Typical values are at $V_{CC} = +3.3V$, $I_{BIAS} = 20mA$, $I_{MOD} = 25mA$, extinction ratio = 10dB, and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BURST-MODE SPECIFICATIONS							
Burst Enable Delay		APC closed loop (Notes 10, 11, 13)		2.3		ns	
Burst Disable Delay		APC closed loop (Notes 10, 12, 13)		2.0		ns	
Burst On-Time (Note 13)	tB-ON	155Mbps		2881		ns	
		622Mbps		720			
		1.25Gbps, 2.5Gbps		576			
Burst Off-Time (Note 13)	tB-OFF	155Mbps		192		ns	
		622Mbps		96			
		1.25Gbps, 2.5Gbps		96			
OPTICAL EVALUATION							
Optical Eye Diagram Mask Margin		ExcelLight SLT3120-DN laser diode (or equivalent)	155.52Mbps	42		%	
			622.08Mbps	30			
			1.25Gbps	23			
			2.48832Gbps	18			

Note 1: Excludes I_{BIAS} and I_{MOD} . Maximum value is specified at $I_{MOD} = 85mA$, $I_{BIAS} = 70mA$, and $I_{MD} = 1.5mA$.

Note 2: For safety purposes, both the bias and modulation currents are switched off if any of the current set pins ($BIASMAX$, $MODSET$) are grounded.

Note 3: Accuracy refers to part-to-part variation.

Note 4: APC loop initialization definitions:

BIAS Error: $I_{BIAS} - I_{BIASSET}$, where I_{BIAS} = the actual bias current and $I_{BIASSET}$ = the level of bias current set by the R_{APCSET} resistor.

Initialization Case 1: Continuous Mode Power-Up. In this case, $\overline{EN}$ = low, BEN = high, and then V_{CC} is ramped up from 0V to $\geq 3.0V$.

Initialization Case 2: Chip-Enable Reset. In this case, $3.0V \leq V_{CC} \leq 3.6V$, BEN = high, and then $\overline{EN}$ changes from high to low.

Initialization Case 3: Burst-Mode Startup. In this case, $3.0V \leq V_{CC} \leq 3.6V$, $\overline{EN}$ = low, and then BEN changes from low to high.

Note 5: I_{BIAS} error is less than 3.8mA (for an extinction ratio of 10dB and $I_{MD} = 1500\mu A$) within 12 μs from the time that $V_{CC} \geq 3.0V$.

Note 6: I_{BIAS} error is less than 3.8mA (for an extinction ratio of 10dB and $I_{MD} = 1500\mu A$) within 2.1 μs (typ) from the time that $\overline{EN} < 0.8V$.

Note 7: I_{BIAS} error must be less than 3.8mA (for an extinction ratio of 10dB and $I_{MD} = 1500\mu A$) at or before the end of the third burst following the transition of BEN from low to high. For the shortest burst on- and off-time (576ns and 96ns), this translates to 1.92 μs from when BEN toggles from low to high for the first time after startup.

Note 8: Rise and fall times are measured as 20% to 80% of the output amplitude with a repeating 0000011111.

Note 9: Deterministic jitter is measured with a continuous data pattern (no bursting) of $2^7 - 1$ PRBS + 80 consecutive ones + $2^7 - 1$ PRBS + 80 consecutive zeros.

Note 10: Measured electrically with a resistive load matched to the laser driver output.

Note 11: Enable delay is measured between (1) the time at which the rising edge of the differential burst enable input signal reaches the midpoint of the voltage swing, and (2) the time at which the combined output currents (bias and modulation) reach 90% of the final level set by R_{APCSET} , $R_{BIASMAX}$, and R_{MODSET} (after all transients such as overshoot, ringing, etc., have settled to within 10% of their final values). See Figure 1. Measurement done for $10mA \leq I_{MOD} \leq 85mA$ and $4mA \leq I_{BIAS} \leq 70mA$.

Note 12: Disable delay is measured between (1) the time at which the falling edge of the differential burst enable input signal reaches the midpoint of the voltage swing, and (2) the time at which the combined output currents (bias and modulation) fall below 10% of the bias on current (after transients have settled). See Figure 1. Measurement done for $10mA \leq I_{MOD} \leq 85mA$ and $4mA \leq I_{BIAS} \leq 70mA$.

Note 13: Guaranteed by design and characterization.

155Mbps to 2.5Gbps Burst-Mode Laser Driver

MAX3656

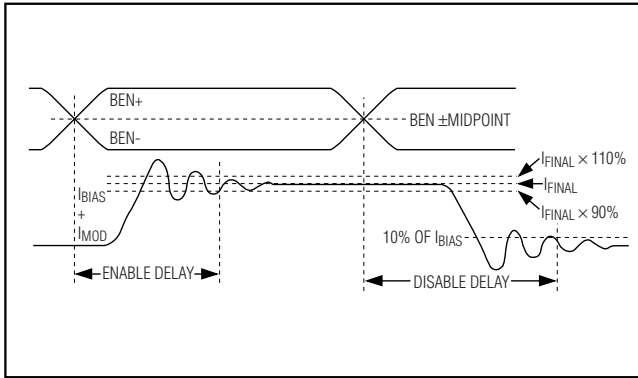


Figure 1. Enable and Disable Delay Times

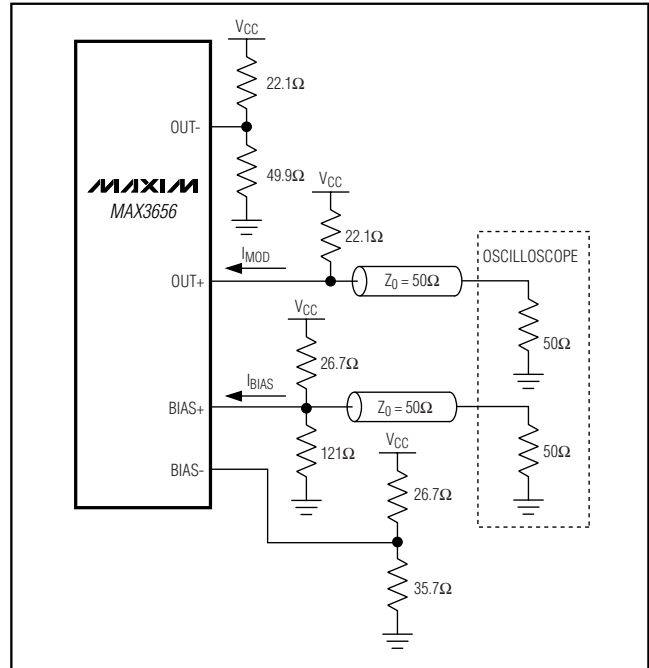
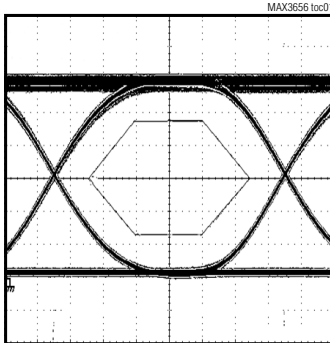


Figure 2. Output Termination for Characterization

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

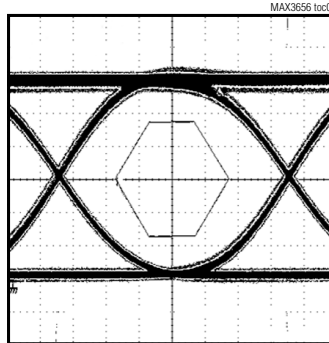
OPTICAL EYE DIAGRAM
(155.52Mbps, 117MHz FILTER,
PATTERN = PRBS $2^7 - 1 + 80$ CID)



EXCELIGHT SLT3120-DN LASER

AVERAGE OPTICAL POWER = -4dBm
EXTINCTION RATIO = 15.2dB
MASK MARGIN = 42%

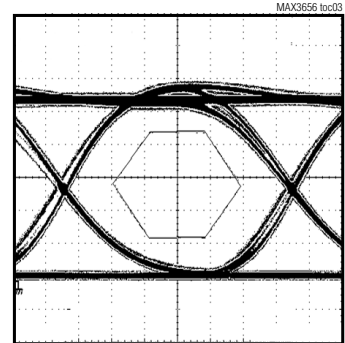
OPTICAL EYE DIAGRAM
(622.08Mbps, 467MHz FILTER,
PATTERN = PRBS $2^7 - 1 + 80$ CID)



EXCELIGHT SLT3120-DN LASER

AVERAGE POWER = -4dBm
EXTINCTION RATIO = 15.1dB
MASK MARGIN = 30%

OPTICAL EYE DIAGRAM
(1.25Gbps, 933MHz FILTER,
PATTERN = PRBS $2^7 - 1 + 80$ CID)



EXCELIGHT SLT3120-DN LASER

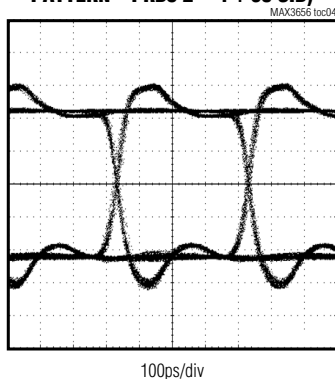
AVERAGE POWER = -3.5dBm
EXTINCTION RATIO = 14dB
MASK MARGIN = 23%

155Mbps to 2.5Gbps Burst-Mode Laser Driver

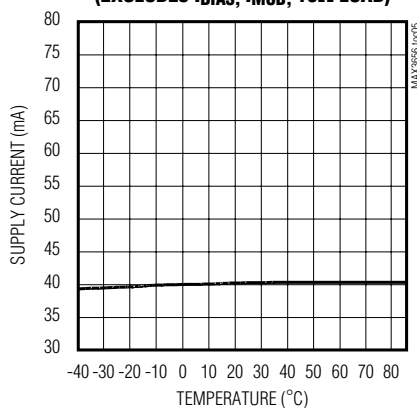
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

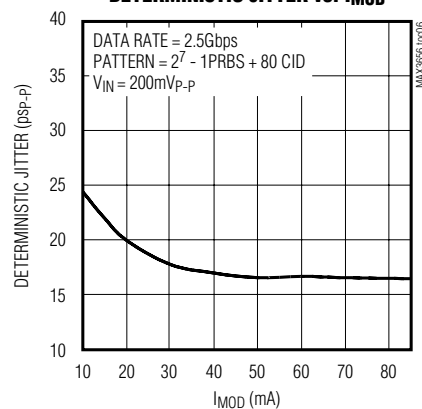
ELECTRICAL EYE DIAGRAM
(2.5Gbps, $I_{MOD} = 30\text{mA}$,
PATTERN = PRBS $2^7 - 1 + 80\text{ CID}$)



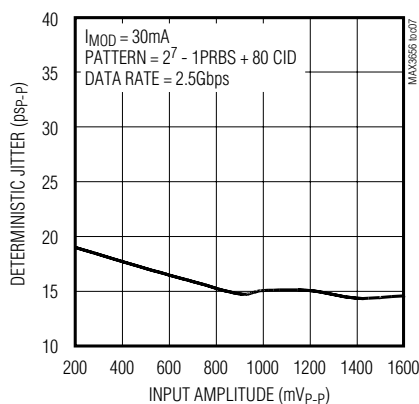
SUPPLY CURRENT vs. TEMPERATURE
(EXCLUDES I_{BIAS} , I_{MOD} , 15Ω LOAD)



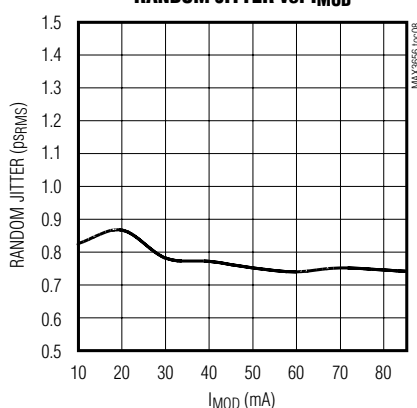
DETERMINISTIC JITTER vs. I_{MOD}



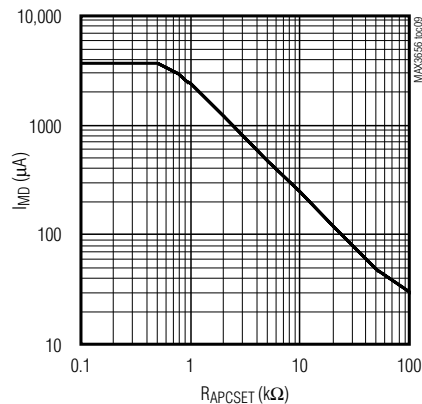
DETERMINISTIC JITTER
vs. INPUT AMPLITUDE



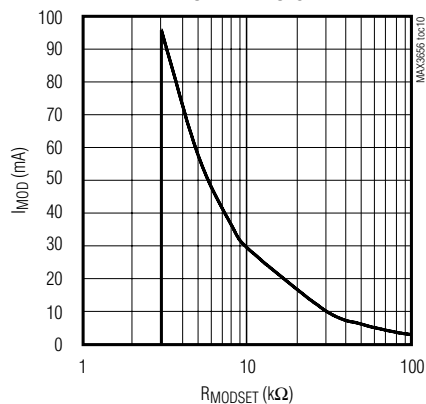
RANDOM JITTER vs. I_{MOD}



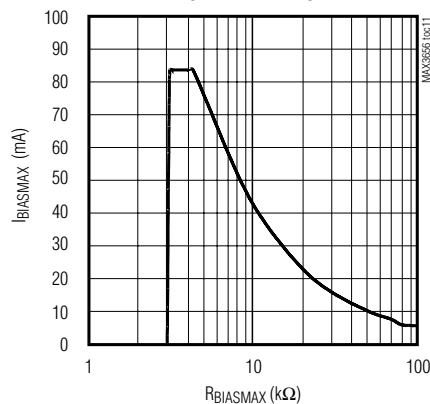
I_{MOD} vs. R_{APCSET}



I_{MOD} vs. R_{MODSET}



$I_{BIASMAX}$ vs. $R_{BIASMAX}$

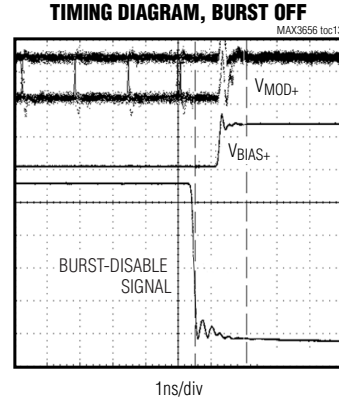
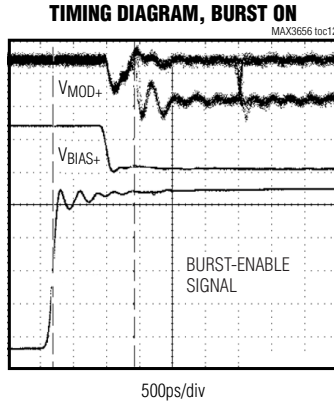


155Mbps to 2.5Gbps Burst-Mode Laser Driver

MAX3656

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 4, 9, 15, 18, 21	VCC	Power-Supply Voltage
2	IN+	Noninverting Data Input with On-Chip Biasing
3	IN-	Inverting Data Input with On-Chip Biasing
5	BEN+	Noninverting Burst-Enable Input with On-Chip Biasing
6	BEN-	Inverting Burst-Enable Input with On-Chip Biasing
7	$\overline{\text{EN}}$	TTL/CMOS Enable Input. Low for normal operation. Float or pull high to disable laser bias and modulation currents.
8, 11, 19	GND	Power-Supply Ground
10	$\overline{\text{FAIL}}$	TTL/CMOS Failure Output. Indicates APC failure when low.
12	LONGB	TTL/CMOS Long Burst (See the <i>Setting the LONGB Input Pin</i> Section)
13	BIAS-	Inverting Laser Bias-Current Output. Connect through 15 Ω to VCC.
14	BIAS+	Noninverting Laser Bias-Current Output. Bias current flows into this pin when BEN is high. Minimize capacitance on this pin.
16	OUT+	Noninverting Laser Modulation-Current Output. Modulation current flows into this pin when BEN and IN are high.
17	OUT-	Inverting Laser Modulation-Current Output. Connect through 15 Ω to VCC.
20	MD	Monitor Diode Input. Connect this pin to the anode of the monitor diode. Leave floating for open-loop operation. Minimize capacitance on this pin.
22	BIASMAX	Maximum Bias Current Set. A resistor connected from this pin to ground sets the maximum bias current. The bias current cannot exceed this level. The APC loop controls the bias current up to the level of the BIASMAX. For APC open-loop operation, this pin sets the laser bias current.
23	MODSET	Modulation Current Set. A resistor connected from this pin to ground sets the desired modulation current.
24	APCSET	Average Power Control Set. A resistor connected from this pin to ground sets the desired average optical power. Connect a 50k Ω resistor to ground for APC open-loop operation.
EP	Exposed Pad	Ground. This pad must be soldered to ground.

155Mbps to 2.5Gbps Burst-Mode Laser Driver

Detailed Description

The MAX3656 laser driver has three main parts: a high-speed modulator, a high-speed bias driver, and a laser-biasing block with automatic power control (see the *Functional Diagram*). Both the bias and modulation output stages are composed of differential pairs with programmable current sources. The circuit design is optimized for high-speed, low-voltage (3.3V), DC-coupled operation. The device is ideal for burst-mode operation with turn-on and turn-off times less than 2ns. The MAX3656 can be configured for nonburst-mode applications (continuous mode) by connecting BEN high.

The MAX3656 modulation output is optimized for driving a 15 Ω load. The modulation current can swing up to 85mA for data rates less than or equal to 1.25Gbps and up to 60mA for data rates greater than 1.25Gbps when the laser is DC-coupled. To interface with the laser diode, a damping resistor (R_D) is required for impedance matching. The combined resistance due to the series damping resistor and the equivalent series resistance (ESR) of the laser diode should be equal to 15 Ω . The OUT- pin should be connected with a 15 Ω resistor to VCC. To reduce optical output aberrations and duty-cycle distortion caused by laser diode parasitic inductance, an RC shunt network is necessary.

The currents in the BIAS output switch at high speeds when bursting. Therefore, the BIAS+ pin should be connected directly through a resistor to the cathode of the laser. The BIAS- pin should be connected to VCC through a 15 Ω resistor.

Automatic Power Control

To maintain constant average optical power, the MAX3656 incorporates a digital automatic power-control (APC) loop to compensate for the changes in laser threshold current over temperature and lifetime. A back-facet photodiode mounted in the laser package converts the optical power into a photocurrent. The APC loop adjusts the laser bias current so the monitor current is matched to a reference current set by RAPCSET.

At startup, the APC loop traverses through a pseudo-binary search algorithm to set the proper monitor current that translates to the proper bias current. When BEN is high, the APC loop maintains constant optical power by digitally controlling the bias current. When BEN is low, the APC loop digitally stores the bias current value of the previous burst. The APC loop is reset in two ways, either power cycling or toggling the $\overline{EN}$ pin.

An external resistor ($R_{BIASMAX}$) sets the maximum allowable bias current during closed-loop operation and sets the bias current during open-loop operation. An APC fail-

ure flag ($\overline{FAIL}$) is set low during initialization and when the bias current cannot be adjusted to achieve the desired average optical power.

APC closed-loop operation requires that the user set three currents with external resistors connected between GND, BIASMAX, MODSET, and APCSET pins. Detailed guidelines for these resistor settings are described in the *Design Procedure* section.

If necessary, the MAX3656 is fully operational without APC. To operate the MAX3656 open loop, connect a 50k Ω resistor from APCSET to ground and leave the MD pin unconnected. In this case, two external resistors connected from BIASMAX and MODSET to GND directly set the laser current.

APC Failure Monitor

The MAX3656 provides an APC failure monitor (TTL) to indicate an APC loop-tracking failure. $\overline{FAIL}$ is set low when the APC loop cannot adjust the bias current to maintain the desired monitor current. For example, the laser diode requires more bias current (to maintain a constant optical output) than maximum bias current set by $R_{BIASMAX}$. The bias current is limited and $\overline{FAIL}$ is asserted. In an alternate example, assume that a circuit failure causes the cathode of the laser diode to be shorted to GND, thereby causing an uncontrolled high optical output. In this case, the APC loop cannot decrease the user current, and $\overline{FAIL}$ is asserted. $\overline{FAIL}$ is also set low during initialization.

Slow-Start

For safety reasons, at initial power-up or after toggling $\overline{EN}$, the MAX3656 incorporates a slow-start circuit that provides a typical delay of 450ns during the beginning of APC loop initialization.

Enable Control

The MAX3656 features a chip-enable function. When $\overline{EN}$ is high, the bias and modulation currents are off and the digital state of the APC loop is reset. When $\overline{EN}$ is toggled from a high to a low, the APC loop begins initialization. The initialization time is typically 2.1 μ s ($LONGB = \text{low}$) and 3.72 μ s ($LONGB = \text{high}$).

APC Loop Initialization

The digital APC loop is reset whenever the power is turned off and/or the $\overline{EN}$ input is driven high. When power is turned on or when $\overline{EN}$ is toggled low, the APC loop automatically performs an initialization routine that quickly adjusts the bias current from its reset level to its initialized level. The initialized bias current level is defined to be within 3.8mA of the final bias current level set by the APCSET resistor. Once initialized, the APC

155Mbps to 2.5Gbps Burst-Mode Laser Driver

loop enters its fine-adjustment mode of operation and adjusts the bias current to match the level set by the APCSET resistor. There are three different cases in which the APC loop starts initialization, and each has a unique initialization time. These cases are defined as follows:

- **Continuous-Mode Power-Up**

In continuous-mode power-up, the chip is enabled ($\overline{EN}$ = low) and the burst-enable input is high (BEN = high) when power is applied to the laser driver. APC loop initialization begins when the power-supply voltage rises above the minimum specified limit of +3.0V. The BEN input remains high indefinitely and the laser driver operates in continuous (nonbursting) mode. In this case, the initialization time is 12 μ s (typ).

- **Chip-Enable Reset**

In chip-enable reset, the power-supply voltage is within the specified limits and BEN is high. The chip-enable input ($\overline{EN}$) is initially high (chip disabled and APC loop reset), and then it is driven low (chip-enabled). In this case, APC loop initialization begins when the voltage at $\overline{EN}$ drops below the specified $\overline{EN}$ input low voltage of 0.8V. After initialization begins, the laser driver can be operating in burst mode (BEN toggling high and low) or continuous mode (BEN = high). In this case, the initialization time is 2.1 μ s (typ).

- **Burst-Mode Startup**

In burst-mode startup, the power-supply voltage is within the specified limits and the chip is enabled ($\overline{EN}$ = low). The burst-enable input is low (BEN = low) and has not been in the high state since the APC loop was reset. APC loop initialization begins when the BEN input is driven high. After initialization begins, the laser driver can be operating in burst mode (BEN toggling high and low) or continuous mode (BEN = high). In this case, the initialization time is 1.6 μ s (typ).

In each of the three cases listed, initialization is complete within three bursts (bursts must comply with specified burst on- and burst off-time) or the time specified in the *Electrical Characteristics* table, whichever comes first.

Burst-Mode Operation

The bias and modulation outputs (BIAS+ and OUT+) can be switched on and off quickly using the differential burst-enable inputs (BEN+ and BEN-). Once the APC loop has initialized, the bias and modulation outputs are switched on when BEN+ = high and BEN- = low and are switched off when BEN+ = low and BEN- = high.

When BEN is switched on, the laser driver sinks the bias and modulation currents set by the APCSET, BIASMAX, and MODSET resistors within the maximum BEN delay time of 2.3ns. For stable APC loop operation, the minimum burst length is limited to the burst on-time listed in the *Electrical Characteristics* table. The maximum burst-on time is unlimited.

When BEN is switched off, the bias and modulation currents fall below the specified bias-off and modulation-off currents within the maximum burst disable delay time of 2.0ns. For stable APC loop operation, the minimum burst off-time is limited to the value listed in the *Electrical Characteristics* table. The maximum burst off-time is unlimited.

Short-Circuit Protection

The MAX3656 provides short-circuit protection for the modulation and bias-current sources. If BIASMAX or MODSET is shorted to ground, the bias and modulation outputs are turned off.

Design Procedure

When designing a laser transmitter, the optical output is usually expressed in terms of average power and extinction ratio. Table 1 shows the relationships helpful in converting between the optical average power and the modulation current. These relationships are valid if the mark density and duty cycle of the optical waveform are 50%.

Programming the Modulation Current

For a given laser power (P_{AVG}), slope efficiency (η), and extinction ratio (r_e), the modulation current can be calculated using Table 1. See the I_{MOD} vs. R_{MODSET} graph in the *Typical Operating Characteristics*, and select the value of R_{MODSET} that corresponds to the required current at +25°C.

Table 1. Optical Power Definition

PARAMETER	SYMBOL	RELATION
Average power	P_{AVG}	$P_{AVG} = (P_0 + P_1) / 2$
Extinction ratio	r_e	$r_e = P_1 / P_0$
Optical power high	P_1	$P_1 = 2P_{AVG} \times r_e / (r_e + 1)$
Optical power low	P_0	$P_0 = 2P_{AVG} / (r_e + 1)$
Optical amplitude	P_{P-P}	$P_{P-P} = P_1 - P_0$
Laser slope efficiency	η	$\eta = P_{P-P} / I_{MOD}$
Modulation current	I_{MOD}	$I_{MOD} = P_{P-P} / \eta$
Laser-to-monitor diode gain	$ALMD$	$(2 \times I_{MD} / I_{MOD})(r_e - 1) / (r_e + 1)$

155Mbps to 2.5Gbps Burst-Mode Laser Driver

Programming the Bias Current

When the MAX3656 is used in open-loop operation, the RBIASMAX resistor determines the bias current. To select this resistor, determine the required bias current. See the IBIASMAX vs. RBIASMAX graph in the *Typical Operating Characteristics*, and select the value of RBIASMAX that corresponds to the required current. For open-loop operation, connect a 50k Ω resistor from RAPCSET to GND, and leave the MD pin open.

When using the MAX3656 in closed-loop operation, the RBIASMAX resistor sets the maximum bias current available to the laser diode over temperature and lifetime. The APC loop can subtract from this maximum value, but cannot add to it. See the IBIASMAX vs. RBIASMAX graph in the *Typical Operating Characteristics* and select the value of RBIASMAX that corresponds to the end-of-life bias current at +85°C.

Programming the APC Loop

When using the MAX3656's APC feature, program the average optical power by adjusting the APCSET resistor. To select this resistor, determine the desired monitor current to be maintained over temperature and lifetime. See the I_{MD} vs. RAPCSET graph in the *Typical Operating Characteristics* and select the value of RAPCSET that corresponds to the required current.

Setting the LONGB Input Pin

Set the LONGB pin according to Table 2 to optimize APC loop operation.

Interfacing with Laser Diodes

To minimize optical output aberrations caused by signal reflections at the electrical interface to the laser diode, a series-damping resistor (R_D) is required (see the *Functional Diagram*). Additionally, the MAX3656 outputs are optimized for a 15 Ω load. Therefore, the series combination of R_D and R_L (where R_L represents the laser-diode resistance) should equal 15 Ω . Typical values for R_D are 8 Ω to 13 Ω . For best performance, a bypass capacitor (0.01 μ F typical) should be placed as close as possible to the anode of the laser diode. An RC shunt network between the OUT+ pin and ground helps minimize optical output aberrations. Starting values for most coaxial lasers are $R = 56\Omega$ in series with $C = 10$ pF. Adjust these values experimentally until the

Table 2. Setting the LONGB Input Pin

LONGB	CONDITION
0	Burst on-time $\leq 1.2\mu$ s
0 or 1	Burst on-time $> 1.2\mu$ s or continuous mode operation
1	Data rates of 155Mbps

optical output waveform is optimized (refer to Application Note HFAN 3.0: *Interfacing Maxim's Laser Drivers with Laser Diodes*).

Input Termination Requirements

The MAX3656 data and BEN inputs are internally biased. Although the inputs are compatible with LVPECL signals, it is not necessary to drive the MAX3656 with a standard LVPECL signal. While DC-coupled, the MAX3656 operates properly as long as the specified common-mode voltage and differential voltage swings are met. Because of the on-chip biasing network (Figure 3), the MAX3656 inputs self-bias to the proper operating point to accommodate AC-coupling.

See Figures 4 and 5 for connecting to PECL or CML data outputs.

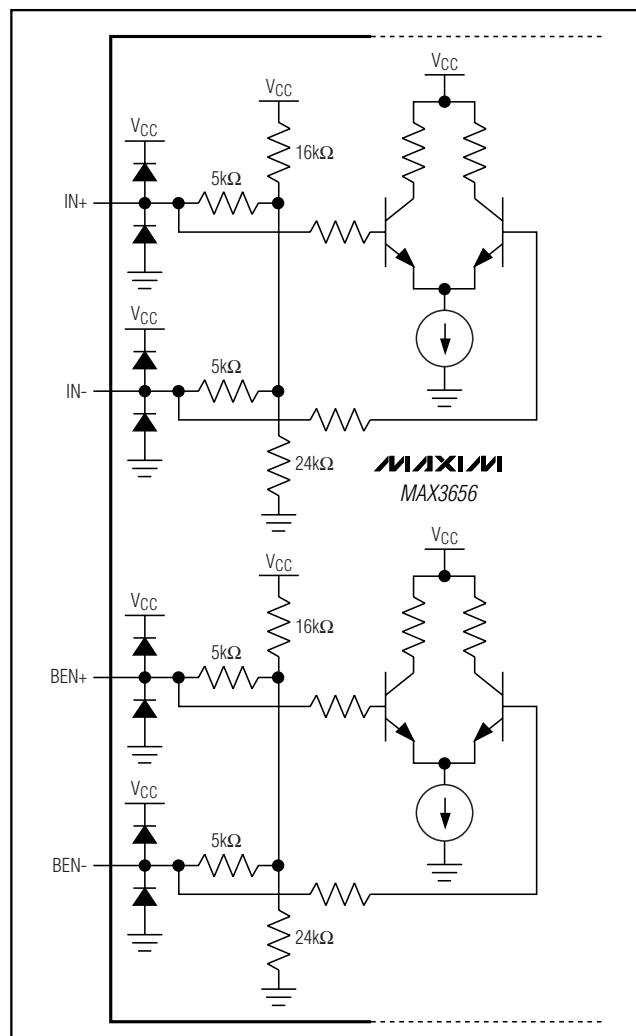


Figure 3. MAX3656 Internal Biasing

155Mbps to 2.5Gbps Burst-Mode Laser Driver

Design Example

Select Laser

Select a communication-grade laser for the proper data rate. Assume the laser output average power is $P_{AVG} = 0\text{dBm}$, the operating temperature is -40°C to $+85^{\circ}\text{C}$, and the laser diode has the following characteristics: wavelength: $\lambda = 1.3\mu\text{m}$, threshold current: $I_{TH} = 22\text{mA}$ at $+25^{\circ}\text{C}$, threshold temperature coefficient: $\beta_{TH} = 1.3\%/^{\circ}\text{C}$, laser-to-monitor transfer: $\rho_{MON} = 0.2\text{A/W}$ ($\rho_{MON} = \rho_{MONITOR/DIODE} \times L_{LASER-TO-MONITOR/DIODE}$), and laser slope efficiency: $\eta = 0.05\text{mW/mA}$ at $+25^{\circ}\text{C}$.

Determining R_{APCSET}

The desired monitor diode current is estimated by $I_{MD} = P_{AVG} \times \rho_{MON} = 200\mu\text{A}$. The I_{MD} vs. R_{APCSET} graph in the *Typical Operating Characteristics* shows R_{APCSET} at $12\text{k}\Omega$.

Determining R_{MODSET}

Assuming $r_e = 10$ and an average power of 0dBm (1mW), the peak-to-peak optical power $P_{P-P} = 1.64\text{mW}$ (Table 1). The required modulation current is $1.64(\text{mW})/0.05(\text{mW/mA}) = 32.8\text{mA}$. The I_{MOD} vs. R_{MODSET} graph in the *Typical Operating Characteristics* shows R_{MODSET} at $9\text{k}\Omega$.

Determining $R_{BIASMAX}$

Determine the maximum threshold current ($I_{TH(MAX)}$) at $T_A = +85^{\circ}\text{C}$ and end of life. Assuming ($I_{TH(MAX)} = 50\text{mA}$, the maximum bias current should be:

$$I_{BIASMAX} = I_{TH(MAX)}$$

In this example, $I_{BIASMAX} = 50\text{mA}$. The $I_{BIASMAX}$ vs. $R_{BIASMAX}$ graph in the *Typical Operating Characteristics* shows $R_{BIASMAX}$ at $8\text{k}\Omega$.

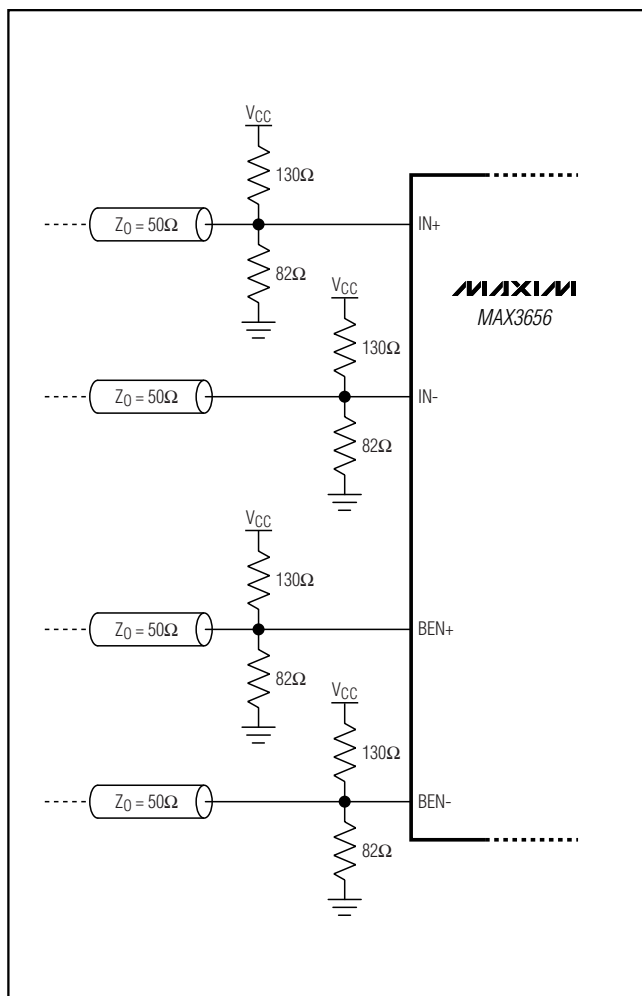


Figure 4. Connecting to PECL Outputs

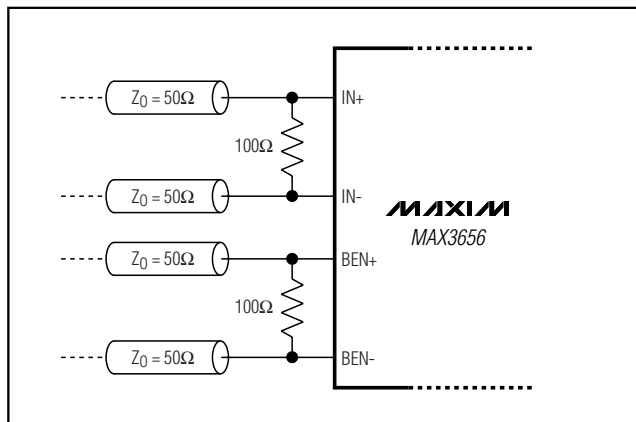


Figure 5. Connecting to CML Outputs

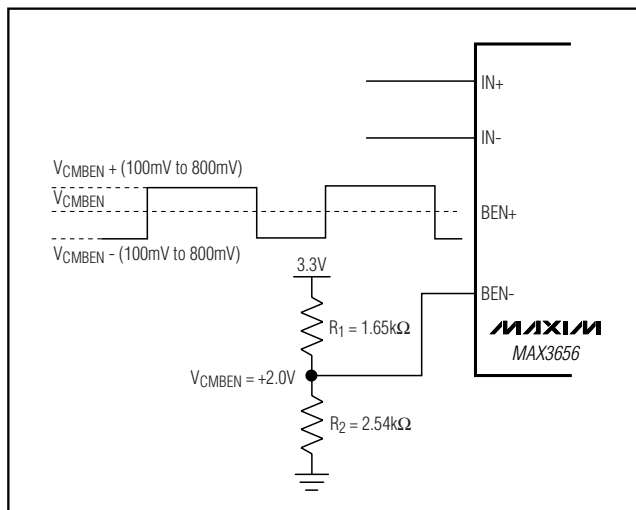


Figure 6. Single-Ended Biasing for Burst Enable

155Mbps to 2.5Gbps Burst-Mode Laser Driver

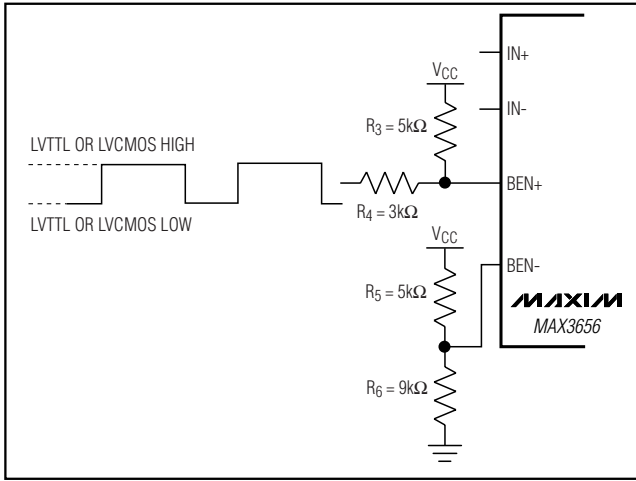


Figure 7. Single-Ended LVTTTL or LVCMOS Biasing for Burst Enable

Applications Information

Running Burst Enable Single-Ended

With PECL signal levels, for single-ended operation of burst enable, connect the BEN+ to the burst-enable control. Connect a resistor (R1) from VCC to BEN- and resistor (R2) from BEN- to ground. The parallel combination of R1 and R2 should be less than 1kΩ. Choose the values of R1 and R2 to set the common-mode voltage in the range defined in the *Electrical Characteristics* table (see Figure 6).

With LVTTTL or LVCMOS signal levels, for single-ended operation of burst enable connect a 3kΩ (R4) resistor from the burst-enable signal to BEN+. Connect a 5kΩ (R3) resistor from VCC to BEN+. Connect a 5kΩ resistor (R5) from VCC to BEN- and a 9kΩ resistor (R6) from BEN- to ground. For typical LVTTTL or LVCMOS specifications of VCC to 2.0V for a high and 0.8V to 0V for a low, the LVTTTL or LVCMOS sources a maximum of 75μA and sinks a maximum of 500μA. See Figure 7 for setting up the single-ended LVTTTL or LVCMOS biasing for burst enable.

Burst Enable Delay

For some lasers, replacing the 15Ω resistors connected from OUT- and BIAS- to VCC with surface-mount signal diodes can reduce burst-enable delay.

Wire-Bonding Die

For high-current density and reliable operation, the MAX3656 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques. Die-pad size is 4.03 mils (102.4μm) square, and die size is 98 mils × 65 mils (2489.2μm × 1651μm).

Table 3. Pad Locations

PAD	NAME	COORDINATES (microns)	
1	VCC	51.2	1146.0
2	IN+	51.2	1003.2
3	IN-	51.2	856.2
4	VCC	51.2	709.2
5	BEN+	51.2	198.2
6	BEN-	51.2	51.2
7	GND	142.2	-111.2
8	$\overline{\text{EN}}$	282.2	-111.2
9	GND	423.6	-111.2
10	VCC	608.4	-111.2
11	$\overline{\text{FAIL}}$	1569.6	-111.2
12	GND	1738.2	-111.2
13	LONGB	1881.0	-111.2
14	GND	2023.8	-111.2
15	BIAS-	2257.6	87.6
16	BIAS+	2257.6	236.0
17	VCC	2257.6	453.0
18	OUT+	2257.6	626.6
19	OUT+	2257.6	768.0
20	OUT-	2257.6	931.8
21	OUT-	2257.6	1073.2
22	VCC	2257.6	1217.4
23	GND	2039.2	1242.6
24	MD	1893.6	1242.6
25	GND	1749.4	1242.6
26	VCC	1603.8	1242.6
27	GND	1461.0	1242.6
28	BIASMAX	700.8	1242.6
29	MODSET	555.2	1242.6
30	APCSET	412.4	1242.6
31	GND	262.6	1242.6

Layout Considerations

To minimize inductance, keep the connections between the MAX3656 output pins and laser diode as close as possible. Optimize the laser diode performance by placing a bypass capacitor as close as possible to the laser anode. Take extra care to minimize stray parasitic capacitance on the BIAS and MD pins. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground planes to minimize EMI and crosstalk.

MAX3656

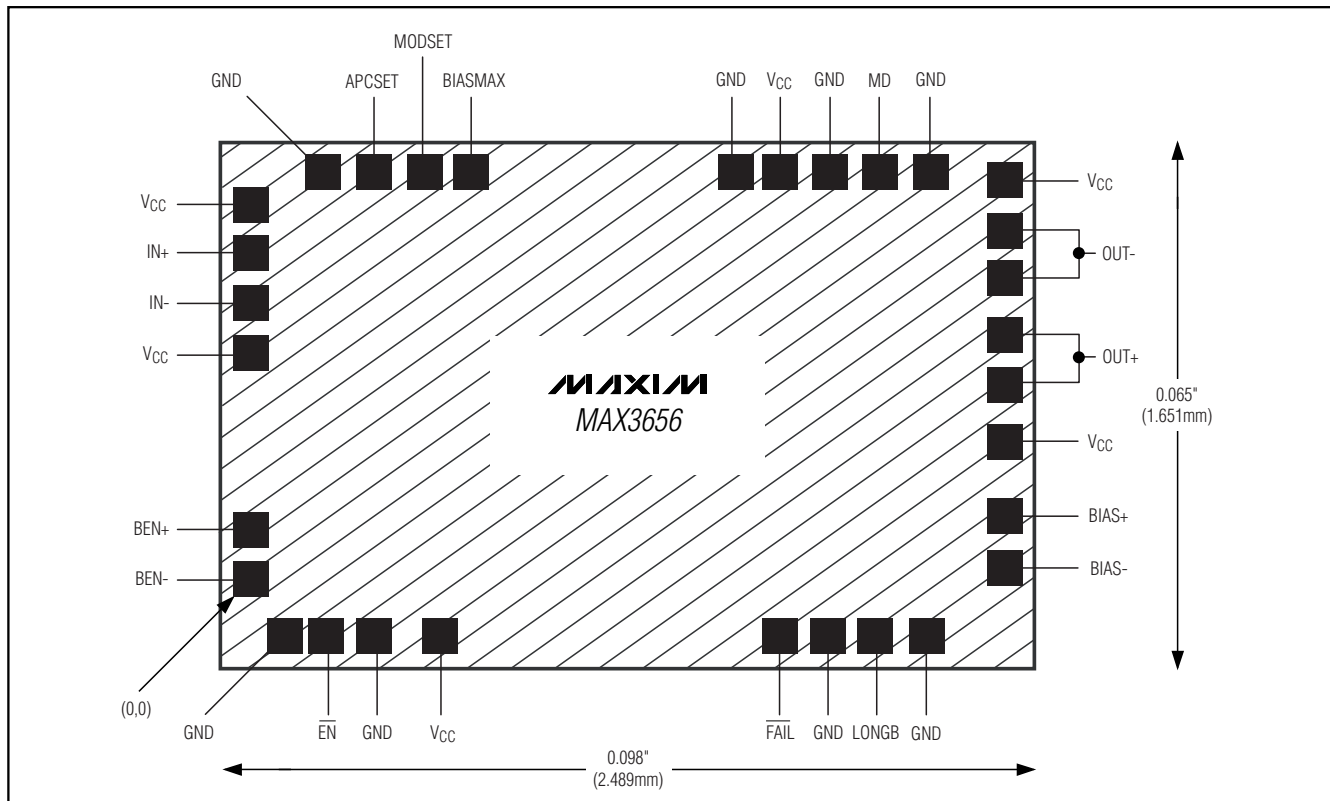
that Maxim products are neither designed nor authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application in which the failure of a Maxim product could create a situation where personal injury or death can occur.

The schematic diagram illustrates the internal architecture of the MAX3656 LED driver. Key components and connections include:

- Inputs:** IN+, IN-, BEN+, and BEN- are connected to the input drivers.
- Current Source:** A current source is connected to the output drivers, with a feedback loop involving a DAC, DSP, and ASP.
- Feedback Loop:** The feedback loop includes a DAC, DSP, and ASP, which are connected to the output drivers.
- Output Drivers:** The output drivers are connected to the output terminals OUT+ and OUT-.
- External Components:** Resistors R_D, R_{COMP}, R_{MODSET}, R_{BIAS_MAX}, and R_{AP_CSET} are connected to the output drivers and feedback loop. A capacitor C_{COMP} is connected to the output drivers.
- LEDs:** Two LEDs are connected to the output drivers and VCC.

155Mbps to 2.5Gbps Burst-Mode Laser Driver

Chip Topography



Chip Information

TRANSISTOR COUNT: 8153

SUBSTRATE: Electrically isolated

DIE SIZE: 2489.2 μ m X 1651 μ m

DIE THICKNESS: 12 mils

PROCESS: SiGe bipolar

MAX3656

24L QFN THIN.EPS

The drawing illustrates the mechanical specifications of a 28-pin Thin QFN package. It includes three main views: TOP VIEW, BOTTOM VIEW, and SIDE VIEW, along with a detail of the terminal profile.

- TOP VIEW:** Shows the package footprint with dimensions D (width), E (height), and $D/2$ (half-width). It features a hatched INDEX AREA ($D/2 \times E/2$) and a 10 MARKING. Surface finish requirements are indicated as $2X \Delta 0.15 C$ and $2X \Delta 0.13 C$.
- BOTTOM VIEW:** Shows the pin array with dimensions $D2$, $D2/2$, $E2$, and $E2/2$. It includes a detail of the pin profile (DETAIL A) and a note for PIN #1 I.D. (0.35×0.35). Surface finish requirements are indicated as $2X \Delta 0.10 C A B$ and $2X \Delta 0.13 C$.
- SIDE VIEW:** Shows the package height and the SEATING PLANE. It includes a note for the terminal profile ($2X \Delta 0.10 C$) and a note for the terminal profile ($2X \Delta 0.08 C$).
- DETAIL A:** A cross-sectional view of the terminal profile, showing the terminal tip and the terminal body. It includes a note for the terminal profile ($2X \Delta 0.10 C$) and a note for the terminal profile ($2X \Delta 0.08 C$).

-DRAWING NOT TO SCALE-

155Mbps to 2.5Gbps Burst-Mode Laser Driver

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
JEDEC	VGG3			VGGC			VGGD-1			VGGD-2			VGGE		

EXPOSED PAD VARIATIONS								
PKG CODES	D2			E2			DOWN BONDS ALLOWED	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO	
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES	
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO	
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3. N IS THE TOTAL NUMBER OF TERMINALS.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC M0220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.

10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

11. COPLANARITY SHALL NOT EXCEED 0.08mm

12. WARPAGE SHALL NOT EXCEED 0.10mm

13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ± 0.05 .

-DRAWING NOT TO SCALE-

	
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm	
APPROVAL	DOCUMENT CONTROL NO. 21-0139
REV. D	2/2

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