

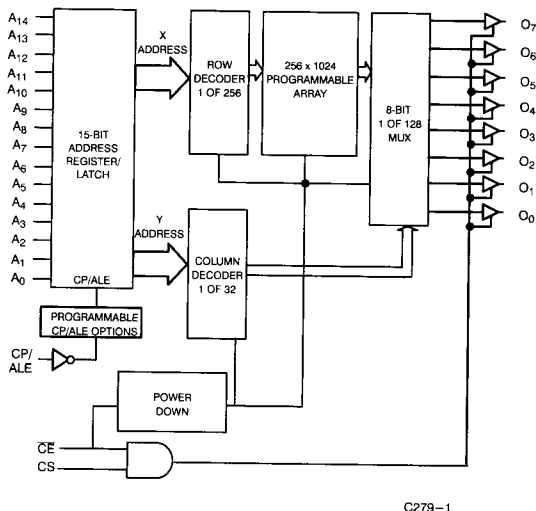


Reprogrammable 32K x 8 Registered PROM

Features

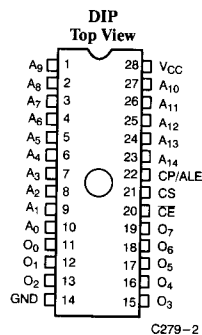
- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
 - 3 ns max. set-up
 - 35 ns clock to output
- Low power
 - 660 mW (commercial)
 - 715 mW (military)
- Programmable address latch enable input
- Optional registered/latched address inputs
- EPROM technology, 100% programmable
- Slim 300-mil, 28-pin plastic or hermetic DIP
- 5V $\pm 10\%$ V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 200V static discharge

Logic Block Diagram

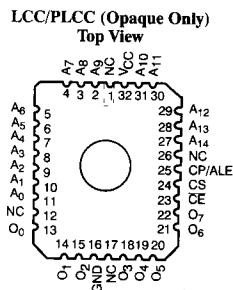


C279-1

Pin Configurations



C279-2



C279-3

Selection Guides

		7C279-35	7C279-45	7C279-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		130	130
Maximum Standby Current (mA)	Commercial	30	30	30
	Military		40	40

Functional Description

The CY7C279 is a high-performance 32K word by 8-bit CMOS PROM. When deselected, the CY7C279 automatically powers down into a low power standby mode. It is packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

The CY7C279 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with

Power Applied - 55°C to +125°C

Supply Voltage to Ground Potential - 0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs

in High Z State - 0.5V to +7.0V

DC Input Voltage - 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

Electrical Characteristics Over the Operating Range^[3,4]

Parameter	Description	Test Conditions	7C279-35		7C279-45, 55		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 2.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC}	2.0	V _{CC}	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	μA
V _{CD}	Input Clamp Diode Voltage		Note 4				
I _{OZ}	Output Leakage Current	0 ≤ V _{OUT} ≤ V _{CC} , Output Disabled ^[5]	-40	+40	-40	+40	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[6]	-20	-90	-20	-90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., CS ≥ V _{IH} I _{OUT} = 0 mA	Commercial			120	mA
			Military			130	
I _{SB}	Standby Supply Current	V _{CC} = Max., CE ≥ V _{IH} I _{OUT} = 0 mA	Commercial			30	mA
			Military			40	
V _{PP}	Programming Supply Voltage		12	13	12	13	V
I _{PP}	Programming Supply Current			50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4	V

Notes:

- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the "instant on" case temperature.

encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C279, address registers are provided to easily interface with microprocessors that deliver addresses around a rising clock edge. A programmable bit is provided to select between latched and registered address inputs. The default is registered inputs, which will sample the address on the RISING EDGE of CP and load the address register. The latched address option will recognize any address changes while the ALE pin is active and load the address into the address latches on the deactivating edge of ALE. If the latched address option is selected, another programmable bit is provided for the user to select the polarity that will define ALE active, with the default being active HIGH.

UV Erasure 7258 Wsec/cm²

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

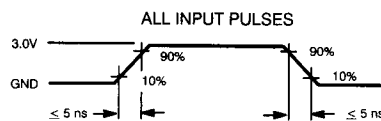
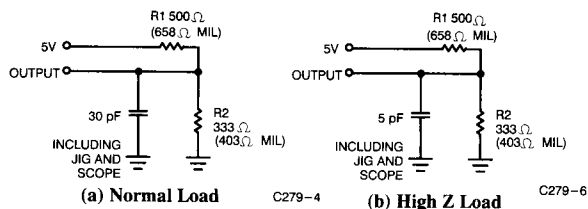
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	- 40°C to +85°C	5V ±10%
Military ^[2]	- 55°C to +125°C	5V ±10%

- See the last page of this specification for Group A subgroup testing information.
- See "Introduction to CMOS PROMs" in this Data Book for general information on testing.

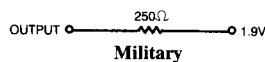
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms^[4]



Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[3,4]

Parameter	Description	7C279-35		7C279-45		7C279-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Data Valid (Latched Mode)		35		45		55	ns
t_{CO}	Clock to Output Valid (Registered Mode)		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20		20	ns
t_{ACS}	Chip Select Active to Output Valid		15		20		20	ns
t_{AR}	Address Set-up to Clock Rise (Registered Mode)	3		10		10		ns
t_{RA}	Address Hold from Clock Rise (Registered Mode)	6		10		10		ns
t_{ADH}	Data Hold from Clock Rise (Registered Mode)	5		5		5		ns
t_{SU}	Address Set-up to ALE Inactive (Latched Mode)	5		10		10		ns
t_{HD}	Address Hold from ALE Inactive (Latched Mode)	10		10		10		ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		40		50		60	ns
$t_{OH}^{[7]}$	Output Hold from Address Change (Latched Mode)	0		0		0		ns
t_{PWA}	ALE Pulse Width	10		20		30		ns
t_{CESC}	Chip Enable Set-up to Clock Rise	10		10		10		ns
t_{CESL}	Chip Enable Set-up to Latch Close (Latch Mode)	10		10		10		ns
t_{LV}	Output Valid from ALE Active (Latched Mode)		40		50		60	ns

Notes:

- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- t_{AA} and t_{OH} apply only when the latched mode is selected.

Architecture Configuration Bits

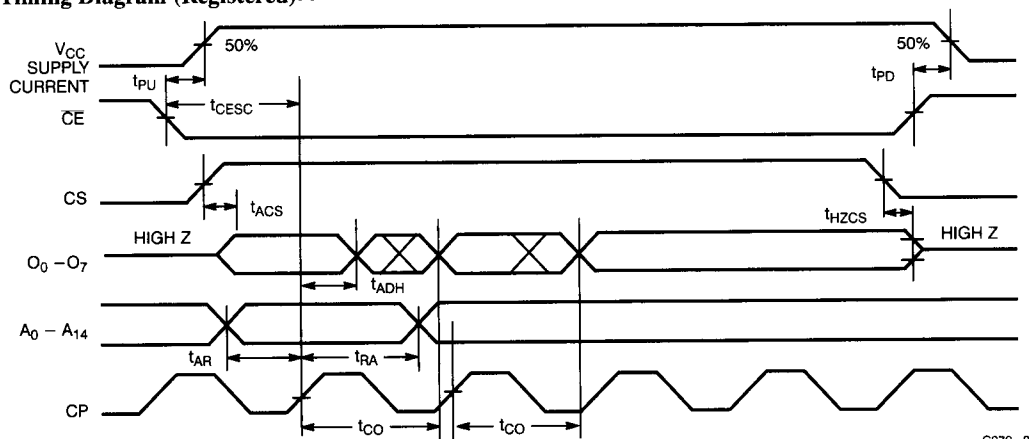
Architecture Bit	Architecture Verify D ₇ – D ₀		Function
ALE	D ₁	0 = DEFAULT	Input Registered
		1 = PGMED	Input Latched
ALEP	D ₂	0 = DEFAULT	ALE = Active HIGH
		1 = PGMED	ALE = Active LOW

Bit Map

Programmer Address (Hex.)	RAM Data
0000	Data
⋮	⋮
7FFF	Data
8000	Control Byte

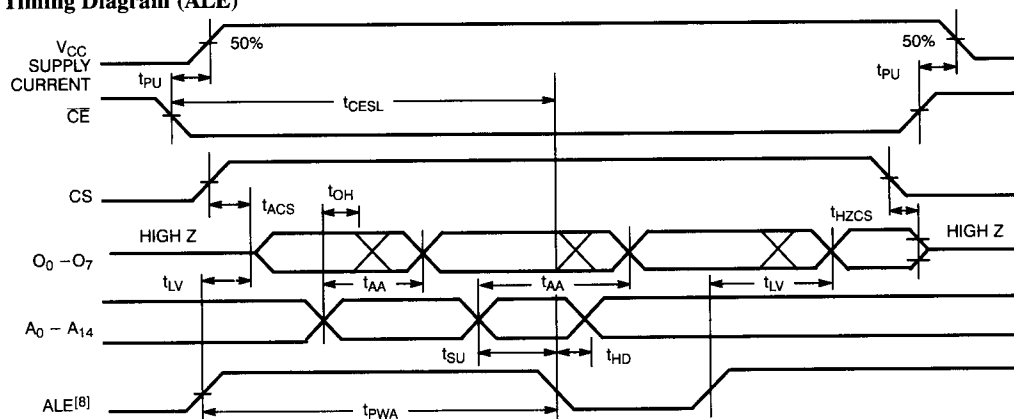
Architecture Byte (8000)
D₇ D₀
C₇ C₆ C₅ C₄ C₃ C₂ C₁ C₀

Timing Diagram (Registered)^[8]



C279–8

Timing Diagram (ALE)



C279–9

Note:

8. ALE is shown with positive polarity.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please

see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Pin Function ^[9]					
	Read or Output Disable	A ₁₄ – A ₀	CE	CS	CP/ALE	O ₇ – O ₀
	Other	A ₁₄ – A ₀	VFY	PGM	V _{PP}	D ₇ – D ₀
Read		A ₁₄ – A ₀	V _{IL}	V _{IH}	V _{IL}	O ₇ – O ₀
Output Disable		A ₁₄ – A ₀	V _{IH}	X	X	High Z
Program		A ₁₄ – A ₀	V _{IHP}	V _{ILP}	V _{PP}	D ₇ – D ₀
Program Verify		A ₁₄ – A ₀	V _{ILP}	V _{IHP} /V _{ILP}	V _{PP}	O ₇ – O ₀
Program Inhibit		A ₁₄ – A ₀	V _{IHP}	V _{IHP}	V _{PP}	High Z
Blank Check		A ₁₄ – A ₀	V _{ILP}	V _{IHP} /V _{ILP}	V _{PP}	O ₇ – O ₀

Note:

9. X = "don't care" but not to exceed V_{CC} ±5%.

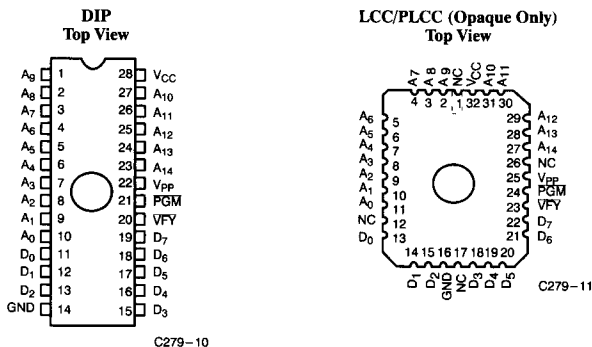
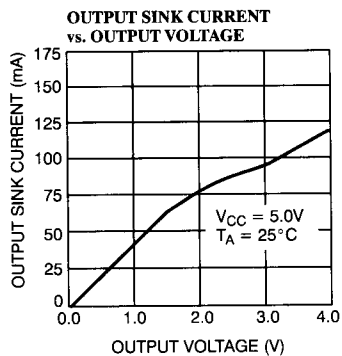
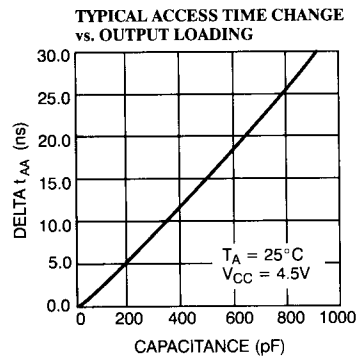
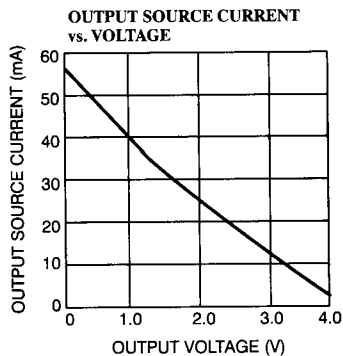
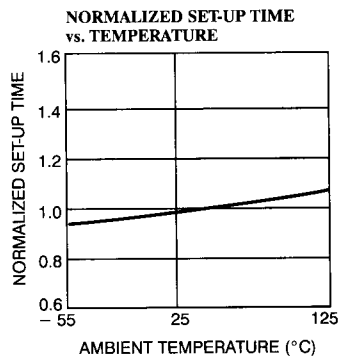
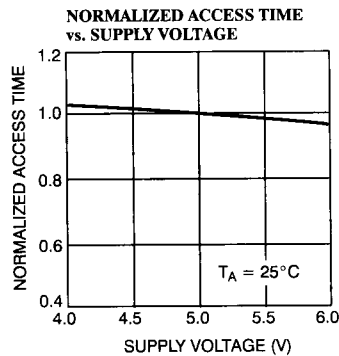
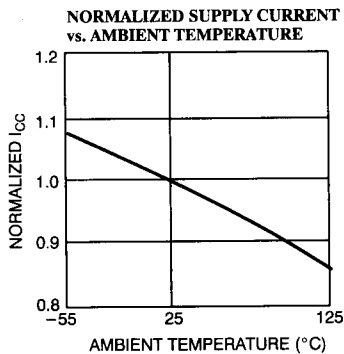
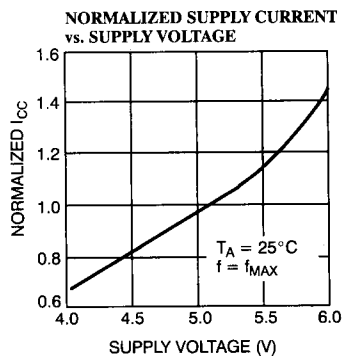


Figure 1. Programming Pinouts

Typical DC and AC Characteristics



Ordering Information^[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
35	CY7C279-35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C279-35WC	W22	28-Lead (300-Mil) Windowed CerDIP	
45	CY7C279-45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C279-45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C279-45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
55	CY7C279-55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C279-55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C279-55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military

Note:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AR}	7, 8, 9, 10, 11
t _{RA}	7, 8, 9, 10, 11
t _{DHA}	7, 8, 9, 10, 11

Document #: 38-00246