

High-Speed Quad-MOSFET Driver

Features

- 6 ns Rise and Fall Time
- 2A Peak Output Source and Sink Currents
- 1.8V to 5V Input CMOS Compatible
- Smart Logic Threshold
- Low-jitter Design
- Four Matched Channels
- Drives Two P-channel and Two N-channel MOSFETs
- Outputs can Swing below Ground
- Built-in Level Translator for Negative Gate Bias
- User-defined damping for Return-to-zero Application
- Low-inductance Quad-flat No-lead Package
- High-performance Thermally Enhanced Package

Applications

- Ultrasound PN Code Transmitter
- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-destructive Testing
- High-speed Level Translator
- High-voltage Bipolar Pulser

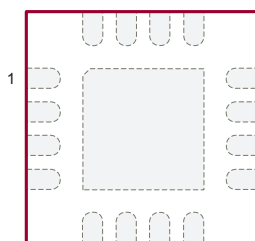
General Description

The MD1812 is a high-speed quad-MOSFET driver designed to drive two P-channel and two N-channel high-voltage MOSFETs for medical ultrasound applications and other applications requiring a high-output current for a capacitive load. The input stage of the MD1812 is a high-speed level translator that is able to operate from logic input signals of 1.8V to 5V amplitude. An adaptive threshold circuit is used to set the level translator switch threshold to the average of the input logic 0 and logic 1 levels. The level translator uses a proprietary circuit which provides DC coupling together with high-speed operation.

The output stage of the MD1812 has separate power connections, enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V and -5V, and the output L and H levels may be varied anywhere over the range of -5V to +5V. The output stage is capable of peak currents of up to $\pm 2A$, depending on the supply voltages used and load capacitance present. The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Second, when OE is low, the outputs are disabled, with the A and C outputs high and the B and D outputs low. This assists in properly pre-charging the AC coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS transistor pair. A built-in level shifter provides PMOS gate negative bias drive. This enables the user-defined damping control to generate return-to-zero bipolar output pulses.

Package Type

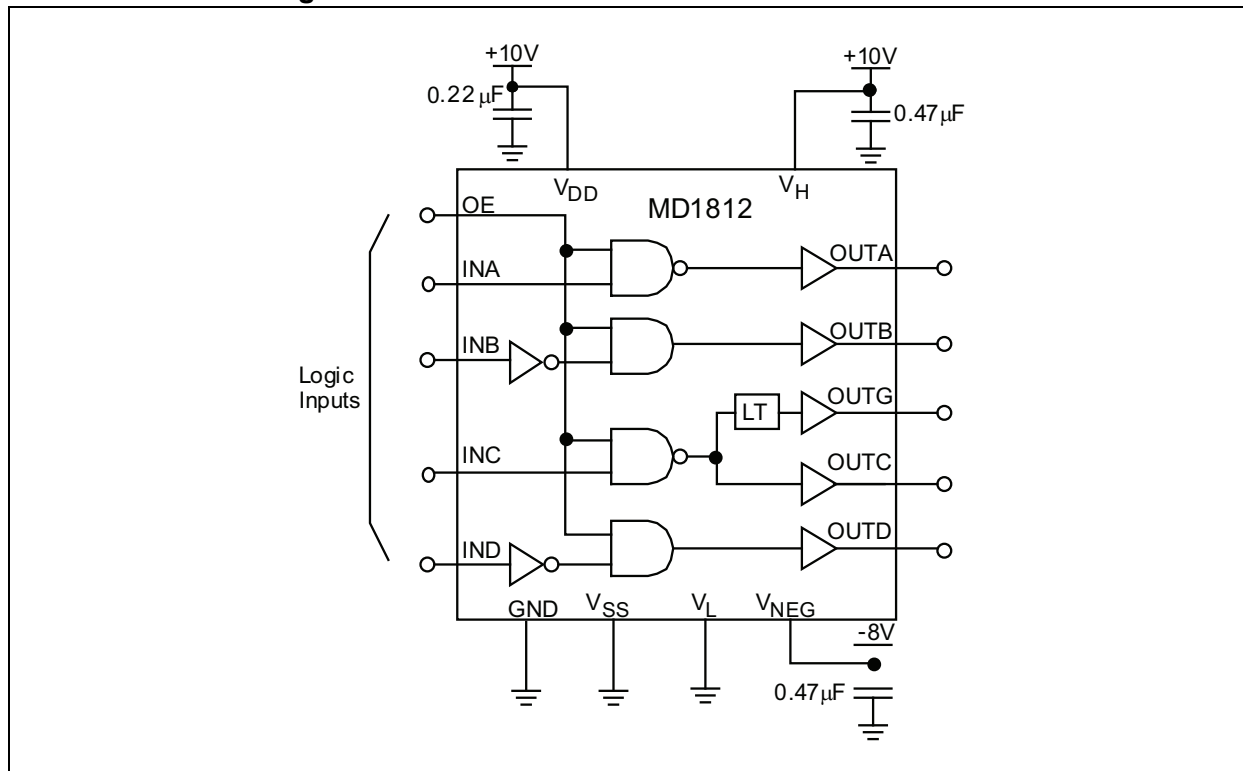
16-lead QFN
(Top view)



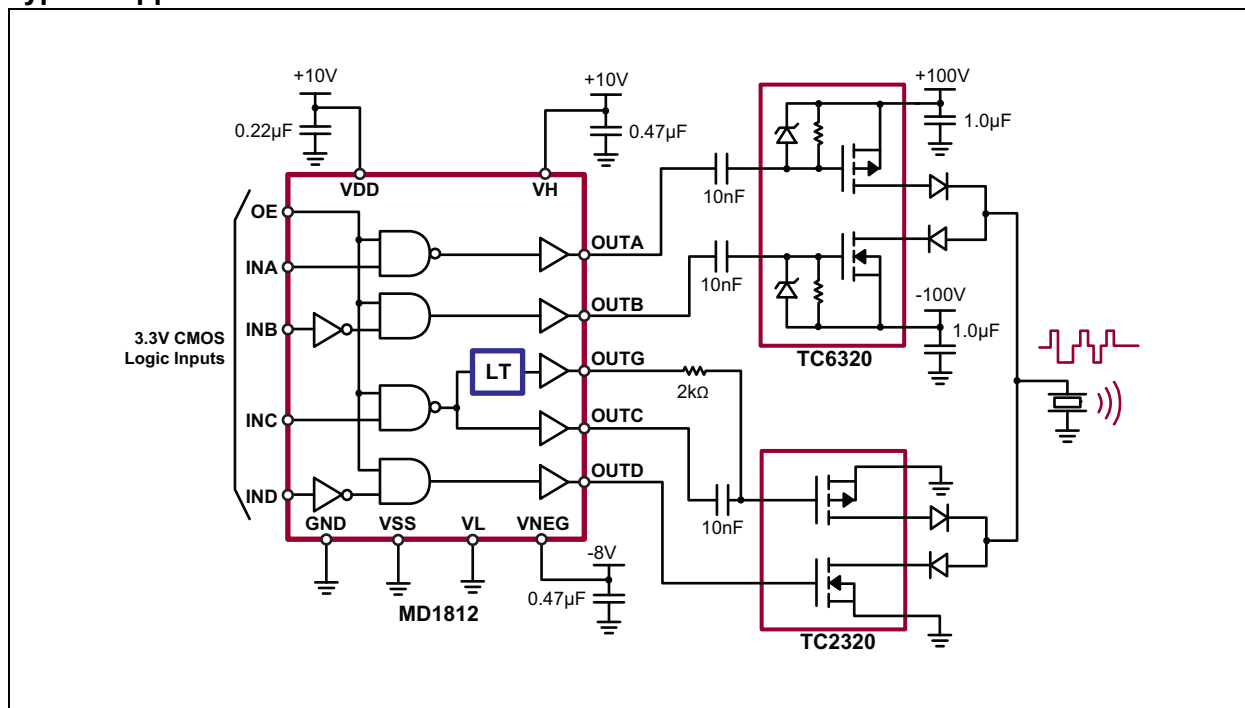
See [Table 2-1](#) for pin information.

MD1812

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, $V_{DD}-V_{SS}$	–0.5V to +13.5V
Output High Supply Voltage, V_H	$V_L-0.5V$ to $V_{DD}+0.5V$
Output Low Supply Voltage, V_L	$V_{SS}-0.5V$ to $V_H+0.5V$
Low-side Supply Voltage, V_{SS}	–7V to +0.5V
Supply Voltage, $V_{DD}-V_{NEG}$	–0.5V to +20V
Negative Supply Voltage, $V_{NEG}-V_{SS}$	$V_{SS}-10V$ to $V_{SS}+0.5V$
Logic Input Levels	$V_{SS}-0.5V$ to GND +7V
Operating Junction Temperature, T_J	–25°C to +125°C
Storage Temperature, T_S	–65°C to +150°C
Power Dissipation	2.2W
ESD Rating (Note 1)	ESD Sensitive

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Device is ESD sensitive. Handling precautions are recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD} = 12V$, $V_L = V_{SS} = \text{GND} = 0V$, $V_{NEG} = -6V$, $V_{OE} = 3.3V$ and $T_J = 25^{\circ}\text{C}$							
Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage		$V_{DD}-V_{SS}$	4.5	—	13	V	$2.5V \leq V_{DD} \leq 13V$
Supply Voltage		$V_{DD}-V_{NEG}$	—	—	18	V	
Low-side Supply Voltage		V_{SS}	-5.5	—	0	V	
Output High Supply Voltage		V_H	$V_{SS} + 2$	—	V_{DD}	V	
Output Low Supply Voltage		V_L	V_{SS}	—	$\frac{V_{DD}-2}{2}$	V	
Negative Supply Voltage		V_{NEG}	-9	—	$V_{SS}-2$	V	May be connected to V_{SS} if OUTG is not used
V_{DD} Quiescent Current		I_{DDQ}	—	1.5	—	mA	No input transitions, $OE = 1$
V_H Quiescent Current		I_{HQ}	—	—	10	μA	
V_{NEG} Quiescent Current		I_{NEGQ}	—	150	—	μA	
V_{DD} Average Current		I_{DD}	—	7	—	mA	One channel on at 5 MHz, no load
V_H Average Current		I_H	—	22	—	mA	
V_{NEG} Average Current		I_{NEG}	—	1.5	—	mA	
Input Logic Voltage High		V_{IH}	$V_{OE}-0.3$	—	5	V	For logic inputs INA, INB, INC and IND
Input Logic Voltage Low		V_{IL}	0	—	0.3	V	
Input Logic Current High		I_{IH}	—	—	1	μA	
Input Logic Current Low		I_{IL}	—	—	1	μA	
OE Input Logic Voltage High		V_{IH}	1.7	—	5	V	For logic input OE
OE Input Logic Voltage Low		V_{IL}	0	—	0.3	V	
OE Input Resistance		R_{IN}	10	20	30	k Ω	
Logic Input Capacitance		C_{IN}	—	5	10	pF	
Output Sink Resistance	OUTA-D	R_{SINK}	—	—	12.5	Ω	$I_{SINK} = 50 \text{ mA}$
	OUTG		—	—	200		$I_{SINK} = 5 \text{ mA}$
Output Source Resistance	OUTA-D	R_{SOURCE}	—	—	12.5	Ω	$I_{SOURCE} = 50 \text{ mA}$
	OUTG		—	—	200		$I_{SOURCE} = 5 \text{ mA}$

DC ELECTRICAL CHARACTERISTICS (CONTINUED)**Electrical Specifications:** $V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{NEG} = -6V$, $V_{OE} = 3.3V$ and $T_J = 25^\circ C$

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Peak Output Sink Current	I_{SINK}	—	2	—	A	
Peak Output Source Current	I_{SOURCE}	—	2	—	A	

AC ELECTRICAL CHARACTERISTICS**Electrical Specifications:** $V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{NEG} = -6V$, $V_{OE} = 3.3V$ and $T_A = 25^\circ C$

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input or OE Rise and Fall Time	t_{irf}	—	—	10	ns	Logic input edge speed requirement
Propagation Delay INC to OUTG	t_{PCG}	—	40	—	ns	10 MΩ load to GND
Propagation Delay when Output is from Low to High for OUTA-D	t_{PLH}	—	7	—	ns	$C_{LOAD} = 1000$ pF, input signal rise/fall time of 2 ns
Propagation Delay when Output is from High to Low for OUTA-D	t_{PHL}	—	7	—	ns	
Output Rise Time	t_r	—	6	—	ns	
Output Fall Time	t_f	—	6	—	ns	
Rise and Fall Time Matching	$ t_r - t_f $	—	1	—	ns	For each channel
Propagation Low-to-high and High-to-low Matching	$ t_{PLH} - t_{PHL} $	—	1	—	ns	
Propagation Delay Matching	Δt_{dm}	—	±2	—	ns	Device-to-device delay match
Output Enable Time	t_{OE_ON}	—	200	—	ns	
	t_{OE_OFF}	—	9	—	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	-25	—	125	°C	
Storage Temperature	T_S	-65	—	150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead QFN	θ_{JA}	—	25	—	°C/W	Note 1

Note 1: 1 oz. 4-layer 3" x 4" PCB

Timing Diagram

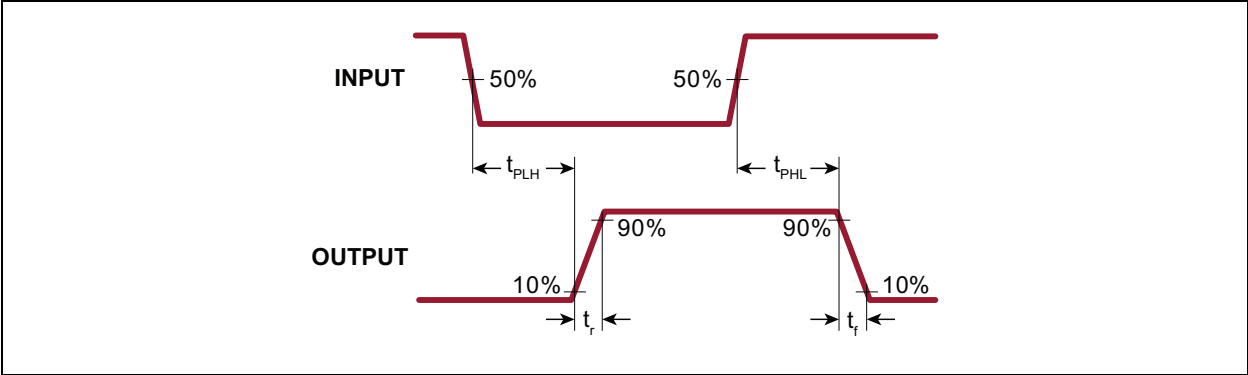


TABLE 1-1: TRUTH FUNCTION TABLE

Logic Inputs			Outputs		
OE	INA	INB	OUTA		OUTB
H	L	L	V_H		V_H
H	L	H	V_H		V_L
H	H	L	V_L		V_H
H	H	H	V_L		V_L
L	X	X	V_H		V_L
OE	INC	IND	OUTC	OUTG	OUTD
H	L	L	V_H	V_{SS}	V_H
H	L	H	V_H	V_{SS}	V_L
H	H	L	V_L	V_{NEG}	V_H
H	H	H	V_L	V_{NEG}	V_L
L	X	X	V_H	V_{SS}	V_L

2.0 PIN DESCRIPTION

The details on the pins of MD1812 are listed on [Table 2-1](#). See [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	INB	Logic input. Controls OUTB when OE is high.
2	VL	Supply voltage for N-channel output stage
3	GND	Device ground
4	VNEG	Supply voltage for the auxiliary gate drive (Note 1)
5	INC	Logic input. Controls OUTC when OE is high.
6	IND	Logic input. Controls OUTD when OE is high.
7	VSS	Supply voltage for low-side analog, level shifter and gate drive circuit
8	OUTD	Output driver
9	OUTC	Output driver
10	OUTG	Auxiliary output driver
11	VH	Supply voltage for P-channel output stage
12	OUTB	Output driver
13	OUTA	Output driver
14	VDD	Supply voltage for high-side analog, level shifter and gate drive circuit
15	INA	Logic input. Controls OUTA when OE is high.
16	OE	Output enable logic input

Note 1: Thermal pad and pin 4, VNEG must be connected externally.

3.0 APPLICATION INFORMATION

For proper operation of the MD1812, low-inductance bypass capacitors should be used on the various supply pins. The GND input pin should be connected to the logic ground. The INA, INB, INC, IND and OE pins should be connected to a logic source with a swing of GND to V_{CC} , where V_{CC} is 1.8V to 5V. When the input logic(s) is high, the output(s) will swing to V_L , and when the input(s) logic is low, the output(s) will swing to V_H . All inputs must be kept low until the device is powered up. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1812 is capable of operating up to 100 MHz, with the primary speed limitation being the loading effect of the load capacitance. Because of this speed and the high transient currents due to the capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the V_{SS} and V_L pins should have a low-inductance bypass capacitor to GND and supply power connections. If these voltages are not zero, they need bypass capacitors in a manner similar to the positive power supplies. The power connection V_{DD} should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

Output drivers OUTA and OUTC drive the gate of an external P-channel MOSFET, while output drivers OUTB and OUTD drive the gate of an external N-channel MOSFET, and they all swing from V_H to V_L . The auxiliary output drive, OUTG, swings from V_{SS} to V_{NEG} and drives the gate of an external P-channel MOSFET through a 2 k Ω series resistor.

The voltages of V_H and V_L decide the output logic levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with a suitable bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1 μ F may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead going to the capacitor. Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface-mount components are highly recommended. Since the output impedance of this driver is very low, in some cases, it may be desirable to add a small series resistor in series with the output signal to obtain better waveform transitions at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

The OE pin sets the threshold level of logic for inputs ($V_{OE} + V_{GND}$)/2. When OE is low, OUTA and OUTC are at V_H , while OUTB and OUTD are at V_L . Auxiliary output OUTG is at V_{SS} , regardless of the inputs INA and INB.

Ensure that parasitic couplings are minimized from the driver output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupled voltages may cause problems. The use of a solid ground plane and good power and signal layout practices will prevent this problem. Make sure that the circulating ground return current from a capacitive load will not react with common inductance and cause noise voltages in the input logic circuitry. Best timing performance is obtained for OUTC when the voltage of $V_{SS}-V_{NEG} = V_H-V_L$.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-lead QFN

Example

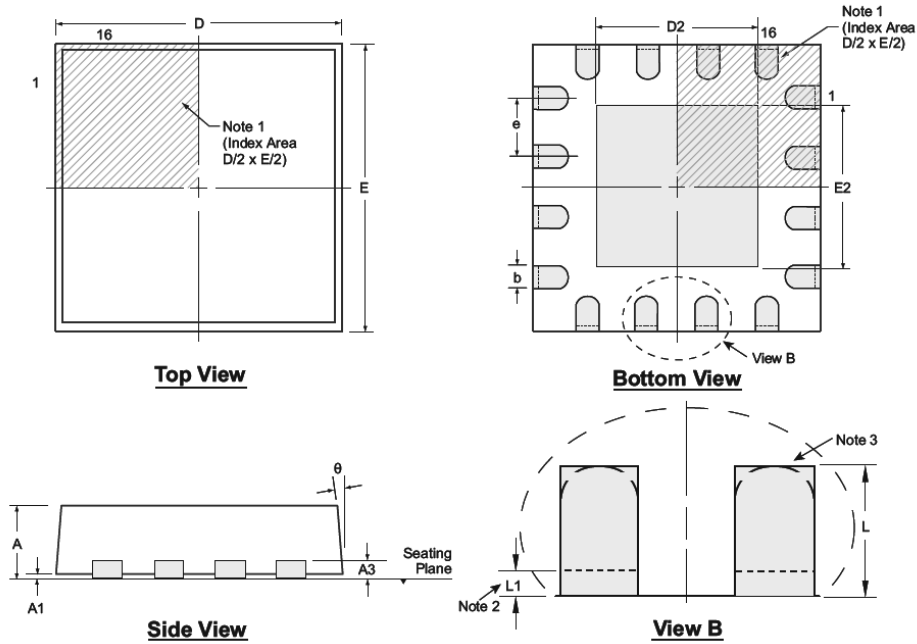
XXXXXX
XXXXXX
(e3)YYWW
NNN

MD
1812K6
(e3)1710
265

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.		

16-Lead QFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 0.65mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85*	2.50	3.85*	2.50	0.65 BSC	0.30 [†]	0.00	0°
	NOM	0.90	0.02		0.30	4.00	2.65	4.00	2.65		0.40 [†]	-	-
	MAX	1.00	0.05		0.35	4.15*	2.80	4.15*	2.80		0.50 [†]	0.15	14°

JEDEC Registration MO-220, Variation VGGC-2, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (May 2017)

- Converted Supertex Doc# DSFP-MD1812 to Microchip DS20005746A
- Changed the package marking format
- Changed the quantity of the 16-lead QFN K6 package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

MD1812

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options			Environmental		Media Type
Device:	MD1812	=		High-Speed Quad-MOSFET Driver		
Package:	K6	=		16-lead QFN		
Environmental:	G	=		Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=		3300/Reel for a K6 Package		

Example:

a) MD1812K6-G: High-Speed Quad-MOSFET Driver, 16-lead QFN, 3300/Reel

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, LINK MD, maxStylus, maxTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, All Rights Reserved.
ISBN: 978-1-5224-1699-9

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820