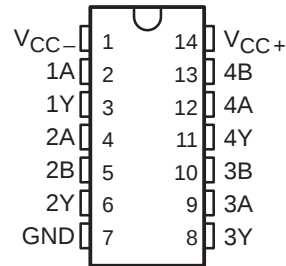


- Bi-MOS Technology With TTL and CMOS Compatibility
- Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Quiescent Current . . . 95 μ A Typ
 $V_{CC\pm} = \pm 12$ V
- Current-Limited Outputs . . . 10 mA Typ
- CMOS- and TTL-Compatible Inputs
- On-Chip Slew Rate Limited to 30 V/ μ s max
- Flexible Supply Voltage Range
- Characterized at $V_{CC\pm}$ of ± 4.5 V and ± 15 V
- Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88

D, DB[†], OR N PACKAGE
(TOP VIEW)



[†] The DB package is only available left-end taped and reeled, i.e., order device SN75C188DBLE.

description

The SN75C188 is a monolithic, low-power, quadruple line driver that interfaces data terminal equipment with data communications equipment. This device is designed to conform to ANSI Standard EIA/TIA-232-E.

An external diode in series with each supply-voltage terminal is needed to protect the SN75C188 under certain fault conditions to comply with EIA/TIA-232-E.

The SN75C188 is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER 1

B	Y
H	L
L	H

DRIVERS 2 – 4

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = don't care



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

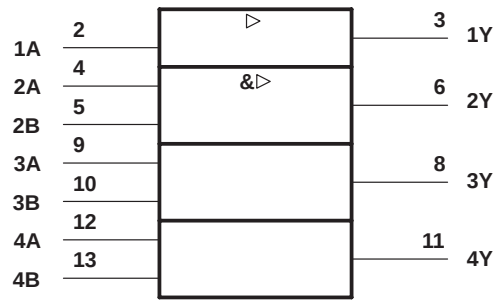
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SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

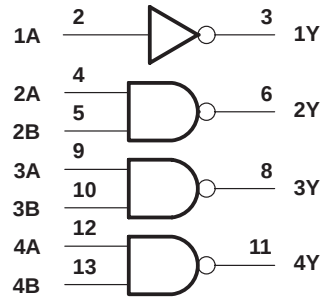
SLLS033F – JANUARY 1988 – REVISED MARCH 1997

logic symbol†



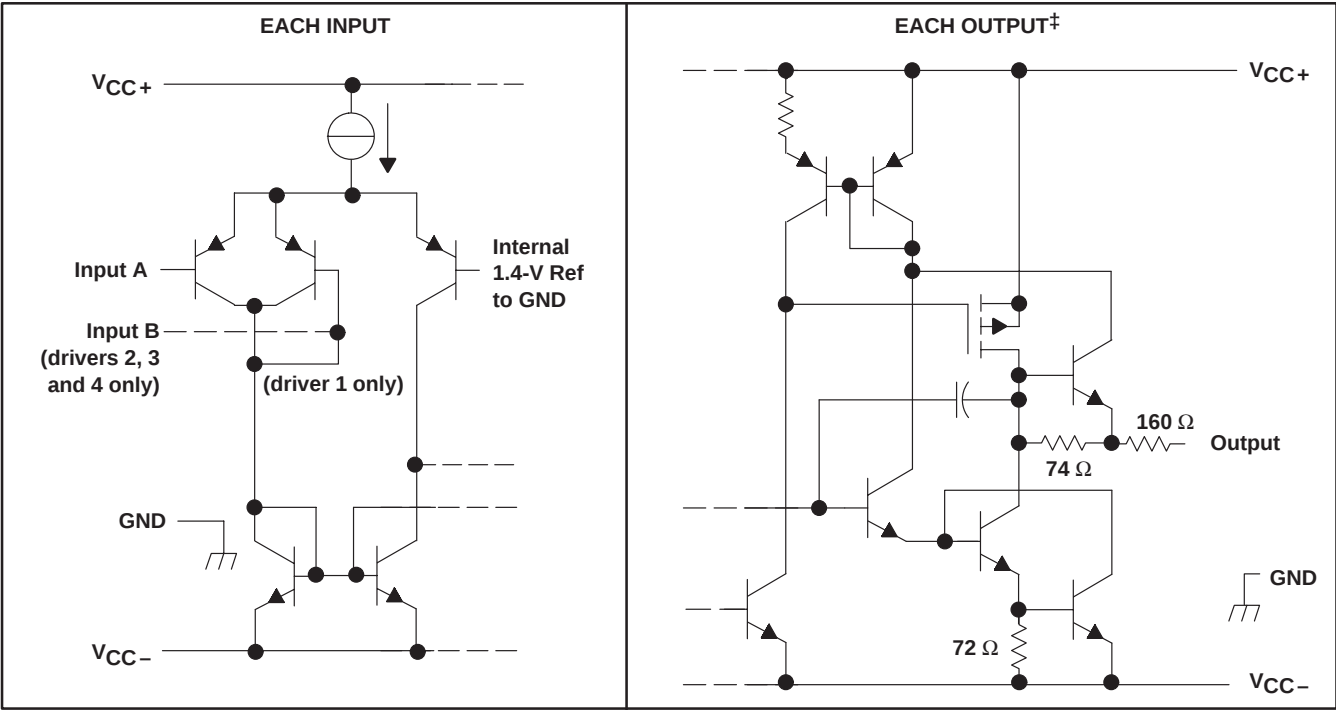
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



positive logic
 $Y = \overline{A}$ (driver 1)
 $Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 through 4)

schematics of inputs and outputs



‡ All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	15 V
Supply voltage, V_{CC-} (see Note 1)	–15 V
Input voltage range, V_I	V_{CC-} to V_{CC+}
Output voltage range, V_O	$V_{CC-} - 6\text{ V}$ to $V_{CC+} + 6\text{ V}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
DB	525 mW	4.2 mW/°C	336 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	–4.5	–12	–15	V
Input voltage, V_I	$V_{CC-} + 2$		V_{CC+}	V
High-level Input voltage, V_{IH}	2			V
Low-level Input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

SN75C188

QUADRUPLE LOW-POWER LINE DRIVERS

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electrical characteristics over operating free-air temperature range, $V_{CC+} = 12\text{ V}$, $V_{CC-} = -12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT
V _{OH}	High-level output voltage	V _{IL} = 0.8 V,	R _L = 3 kΩ	V _{CC+} = 5 V, V _{CC−} = −5 V	4			V
				V _{CC+} = 12 V, V _{CC−} = −12 V	10			
V _{OL}	Low-level output voltage (see Note 2)	V _{IH} = 2 V,	R _L = 3 kΩ	V _{CC+} = 5 V, V _{CC−} = −5 V	−4			V
				V _{CC+} = 12 V, V _{CC−} = −12 V	−10			
I _{IH}	High-level input current	V _I = 5 V			10			μA
I _{IL}	Low-level input current	V _I = 0			−10			μA
I _{OS(H)}	High-level short-circuit output current [‡]	V _I = 0.8 V,	V _O = 0 or V _{CC−}		−5.5	−10	−19.5	mA
I _{OS(L)}	Low-level short-circuit output current [‡]	V _I = 2 V,	V _O = 0 or V _{CC+}		5.5	10	19.5	mA
r _O	Output resistance, power off	V _{CC+} = 0,	V _{CC−} = 0,	V _I = −2 V to 2 V	300			Ω
I _{CC+}	Supply current from V _{CC+}	V _{CC+} = 5 V, No load	V _{CC−} = −5 V,	All inputs at 2 V or 0.8 V	90			μA
		V _{CC+} = 12 V, No load	V _{CC−} = −12 V,		95			
I _{CC−}	Supply current from V _{CC−}	V _{CC+} = 5 V, No load	V _{CC−} = −5 V,	All inputs at 2 V or 0.8 V	−90			μA
		V _{CC+} = 12 V, No load	V _{CC−} = −12		−95			

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only; e.g., if -4 V is a maximum, the typical value is a more negative voltage.

switching characteristics, $V_{CC+} = 12\text{ V}$, $V_{CC-} = -12\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
t _{PLH}	Propagation delay time, low- to high-level output [§]	R _L = 3 kΩ, See Figure 1	C _L = 15 pF,			3	μs		
t _{PHL}	Propagation delay time, high- to low-level output [§]					3.5	μs		
t _{TLH}	Transition time, low- to high-level output [¶]			0.53	3.2	μs			
t _{THL}	Transition time, high- to low-level output [¶]			0.53	3.2	μs			
t _{TLH}	Transition time, low- to high-level output [#]	R _L = 3 kΩ to 7 kΩ, See Figure 1	C _L = 2500 pF,			1.5	μs		
t _{THL}	Transition time, high- to low-level output [#]					1.5	μs		
SR	Output slew rate [§]	R _L = 3 kΩ to 7 kΩ, C _L = 15 pF				6	15	30	V/μs

[§] Measured at the 50% level

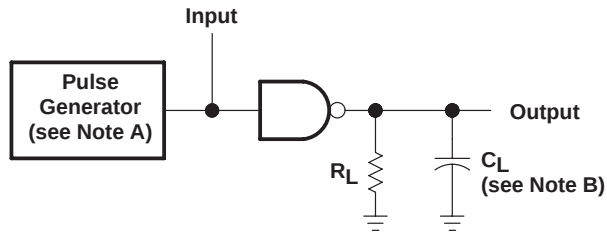
[¶] Measured between the 10% and 90% points on the output waveform

[#] Measured between the 3-V and -3 V points on the output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low

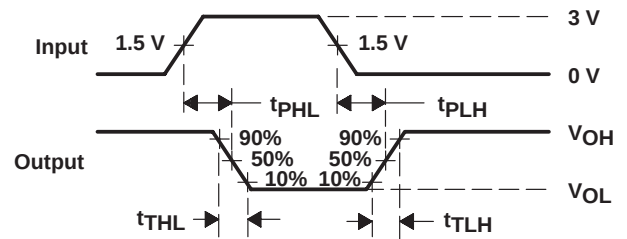


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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

SN75C188

QUADRUPLE LOW-POWER LINE DRIVERS

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TYPICAL CHARACTERISTICS

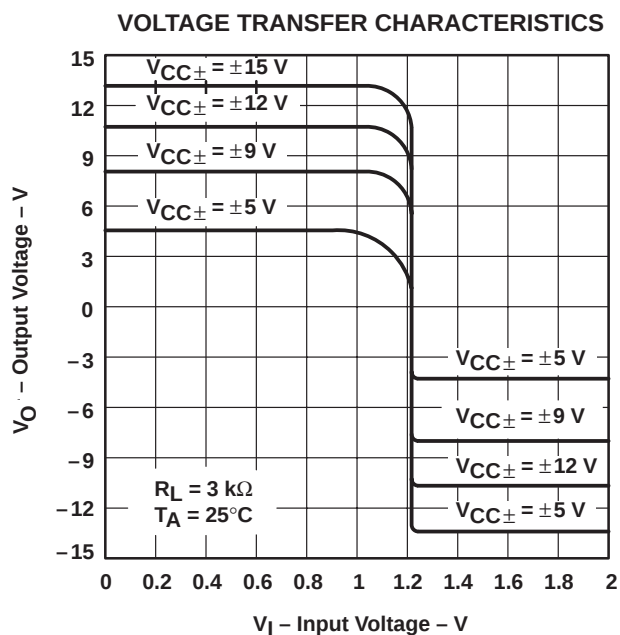


Figure 2

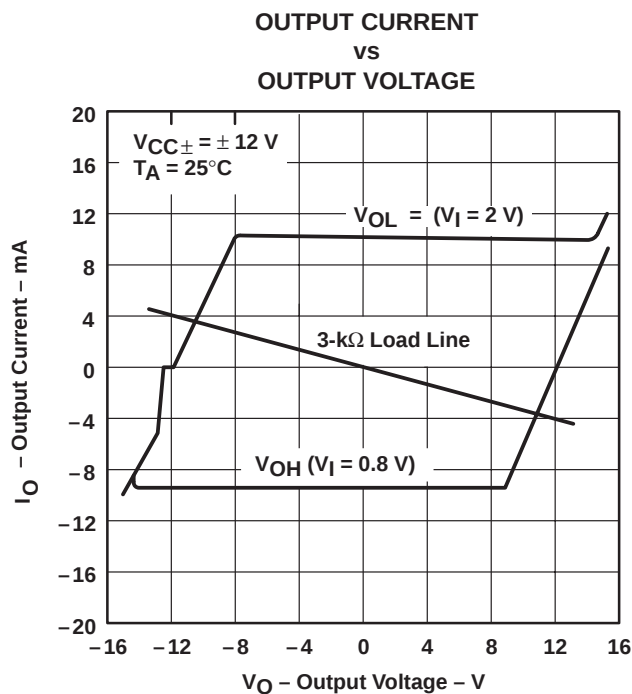


Figure 3

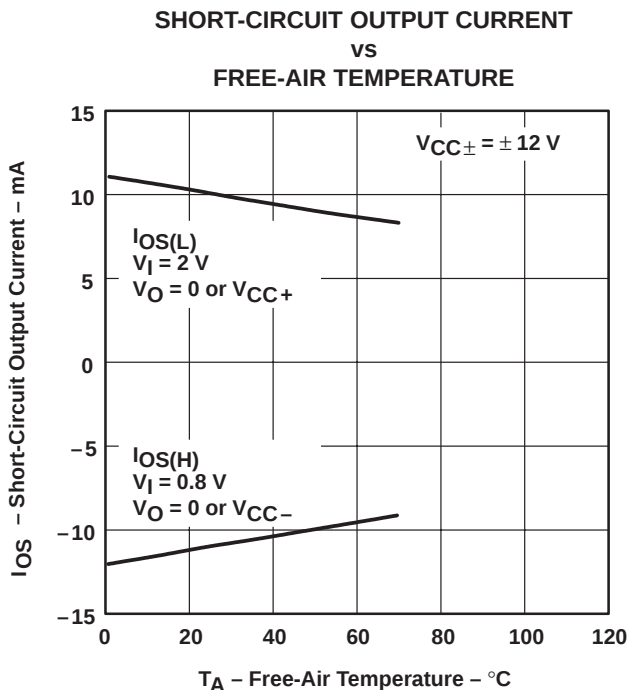


Figure 4

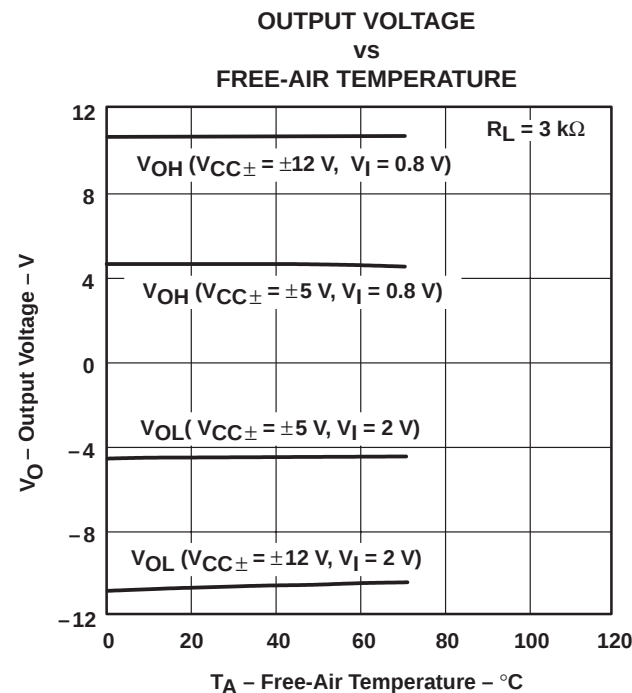
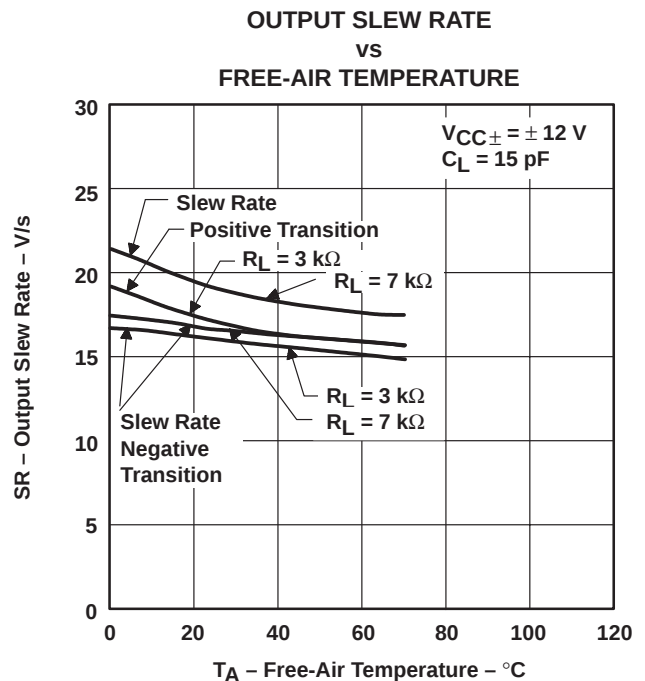
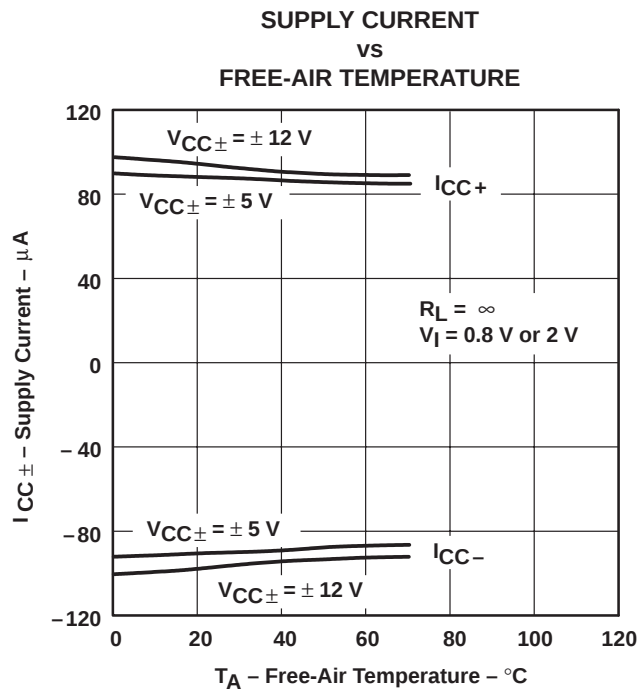
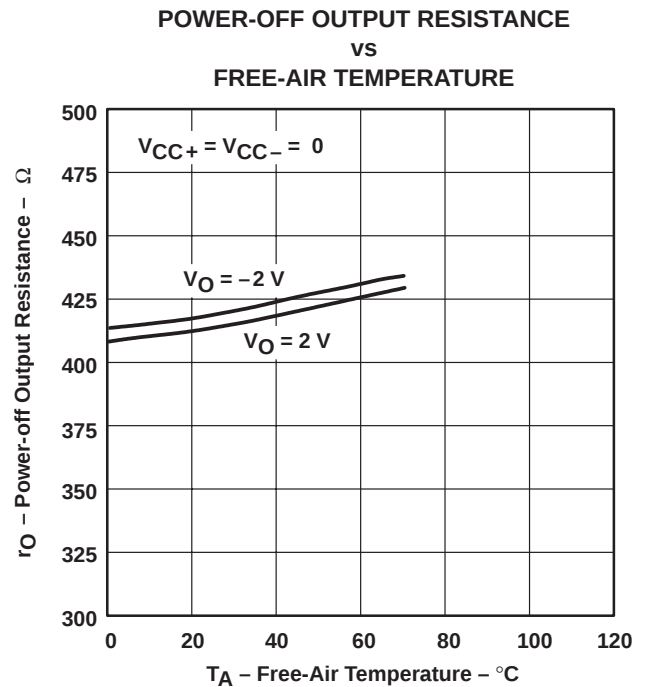
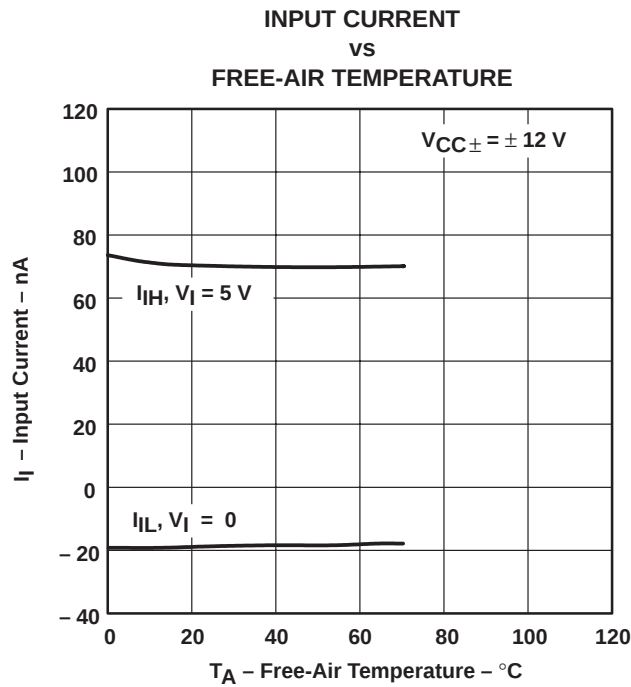


Figure 5

TYPICAL CHARACTERISTICS



SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS033F – JANUARY 1988 – REVISED MARCH 1997

TYPICAL CHARACTERISTICS

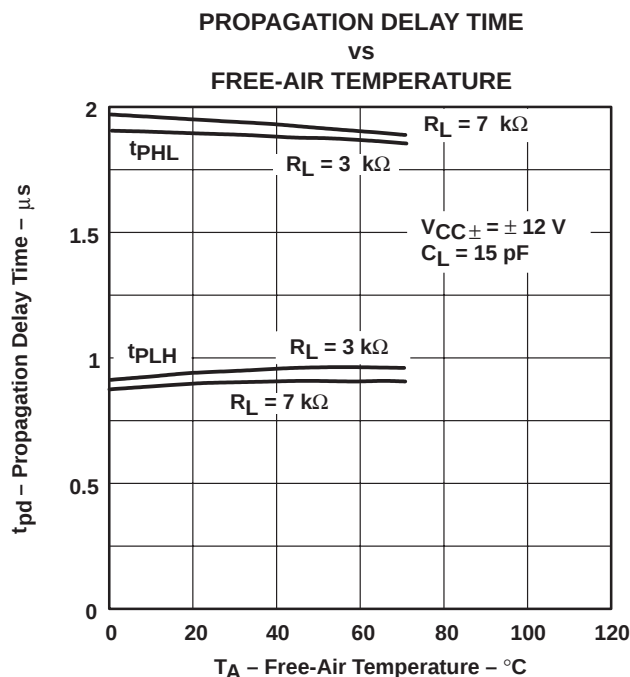


Figure 10

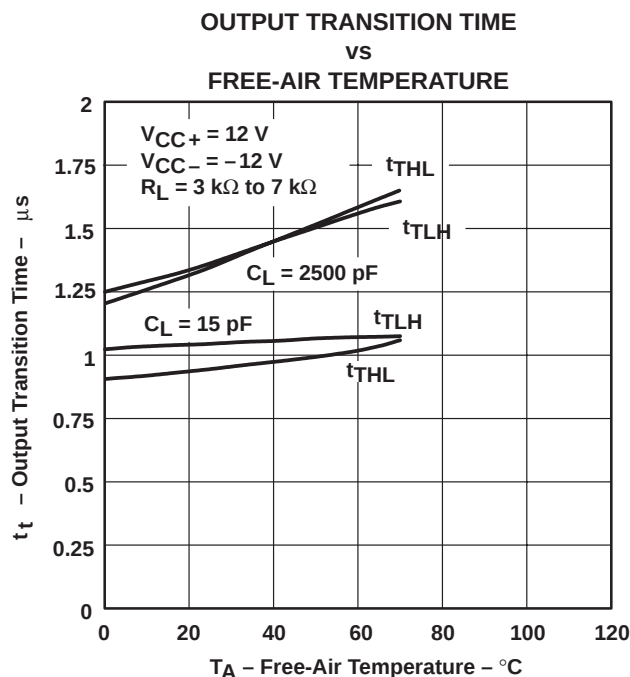


Figure 11

APPLICATION INFORMATION

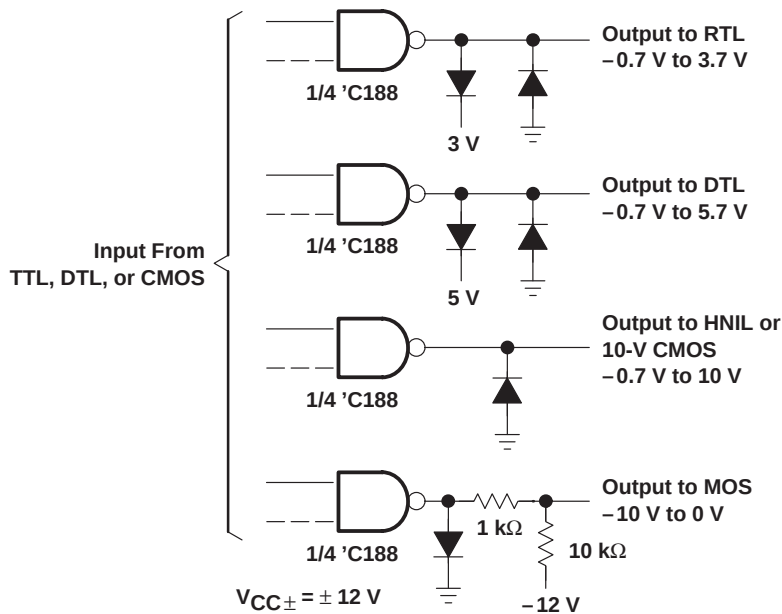
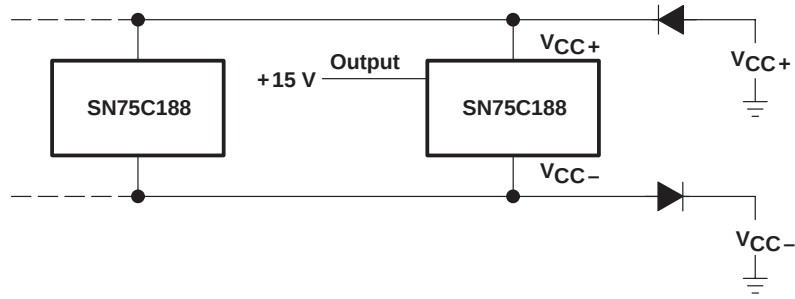


Figure 12. Logic Translator Applications

APPLICATION INFORMATION



NOTE A: External diodes placed in series with the V_{CC+} and V_{CC-} leads protect the SN75C188 in the fault condition where the device outputs are shorted to ± 15 V and the power supplies are at low voltage and provide low-impedance paths to GND.

Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA/TIA-232-E

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75C188D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188
SN75C188D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188
SN75C188DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA188
SN75C188DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA188
SN75C188DE4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188
SN75C188DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188
SN75C188DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188
SN75C188DRE4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188
SN75C188N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C188N
SN75C188N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C188N
SN75C188NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C188
SN75C188NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C188

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C188DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C188NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C188DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN75C188DR	SOIC	D	14	2500	353.0	353.0	32.0
SN75C188NSR	SOP	NS	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75C188D	D	SOIC	14	50	507	8	3940	4.32
SN75C188D	D	SOIC	14	50	506.6	8	3940	4.32
SN75C188D.A	D	SOIC	14	50	507	8	3940	4.32
SN75C188D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN75C188DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN75C188DE4	D	SOIC	14	50	507	8	3940	4.32
SN75C188N	N	PDIP	14	25	506	13.97	11230	4.32
SN75C188N.A	N	PDIP	14	25	506	13.97	11230	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

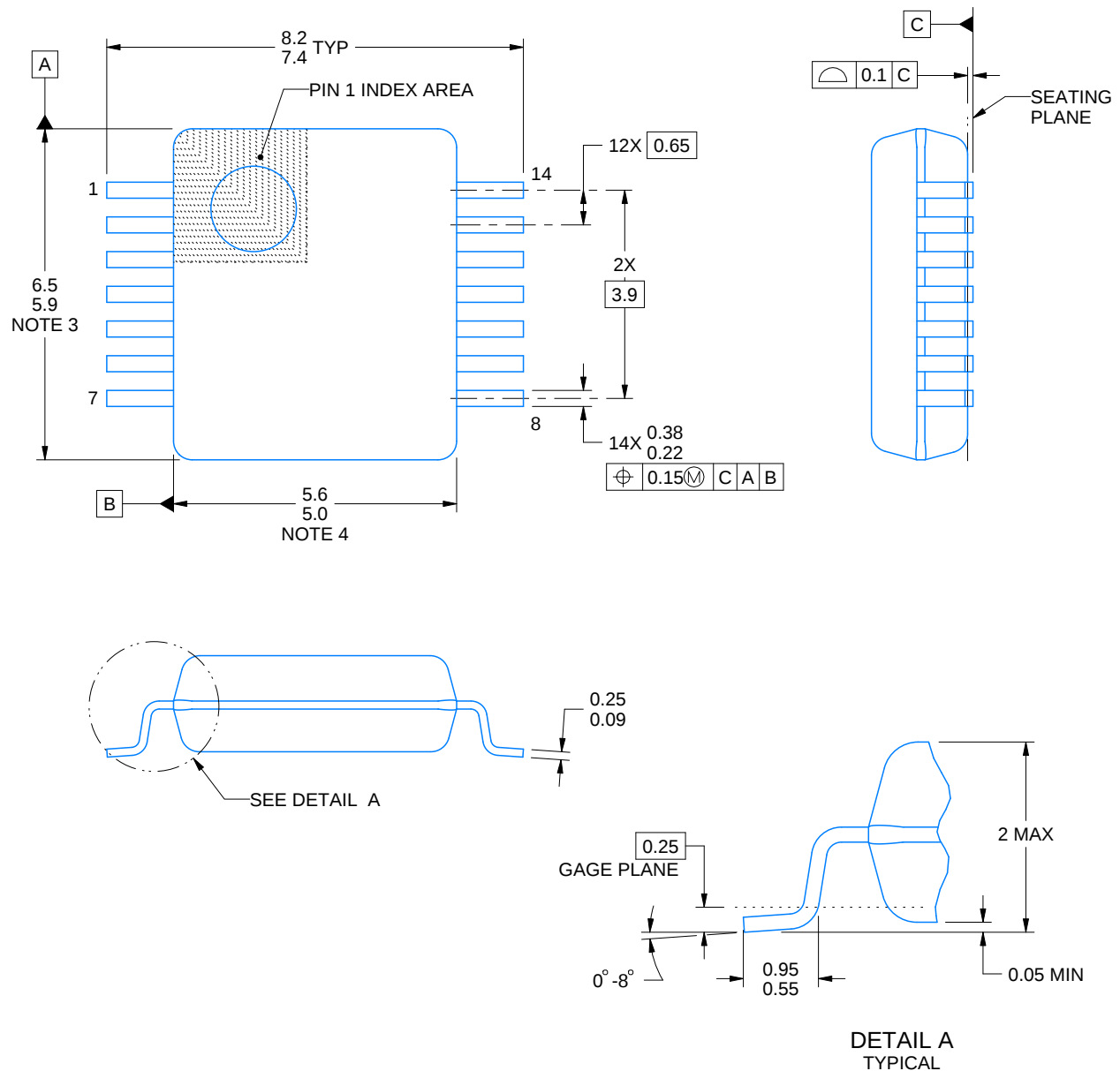
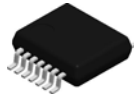
NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220762/A 05/2024

NOTES:

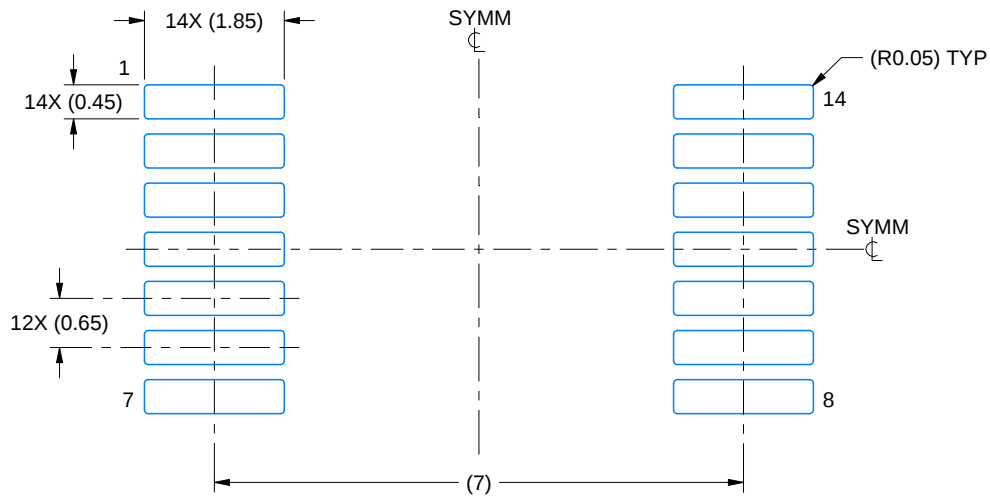
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

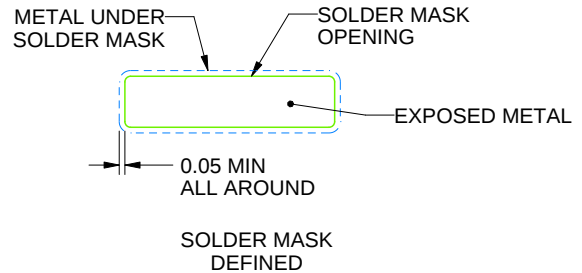
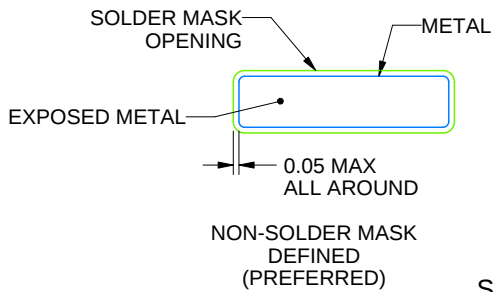
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

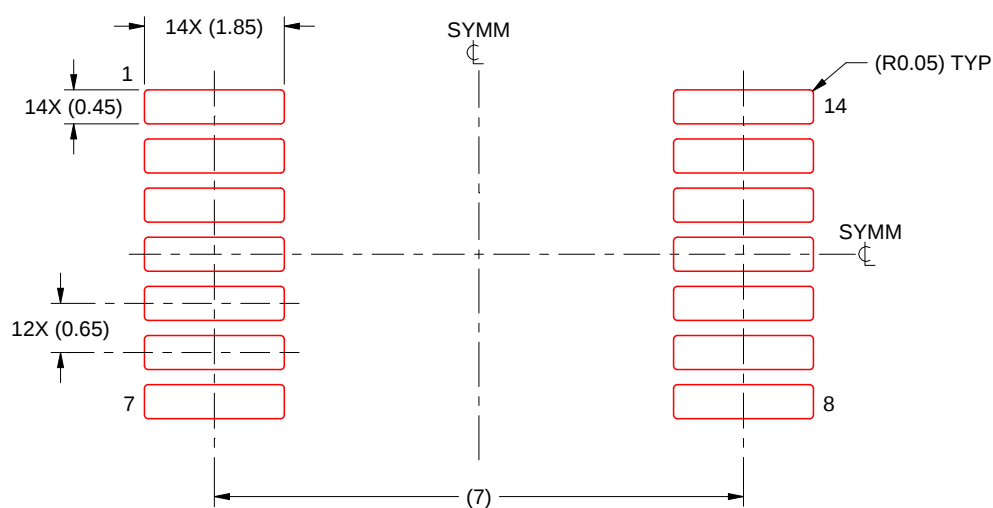
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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