

**M5M5256DFP,VP -70G,-70GI,-70XG**

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

**DESCRIPTION**

The M5M5256DFP,VP is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 poly silicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256DVP are packaged in a 28-pin thin small outline package.

**FEATURE**

Type	Access time (max)	Operating Temperature	Power supply current	
			Active (max)	Stand-by (max)
M5M5256DFP,VP -70G	70ns	0~70°C	45mA (Vcc=5.5V) 25mA (Vcc=3.6V)	20µA (Vcc=5.5V) 12µA (Vcc=3.6V)
M5M5256DFP,VP -70GI	70ns	-40~85°C		40µA (Vcc=5.5V) 24µA (Vcc=3.6V)
M5M5256DFP,VP -70XG	70ns	0~70°C		5µA (Vcc=5.5V) 2.4µA (Vcc=3.6V) 0.05µA (Vcc=3.0V Typical)

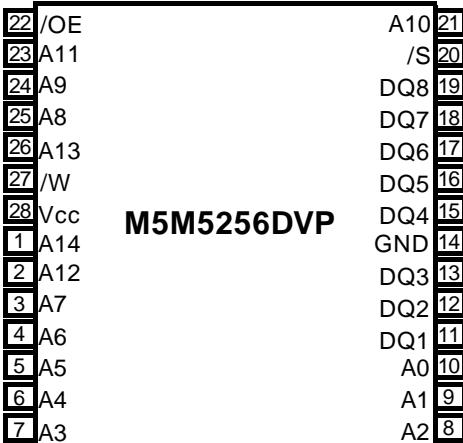
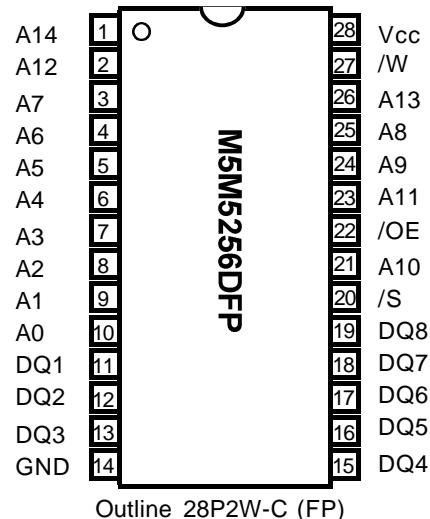
- Single 3.0~5.5V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- /OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Low stand-by current ..... 0.05µA(typ.)

**PACKAGE**

M5M5256DFP : 28 pin 450 mil SOP  
 M5M5256DVP : 28pin 8 X 13.4 mm<sup>2</sup> TSOP

**APPLICATION**

Small capacity memory units

**PIN CONFIGURATION (TOP VIEW)**

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**FUNCTION**

The operation mode of the M5M5256DFP,VP is determined by a combination of the device control inputs /S, /W and /OE. Each mode is summarized in the function table.

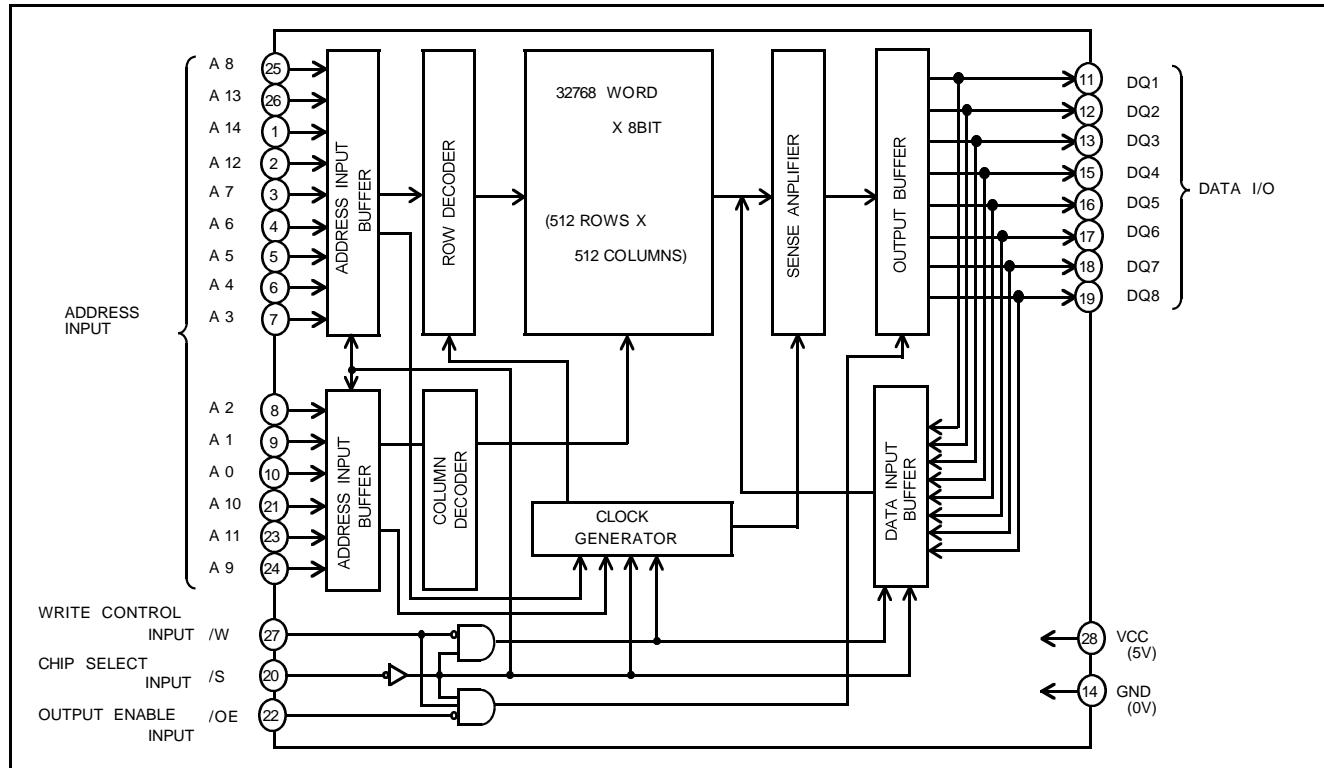
A write cycle is executed whenever the low level /W overlaps with the low level /S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

**FUNCTION TABLE**

/S	/W	/OE	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D <sub>IN</sub>	Active
L	H	L	Read	D <sub>OUT</sub>	Active
L	H	H		High-impedance	Active

Note • "H" and "L" in this table mean VIH and VIL, respectively.

• "X" in this table should be "H" or "L".

**BLOCK DIAGRAM**

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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings			Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	-0.3*~7.0			V
V <sub>i</sub>	Input voltage		-0.3*~V <sub>cc</sub> +0.3 (Max 7.0)			V
V <sub>o</sub>	Output voltage		0~V <sub>cc</sub>			V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	700		mW	
T <sub>opr</sub>	Operating temperature	-G,-XG	0~70		°C	
		-GI	-40~85			
T <sub>stg</sub>	Storage temperature		-65~150			°C

\* -3.0V in case of AC ( Pulse width &lt; 30ns )

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test conditions	Limits1 (V <sub>cc</sub> =3.3±0.3V)			Limits2 (V <sub>cc</sub> =5.0±0.5V)			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>ih</sub>	High-level input voltage		2.0		V <sub>cc</sub> +0.3	2.2		V <sub>cc</sub> +0.3	V
V <sub>il</sub>	Low-level input voltage		-0.3*		0.6	-0.3*		0.8	V
V <sub>oh1</sub>	High-level output voltage 1	I <sub>oh</sub> =-1mA I <sub>oh</sub> =-0.5mA (V <sub>cc</sub> =5.0±0.5V) (V <sub>cc</sub> =3.3±0.3V)	2.4			2.4			V
V <sub>oh2</sub>	High-level output voltage 2	I <sub>oh</sub> =-0.1mA I <sub>oh</sub> =-0.05mA (V <sub>cc</sub> =5.0±0.5V) (V <sub>cc</sub> =3.3±0.3V)	V <sub>cc</sub> -0.5			V <sub>cc</sub> -0.5			V
V <sub>ol</sub>	Low-level output voltage	I <sub>ol</sub> =2mA I <sub>ol</sub> =1mA (V <sub>cc</sub> =5.0±0.5V) (V <sub>cc</sub> =3.3±0.3V)			0.4			0.4	V
I <sub>i</sub>	Input current	V <sub>i</sub> =0~V <sub>cc</sub>			±1			±1	μA
I <sub>o</sub>	Output current in off-state	/S=V <sub>ih</sub> or or /OE=V <sub>ih</sub> , V <sub>i/o</sub> =0~V <sub>cc</sub>			±1			±1	μA
I <sub>cc1</sub>	Active supply current (AC, MOS level )	/S<0.2V, Output-open Other inputs<0.2V or >V <sub>cc</sub> -0.2V	70ns		13	25		25	40
			1MHz		1.5	3		2	4
I <sub>cc2</sub>	Active supply current (AC, TTL level )	/S=V <sub>il</sub> , Output-open other inputs=V <sub>ih</sub> or V <sub>il</sub>	70ns		14	25		25	45
			1MHz		1.5	3		4	8
I <sub>cc3</sub>	Stand-by current	/S>V <sub>cc</sub> -0.2V, other inputs =0~V <sub>cc</sub>	~25°C	-G,-GI		1.2		2	μA
			-XG		0.05	0.3		0.1	
			~40°C	-G,-GI		3.6		6	
			-XG		0.8			1.2	
			~70°C	-G,-GI		12		20	
I <sub>cc4</sub>	Stand-by current	/S=V <sub>ih</sub> ,other inputs=0~V <sub>cc</sub>	-XG		2.4			5	mA
			-GI		24			40	

\* -3.0V in case of AC ( Pulse width &lt; 30ns )

**CAPACITANCE**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>i</sub>	Input capacitance	V <sub>i</sub> =GND, V <sub>i</sub> =25mVrms, f=1MHz			6	pF
C <sub>o</sub>	Output capacitance	V <sub>o</sub> =GND, V <sub>o</sub> =25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).

1: Typical value is one at T<sub>a</sub> = 25°C.2: C<sub>i</sub>, C<sub>o</sub> are periodically sampled and are not 100% tested.

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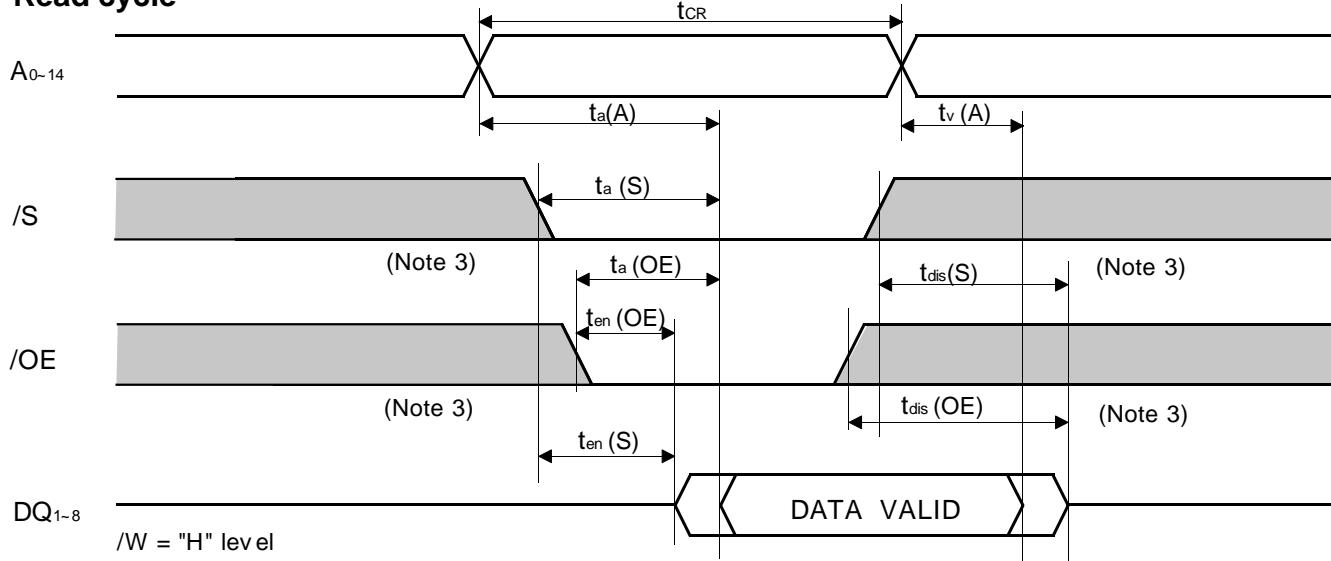
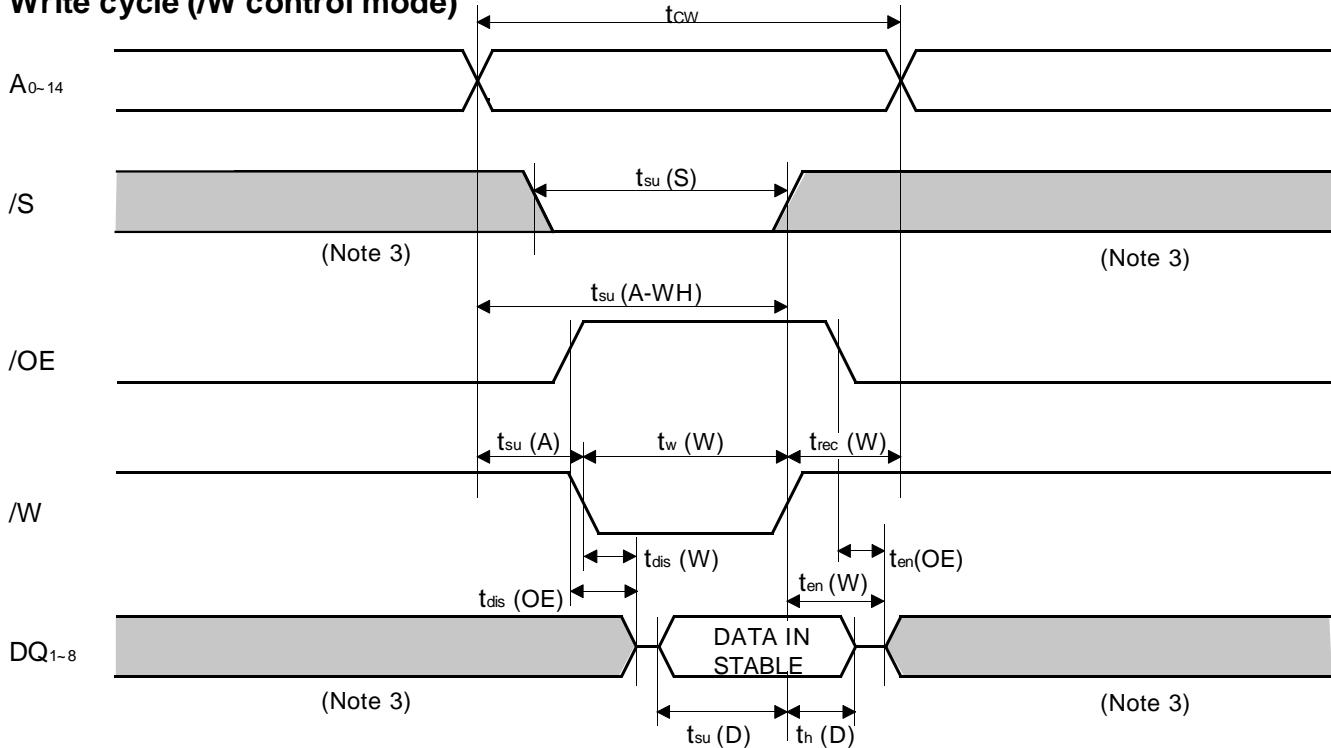
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**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

Symbol	Parameter	Limits1 Vcc=3.3±0.3V		Limits2 Vcc=5.0±0.5V		Unit
		Min	Max	Min	Max	
$t_{CR}$	Read cycle time	70		70		ns
$t_a(A)$	Address access time		70		70	ns
$t_a(S)$	Chip select access time		70		70	ns
$t_a(OE)$	Output enable access time		35		35	ns
$t_{dis}(S)$	Output disable time after /S high		25		25	ns
$t_{dis}(OE)$	Output disable time after /OE high		25		25	ns
$t_{en}(S)$	Output enable time after /S low	5		5		ns
$t_{en}(OE)$	Output enable time after /OE low	5		5		ns
$t_v(A)$	Data valid time after address	10		10		ns

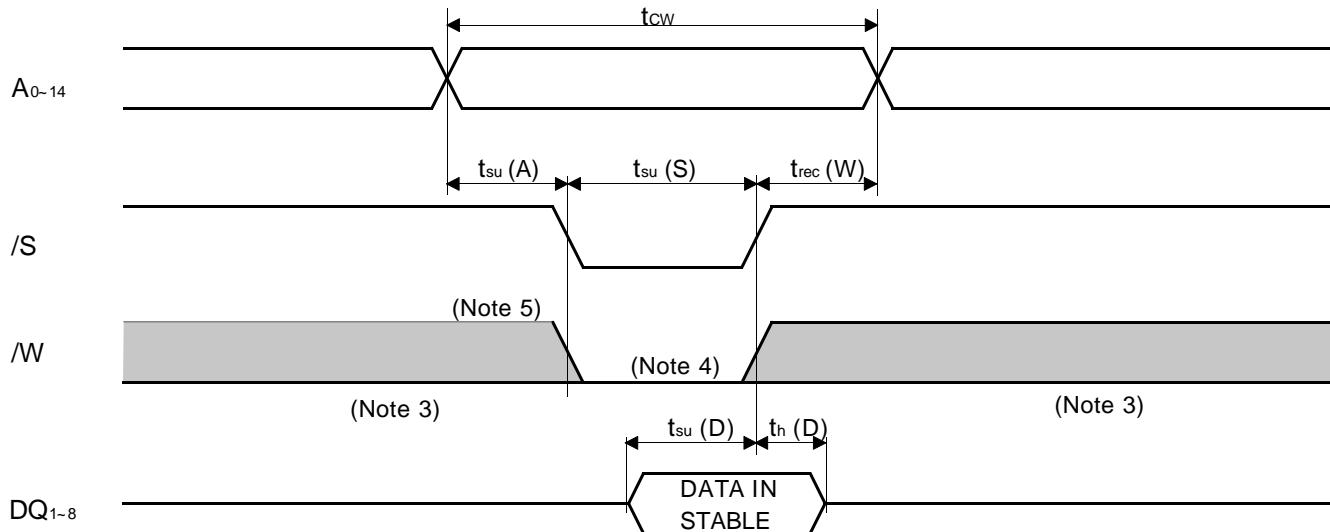
**(2) WRITE CYCLE**

Symbol	Parameter	Limits1 Vcc=3.3±0.3V		Limits2 Vcc=5.0±0.5V		Unit
		Min	Max	Min	Max	
$t_{cw}$	Write cycle time	70		70		ns
$t_w(W)$	Write pulse width	55		50		ns
$t_{su}(A)$	Address setup time	0		0		ns
$t_{su}(A-WH)$	Address setup time with respect to /W high	65		65		ns
$t_{su}(S)$	Chip select setup time	65		65		ns
$t_{su}(D)$	Data setup time	30		30		ns
$t_h(D)$	Data hold time	0		0		ns
$t_{rec}(W)$	Write recovery time	0		0		ns
$t_{dis}(W)$	Output disable time from /W low			25		ns
$t_{dis}(OE)$	Output disable time from /OE high			25		ns
$t_{en}(W)$	Output enable time from /W high	5		5		ns
$t_{en}(OE)$	Output enable time from /OE low	5		5		ns

**(3) TIMING DIAGRAMS****Read cycle****Write cycle (/W control mode)**

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**Write cycle ( /S control mode)****(4) MEASUREMENT CONDITIONS**Limits1:  $V_{CC}=3.3\pm 0.3V$ Input pulse level .....  $V_{IH}=2.4V, V_{IL}=0.4V$ 

Input rise and fall time ..... 5ns

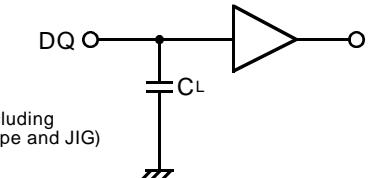
Reference level .....  $V_{OH}=V_{OL}=1.5V$ Output load ..... Fig.1,  $CL=30pF$  $CL=5pF$  (for ten,tdis)Transition is measured  $\pm 500mV$  from steady state voltage. (for ten,tdis)

Fig.1 Output load

Limits2:  $V_{CC}=5.0\pm 0.5V$ Input pulse level .....  $V_{IH}=2.4V, V_{IL}=0.6V$ 

Input rise and fall time ..... 5ns

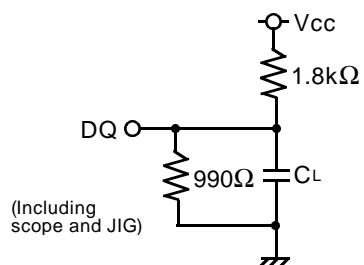
Reference level .....  $V_{OH}=V_{OL}=1.5V$ Output load ..... Fig.2,  $CL=100pF$  $CL=5pF$  (for ten,tdis)Transition is measured  $\pm 500mV$  from steady state voltage. (for ten,tdis)

Fig.2 Output load

Note 3 : Hatching indicates the state is "don't care".

4 : Writing is executed in overlap of /S and /W low.

5 : If /W goes low simultaneously with or prior to /S, the outputs remain in the high impedance state.

6 : Don't apply inverted phase signal externally when DQ pin is output mode.

7 : ten, tdis are periodically sampled and are not 100% tested.

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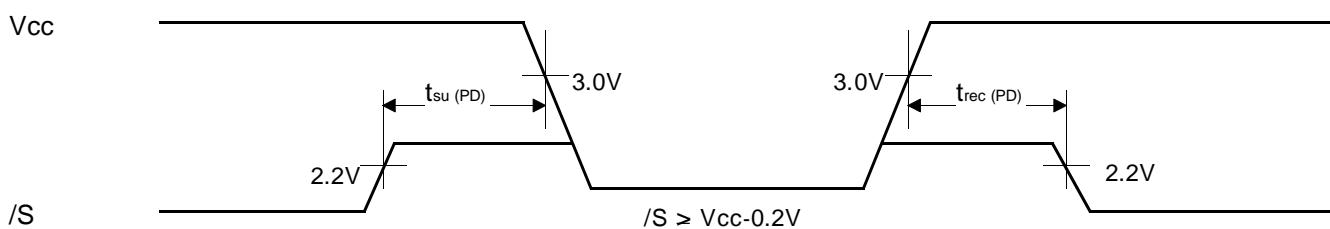
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**POWER DOWN CHARACTERISTICS****(1) ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>CC (PD)</sub>	Power down supply voltage		2			V
V <sub>I (S)</sub>	Chip select input /S	2.2V < V <sub>CC(PD)</sub>	2.2			V
		2V < V <sub>CC(PD)</sub> < 2.2V		V <sub>CC(PD)</sub>		V
I <sub>CC (PD)</sub>	Power down supply current	V <sub>CC</sub> = 3V, /S > V <sub>CC</sub> -0.2V, Other inputs=0~V <sub>CC</sub>	~25°C	-G,-GI		1
				-XG	0.05	0.2
			~40°C	-G,-GI		3
				-XG		0.6
			~70°C	-G,-GI		10
				-XG		2
			~85°C	-GI		20

**(2) TIMING REQUIREMENTS**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>su (PD)</sub>	Power down set up time		0			ns
t <sub>rec (PD)</sub>	Power down recovery time			t <sub>CR</sub>		ns

**(3) POWER DOWN CHARACTERISTICS****/S control mode**

RENESAS LSIs

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