

## Low Power, Class G Stereo Headphone Driver

### DESCRIPTION

The WM9010 is a low power stereo headphone driver designed for mobile handset and portable media player (PMP) applications. Class G amplifier technology is used to achieve high power efficiency and low quiescent current.

Stereo analogue inputs accept 1Vrms line level inputs; the Hi-Fi output drivers deliver up to 28mW into a 32Ω load. Active ground-loop feedback provides rejection of system-related ground noise.

An integrated charge pump circuit generates split-rail voltage supplies to power the ground-referenced headphone driver.

The WM9010 incorporates Wolfson Silent Switch™ technology to provide pop and click suppression whenever the WM9010 is enabled or disabled.

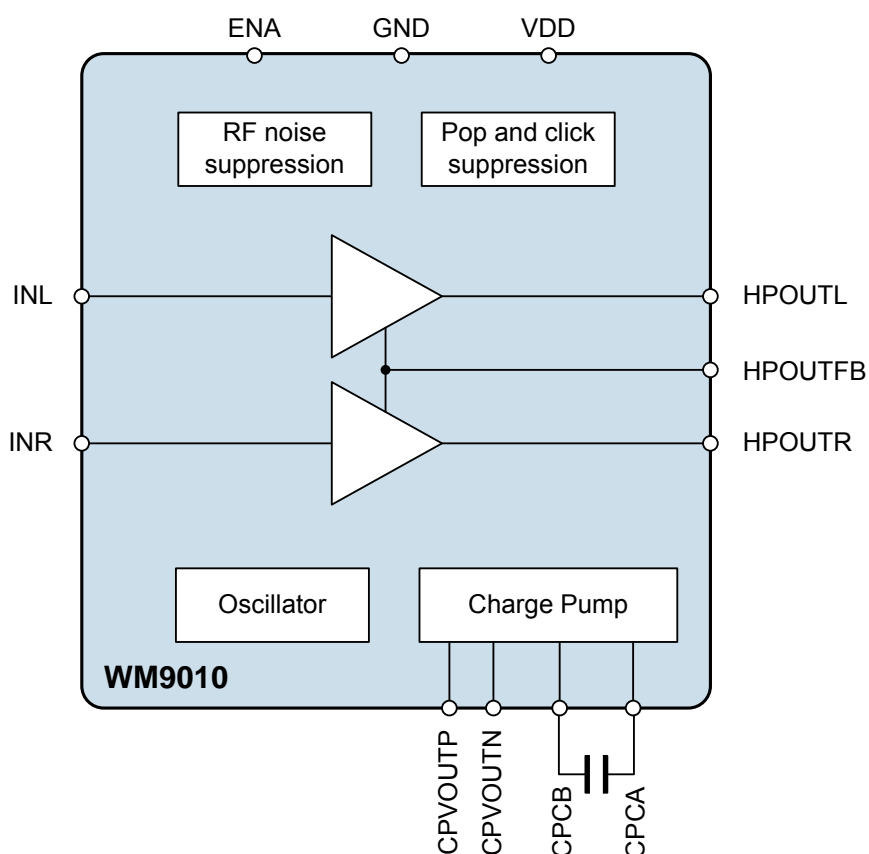
The WM9010 is supplied in a 12-pin CSP package.

### FEATURES

- Hi-fi audio headphone drivers (104dB SNR - 'A' weighted)
- Stereo analogue audio inputs
- Ground-referenced, cap-less headphone outputs
- Integrated charge pump and oscillator circuits
- Low quiescent current
- RF noise suppression
- Pop and click suppression
- 12-pin CSP package (1.84 x 1.34 x 0.7mm)

### APPLICATIONS

- Mobile Handsets
- Portable Media Players (PMP)
- Notebooks / Laptop computers
- LCD televisions

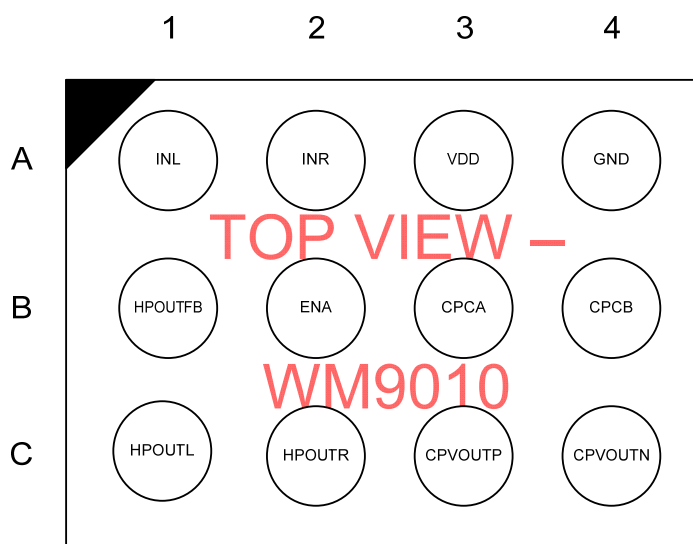


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## PIN CONFIGURATION

The WM9010 is supplied in a 12-pin CSP format. The pin configuration is illustrated below, showing the top-down view from above the chip.



## ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM9010ECSN/R	-40°C to +85°C	12-pin CSP (Pb-free, tape and reel)	MSL1	260°C

**Note:**

Reel quantity = 3500

## PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	INL	Analogue Input	Left channel analogue input
A2	INR	Analogue Input	Right channel analogue input
A3	VDD	Supply	Positive supply
A4	GND	Supply	Ground
B1	HPOUTFB	Analogue Input	HPOUTL and HPOUTR ground loop noise rejection feedback
B2	ENA	Digital Input	Device Enable / Mute control
B3	CPCA	Analogue Output	Charge pump fly-back capacitor pin
B4	CPCB	Analogue Output	Charge pump fly-back capacitor pin
C1	HPOUTL	Analogue Output	Left headphone output
C2	HPOUTR	Analogue Output	Right headphone output
C3	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin
C4	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage (VDD)	-0.3V	2.5V
Voltage range digital input (ENA)	-0.7V	3.3V
Voltage range analogue inputs	-0.7V	VDD +0.7V
Operating temperature range, T <sub>A</sub>	-40°C	+85°C
Junction temperature, T <sub>JMAX</sub>	-40°C	+150°C
Storage temperature after soldering	-65°C	+150°C

## RECOMMENDED OPERATING CONDITIONS

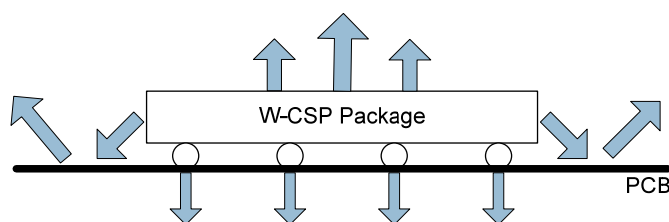
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	VDD	1.71	1.8	2.0	V
Logic 1 digital input (ENA)	ENA	0.8 x VDD	VDD	2.7	V
Ground	GND		0		V

## THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM9010 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND pin through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package pins to PCB (conduction).



**Figure 1 Heat Transfer Paths**

The temperature rise  $T_R$  is given by  $T_R = P_D \cdot \Theta_{JA}$

- $P_D$  is the power dissipated in the device.
- $\Theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.  $\Theta_{JA}$  is determined with reference to JEDEC standard JESD51-9.

The junction temperature  $T_J$  is given by  $T_J = T_A + T_R$ , where  $T_A$  is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	$T_A$	-40		85	°C
Operating junction temperature	$T_J$	-40		125	°C
Thermal Resistance	$\Theta_{JA}$		TBD		°C/W

**Note:**

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

## ELECTRICAL CHARACTERISTICS

## Test Conditions

VDD = 1.8V, GND = 0V, Load resistance = 16Ω, T<sub>A</sub> = +25°C, 1kHz signal unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Inputs (INL, INR)</b>						
Maximum input signal level		Single-ended input		VDD/1.8		V <sub>rms</sub>
Input resistance				20		kΩ
Input capacitance				TBD		pF
<b>Headphone Output Path (HPOUTL, HPOUTR)</b>						
Output Power	P <sub>O</sub>	R <sub>L</sub> = 32Ω; THD+N = 0.1%		27		mW
		R <sub>L</sub> = 32Ω; THD+N = 1%		28		
		R <sub>L</sub> = 16Ω; THD+N = 0.1%		31		
		R <sub>L</sub> = 16Ω; THD+N = 1%		33		
Signal to Noise ratio	SNR	A-weighted		104		dB
Total Harmonic Distortion + Noise	THD+N	R <sub>L</sub> = 32Ω; P <sub>O</sub> = 20mW		-88		dB
		R <sub>L</sub> = 32Ω; P <sub>O</sub> = 5mW		-84		
		R <sub>L</sub> = 16Ω; P <sub>O</sub> = 20mW		-80		
		R <sub>L</sub> = 16Ω; P <sub>O</sub> = 5mW		-79		
DC Offset				0.5	1	mV
Channel separation				TBD		dB
Mute attenuation		ENA = 0		95		dB
Power supply rejection	PSRR	100mV pk-pk @ 217Hz on VDD		TBD		dB
Maximum load capacitance		HPOUTL or HPOUTR			2	nF
<b>Digital Input (ENA)</b>						
Input high level			0.8 x VDD			V
Input low level					0.2 x VDD	V
<b>Other Parameters</b>						
Quiescent current	I <sub>VDD</sub>	ENA = 1, Inputs grounded		1		mA
Shutdown current	I <sub>VDD</sub>	ENA = 0		1		μA
Start-up time				12		ms

## TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (L/R) (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, and the right channel amplitude is measured. Next, a full scale signal is applied to the right channel only, and the left channel amplitude is measured. The worst case channel separation is quoted; this is the difference in level between the full-scale output and the cross-channel output signal level, expressed as a ratio.
5. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
6. Mute attenuation - This is a measure of the difference in level between the full scale output signal and the output with mute applied (ie. ENA = logic 0).
7. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

## DEVICE DESCRIPTION

### INTRODUCTION

The WM9010 is a low power stereo headphone driver designed for mobile handset and portable media player (PMP) applications. It is packaged in a 12-pin CSP.

The device comprises two analogue input pins, each accepting line signals up to 1Vrms. The signal path gain is fixed at 0dB. The headphone output drivers deliver up to 28mW into a 32Ω load.

The WM9010 incorporates Class G technology to achieve high efficiency and low quiescent current. An integrated charge pump circuit is used to generate the split (positive and negative) power rails from a single VDD supply. The ground-referenced headphone driver design reduces the device power consumption and also eliminates external DC-blocking capacitors on the audio output path.

The WM9010 is enabled when a logic high level is detected on ENA. Note that the ENA pin can support digital logic levels up to 2.7V.

Wolfson's Silent Switch™ technology is incorporated in order to minimise 'pop' noise whenever the WM9010 is enabled or disabled.

A power on reset circuit ensures correct start-up and shut-down when VDD is switched on or off. The WM9010 is held in reset when the ENA pin is held low, offering a low-power standby state.

Short circuit and thermal protection is also provided.

### HEADPHONE DRIVER

The WM9010 has two analogue input pins, INL and INR. The maximum analogue input signal level varies with VDD, but is typically 0dBV (1Vrms) when VDD = 1.8V. This is suitable for single-ended connection to line level input signals.

The headphone output drivers are capable of driving up to 28mW into a 32Ω load such as a stereo headset or headphones. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors. This is achieved by having separate positive and negative supply rails powered by an on-chip charge pump.

A pop-suppression circuit ensures that DC offsets are minimised, suppressing 'pop' noise and reducing power consumption. To obtain optimal DC offsets, the device should be powered on with no signal on the input pins.

The headphone output incorporates a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The return path is via HPOUTFB. This pin should be connected to the headphone as illustrated in Figure 2.

It is recommended to connect a zobel network to the headphone output pins HPOUTL and HPOUTR for best audio performance in all applications. The components of the zobel network have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier. The capacitance of lengthy cables or PCB tracks can also lead to amplifier instability. The zobel network should comprise of a 20Ω resistor and 100nF capacitor in series with each other, as illustrated in Figure 2.

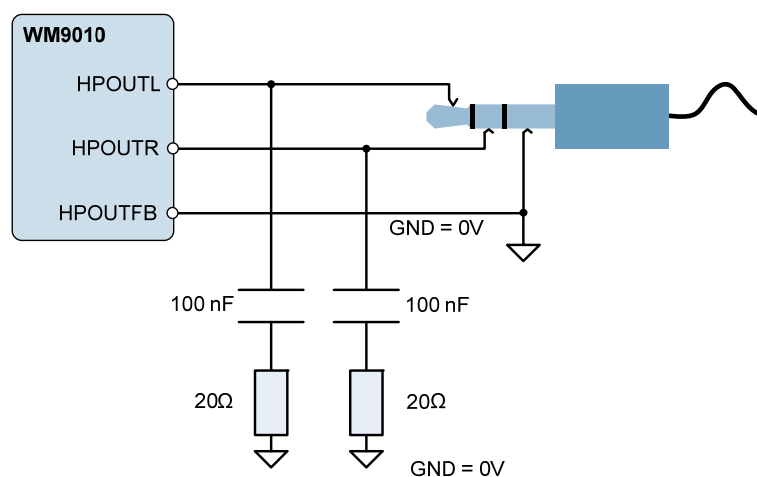


Figure 2 External Connections for HPOUTL and HPOUTR

## CHARGE PUMP

The WM9010 incorporates a charge pump circuit, which generates the supply rails for the headphone output drivers. The charge pump is powered from VDD, and generates split rails CPVOUTP and CPVOUTN. The circuit is adaptive according to the audio signal conditions, supporting the Class G operation and ensuring optimum circuit configuration at all times. The switching clock for the charge pump is generated internally.

The external connections for the charge pump are illustrated in Figure 3. A fly-back capacitor is connected between the CPCA and CPCB pins. De-coupling capacitors are required on CPVOUTP and CPVOUTN. An input decoupling capacitor may also be required at VDD, depending upon the system configuration.

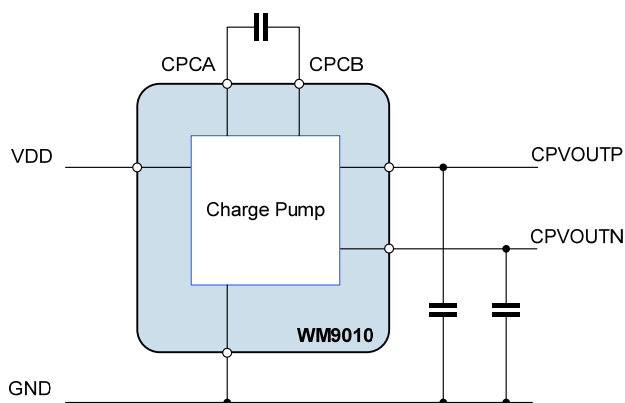


Figure 3 External Connections for Charge Pump

## APPLICATIONS INFORMATION

### RECOMMENDED EXTERNAL COMPONENTS

Figure 4 provides a summary of recommended external components for WM9010. Note that the actual requirements may differ according to the specific target application.

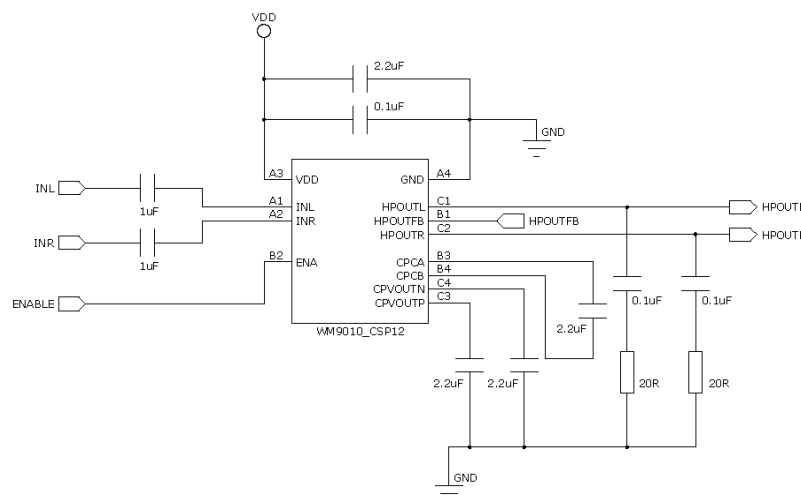


Figure 4 WM9010 Recommended External Components Diagram

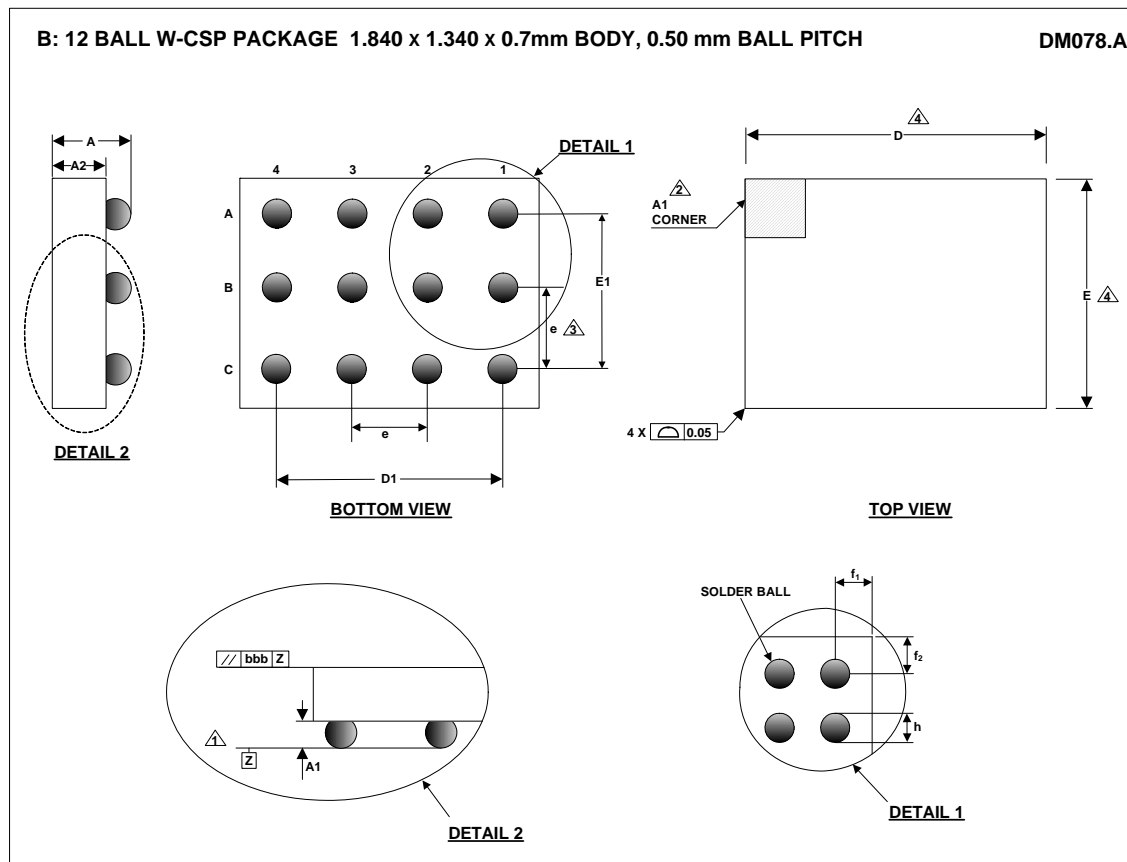
### PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM9010 device as possible, with current loop areas kept as small as possible.

## PACKAGE DIMENSIONS

B: 12 BALL W-CSP PACKAGE 1.840 x 1.340 x 0.7mm BODY, 0.50 mm BALL PITCH

DM078.A



Symbols	Dimensions (mm)			NOTE
	MIN	NOM	MAX	
A	0.675	0.7	0.725	
A1	0.187	0.2	0.213	
A2	0.488	0.500	0.512	
D	1.820	1.840	1.860	
D1		1.500 BSC		
E	1.320	1.340	1.360	
E1		1.000 BSC		
e		0.500 BSC		3
f <sub>1</sub>	0.160			
f <sub>2</sub>	0.160			
h		0.267		

## NOTES:

1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
3. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
4. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
5. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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