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Revisions			
Rev	Description	Date	Approved
x1	A70 release placement	23 May 11	TTC
x2	preliminary schematics	27 May 11	TTC
A	Prototype release	22 Jul 11	TTC
AX1	Rev B changes 1.U53- Switch from socketed to non-socketed processor 2.SPI port connections added on secondary connector 3. Zero ohms R added on PTC16 and PTC17 to allow for disconnect from NAND. 4.FB_AD[31:24] is connected with EBI_D[7:0] on the primary. 5. Push button labels are placed at PTD0,PTE26 6. VrefH, VrefL are removed from Primary elevator connector. 7.LCD_Contrast tied at PTC18. 8.PTD0,PTD1 nets of U8 are renamed 9.Primary connector pin B21 is connected to PTE19, A9 is connected to PTE18 10.L3(IND_0805) is replaced with R143(R0805) zero ohms resistor Schematics Alignment	24 Oct 11	Peter, Melissa
B	A085 Release	27 Oct 11	
B1	A085 Release - MCU Marketing part number updated as per MCO30515	3 Nov 11	Peter

1. Unless Otherwise Specified:

- All resistors are in ohms
- All capacitors are in uF
- All voltages are DC
- All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:

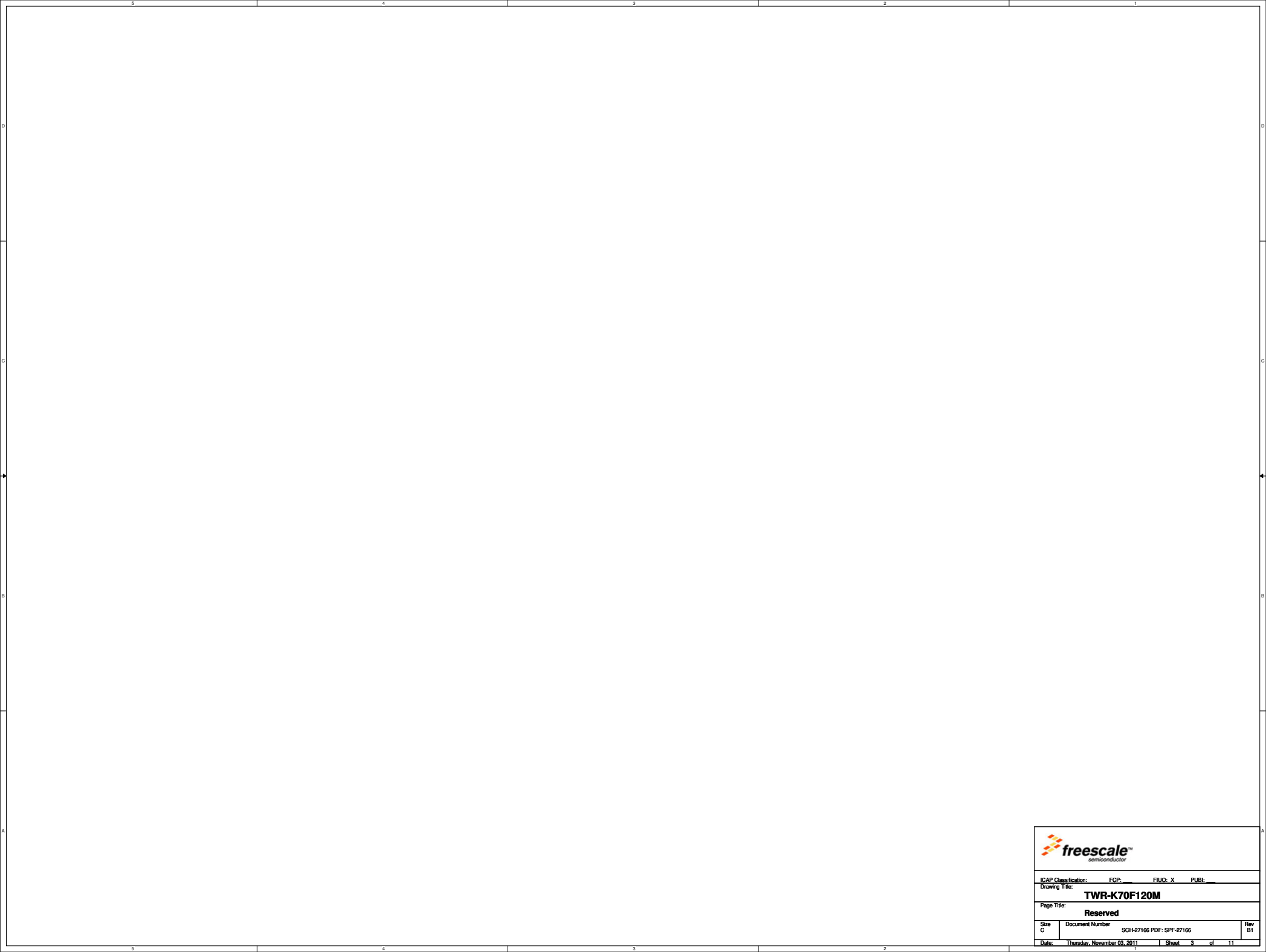
- _B Denotes - Active-Low Signal
- <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

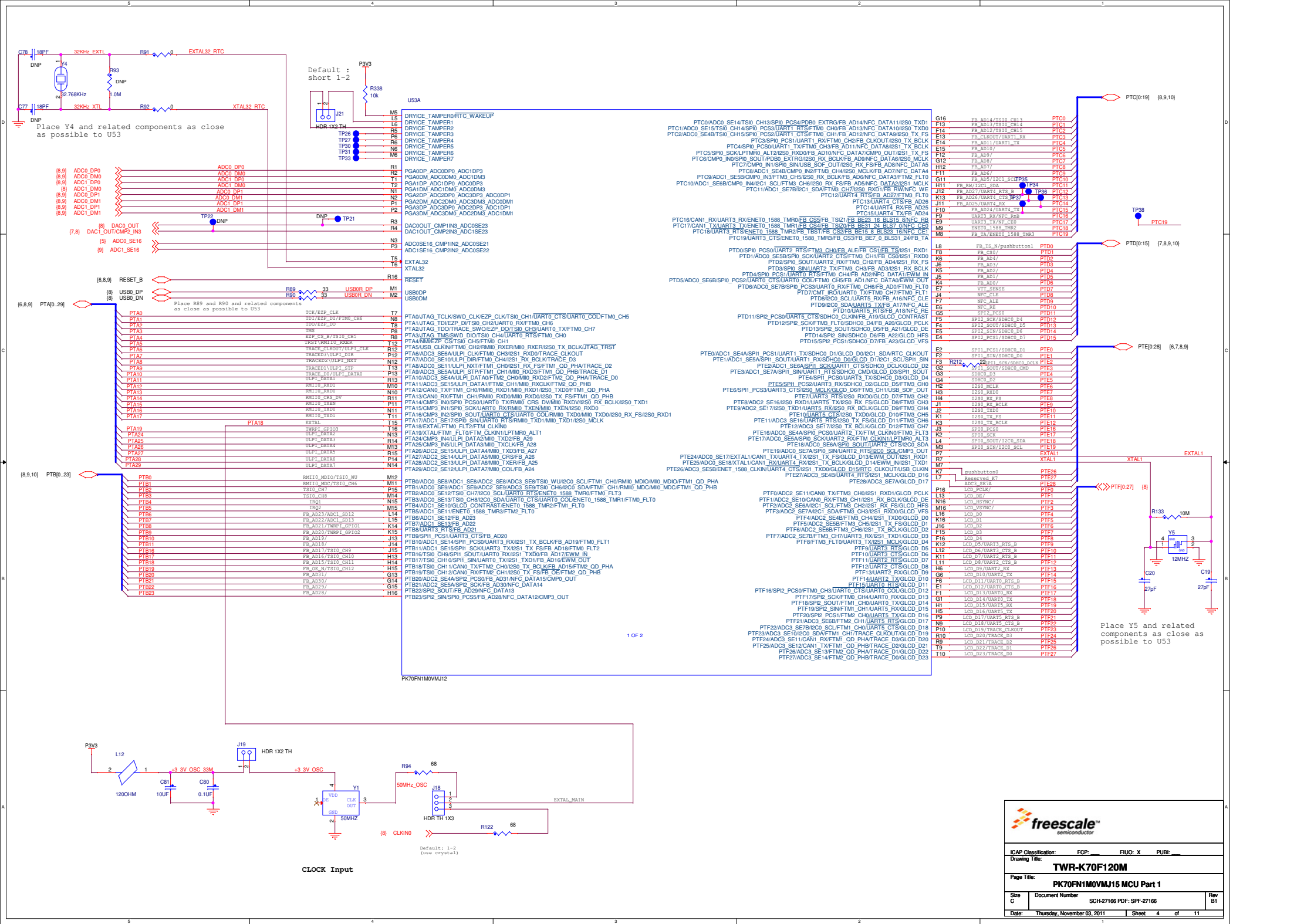
Power & Ground Nets

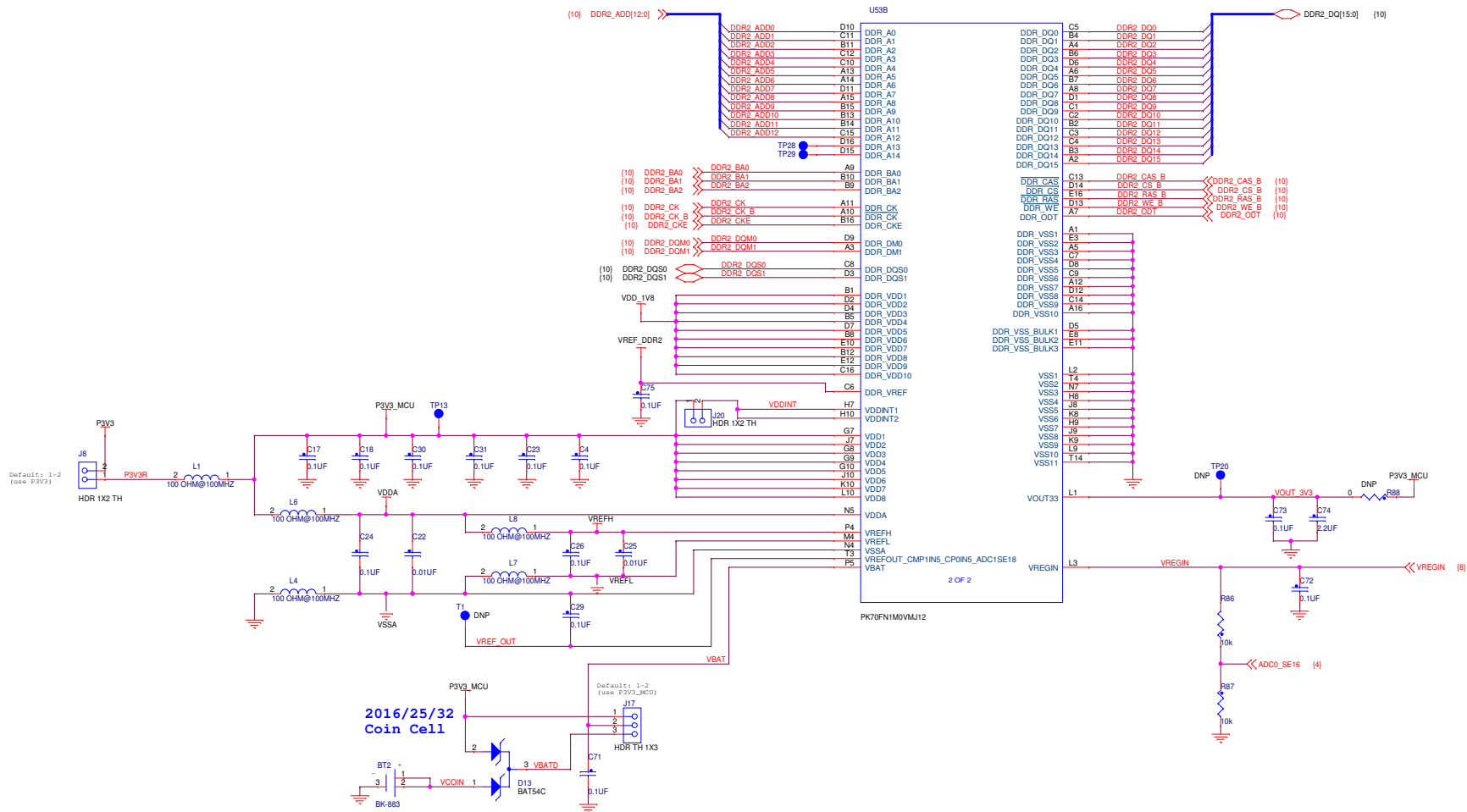
NET	VOLTAGE	DESCRIPTION
P5V_USB	5V	Primary input power. Filtered from USB connector. Input to USB power switch.
P5V_SW	5V	Output of USB power switch controlled by the 5V_EN signal from the JM60 MCU. Used by OSBDM voltage translation circuits.
P5V_TRG_USB	5V	Output of USB power switch controlled by the VTRG_EN signal from the JM60 MCU. Provides input to regulator.
P3V3	3.3V	Output of regulator using USB power input (P5V_TRG_USB).
P3V3_MCU	3.3V	MCU digital power. Filtered from P3V3.
VDDA	3.3V	VDDA power for MCU and analog circuits. Filtered from P3V3_MCU.
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital Ground.
VDD_INT	3.3V	MCU Internal supply
VREF_DDR2	0.9V	DDR2 VREF = VDDQ/2 supply for MCU and SDRAM
VTT_DDR2	0.9V	DDR2 VTT= VDDQ/2 termination supply for MCU and SDRAM
VDD_1V8	1.8V	DDR2 VDDQ supply for MCU and SDRAM

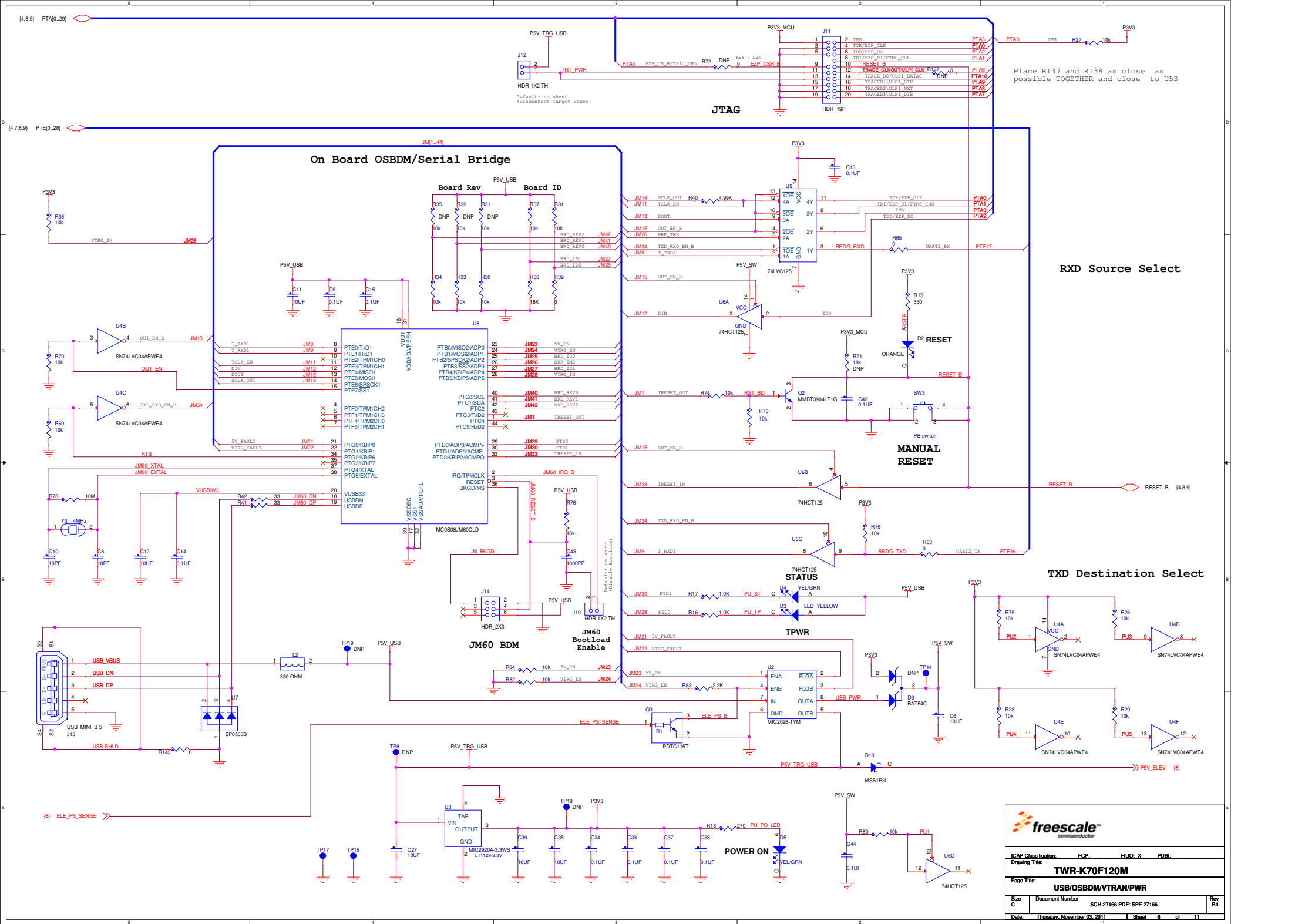
		
ICAP Classification: FCP: FLUQ: X PUB:		
Drawing Title: TWR-K70F120M		
Page Title: Notes		
Size C	Document Number SCH-27166 PDF: SPF-27166	Rev B1
Date: Thursday, November 03, 2011	Sheet 2 of 11	



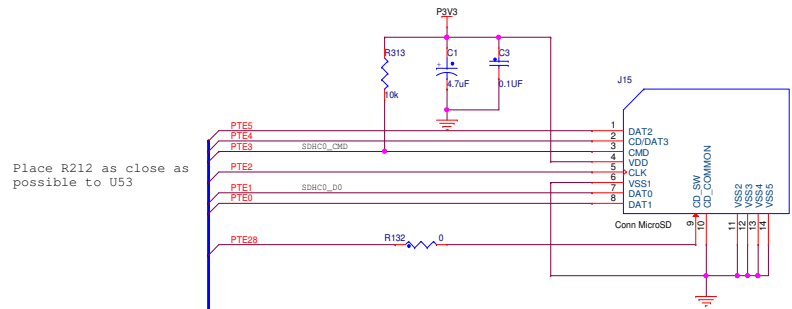
ICAP Classification:		FCP:	FIUQ: X	PUB:
Drawing Title:		TWR-K70F120M		
Page Title:		Reserved		
Size C	Document Number	SCH-27166 PDF: SPF-27166		Rev B1
Date:	Thursday, November 03, 2011	Sheet	3 of 11	



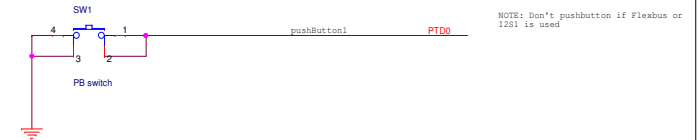




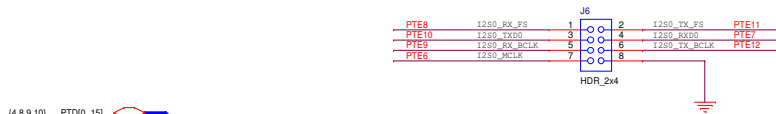
MICRO SD INTERFACE



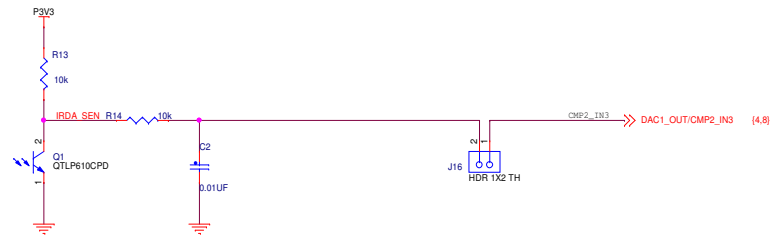
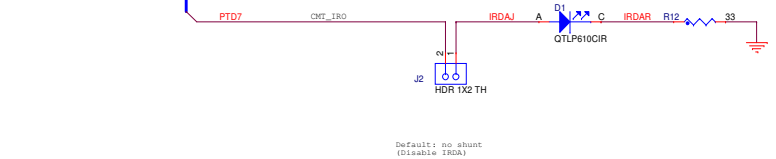
PUSH BUTTON

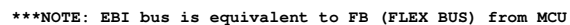


I2S SAI HEADER



IRDA





and remove R43,R44

DDR-2 MEMORIES AND TERMINATIONS

Note:

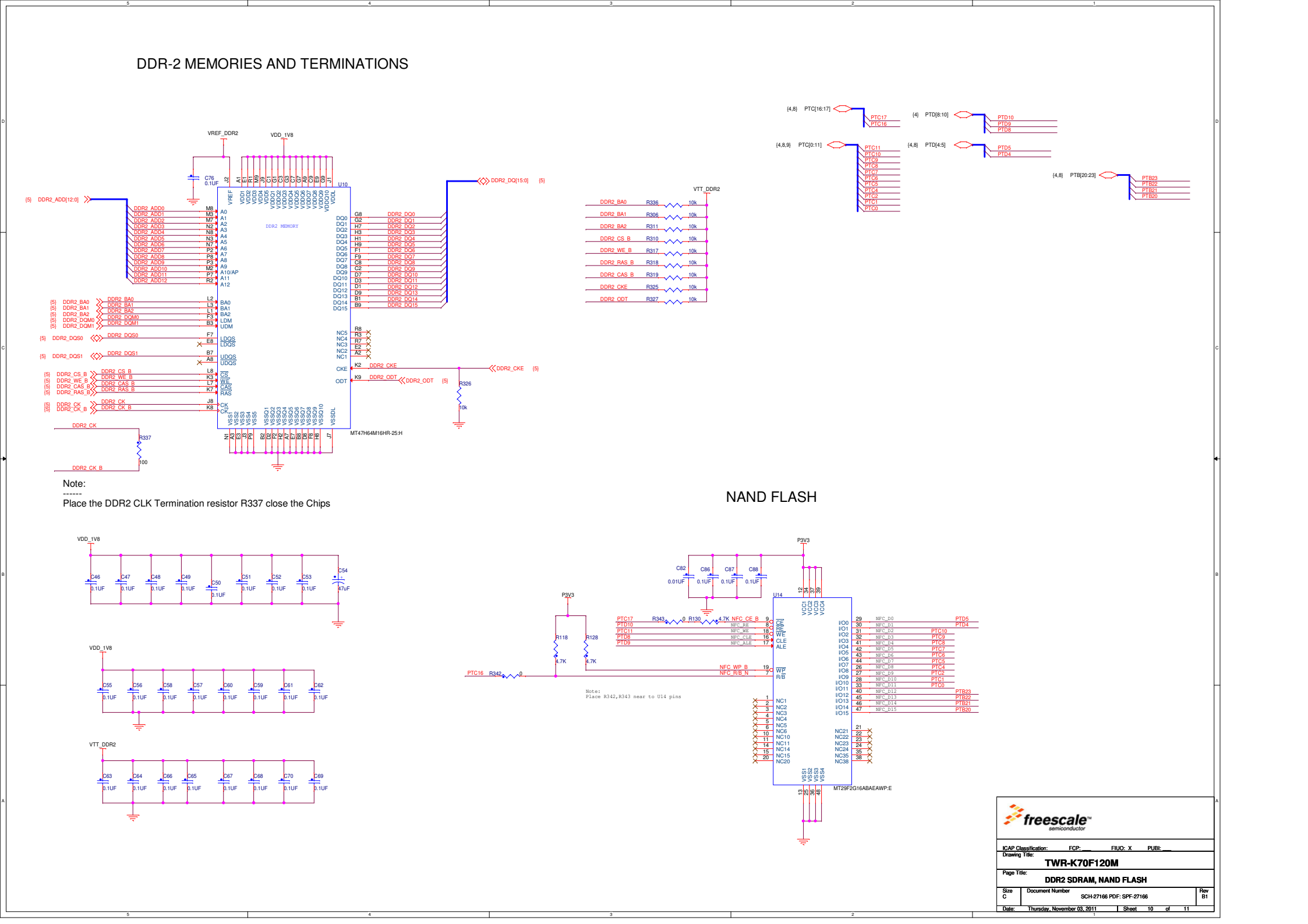
Place the DDR2 CLK Termination resistor R337 close the Chips

NAND FLASH

Note:
Place R342, R343 near to U14 pins

ICAP Classification: FCP: FLUQ: X PUBk:
Drawing Title: **TWR-K70F120M**
Page Title: **DDR2 SDRAM, NAND FLASH**
Size C Document Number SCH-27166 PDF: SPF-27166 Rev B1
Date: Thursday, November 03, 2011 Sheet 10 of 11

Place the DDR2 CLK Termination resistor R337 close the Chips



DDR-2 MEMORIES AND TERMINATIONS

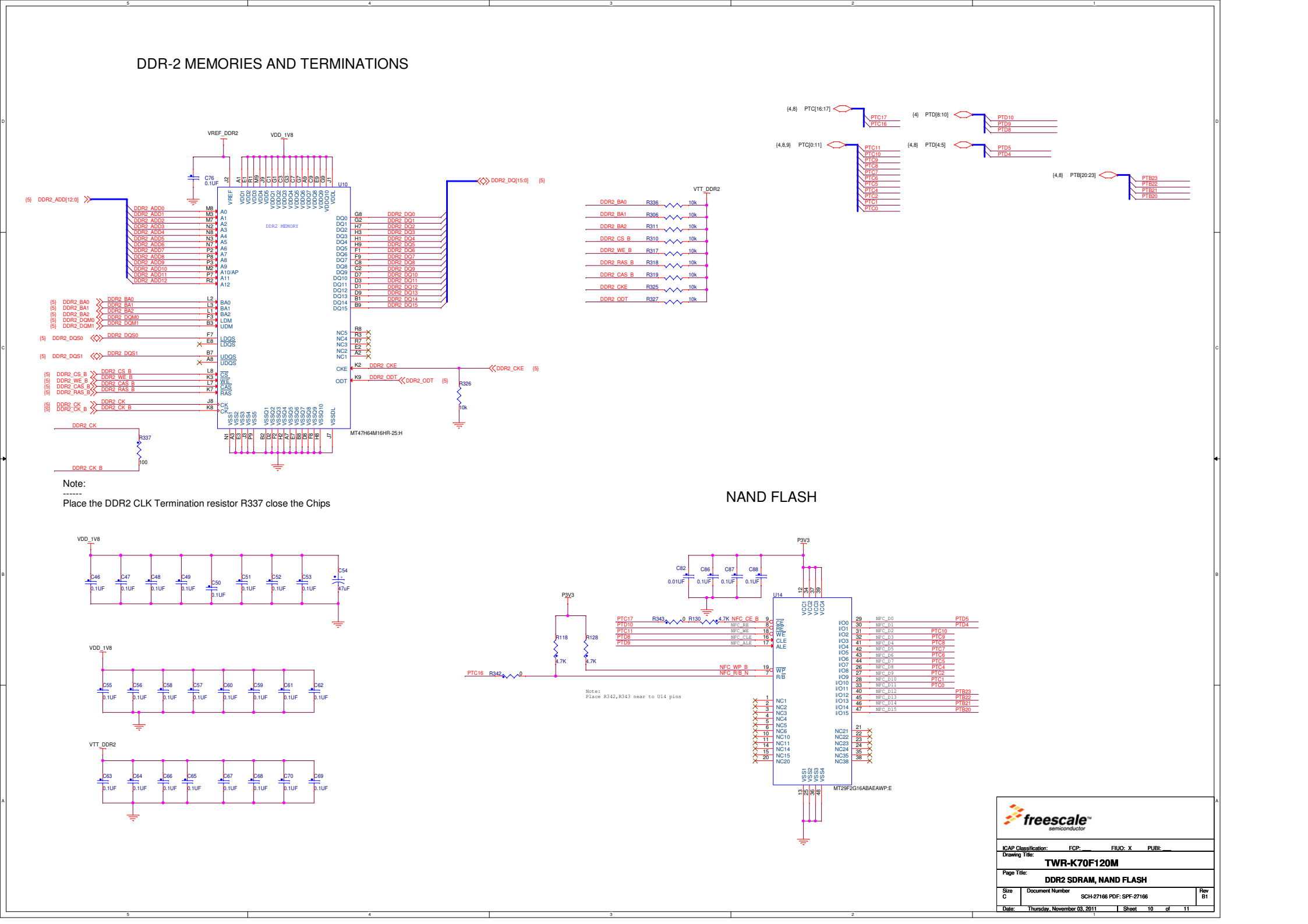
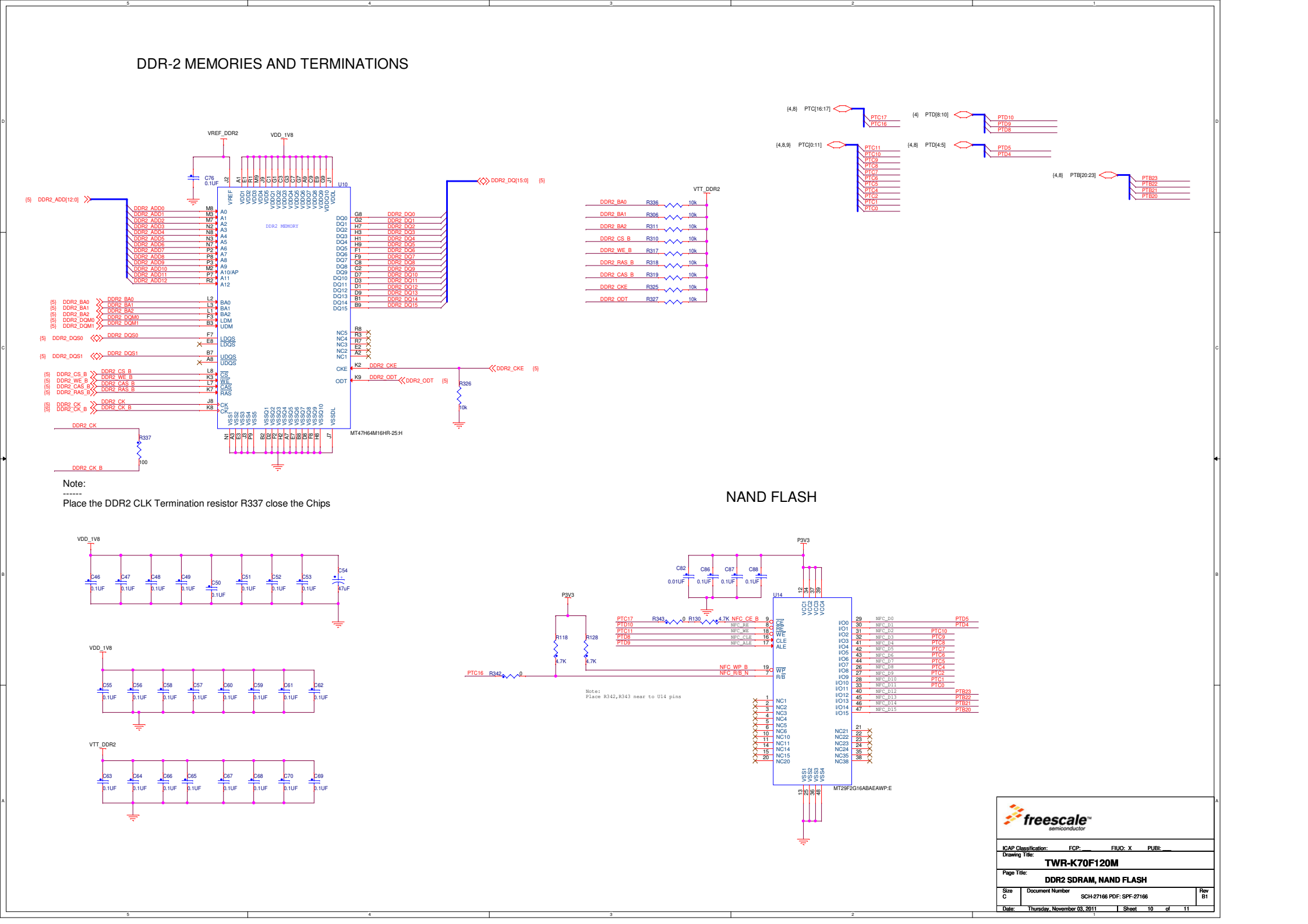
Note:

Place the DDR2 CLK Termination resistor R337 close the Chips

NAND FLASH

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Place R342,R343 near to U14 pins

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DDR-2 MEMORIES AND TERMINATIONS

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Place the DDR2 CLK Termination resistor R337 close the Chips

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P9V3

C135 47uF

C136 47uF

C137 1uF

Place C135 next to pins 21 and 22, C136 next to pins 9 and 10, C137 next to pin 23 of U56

U56

15 RT

14 RUN1

13 RUN2

24 TRACK/SS1

2 ITH1

6 ITH2

3 MODE/SYNC

4 PHASE

18 PGOOD1

16 PGOOD2

LTC3618

23 SWIN

21 PVIN1_1

22 PVIN1_2

20 PVIN2_1

19 PVIN2_2

VDDOIN

SW1_1

SW1_2

7

19

20

1 L9 0.47uH

2

R339

VDD_1V8

C133 47uF

VTT_DDR2

11

12

1 L10 0.47uH

2

422.0K

R341

210.0K

5

17

FB1

SW2_1

SW2_2

FB2

VTTTR

VREF_DDR2

C79 0.1uF

C134 47uF