INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT533

Octal D-type transparent latch; 3-state; inverting

Product specification
File under Integrated Circuits, IC06

December 1990





Octal D-type transparent latch; 3-state; inverting

74HC/HCT533

FEATURES

- · 3-state inverting outputs for bus oriented applications
- · Common 3-state output enable input
- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT533 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT533 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When $\overline{\text{OE}}$ is LOW, the contents of the 8 latches are available at the outputs.

When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The "533" is functionally identical to the "373", "563" and "573", but the "373" and "573" have non-inverted outputs and the "563" and "573" have a different pin arrangement.

QUICK REFERENCE DATA

 $GND = 0 \text{ V}; T_{amb} = 25 \, ^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYI | TYPICAL | | |
|-------------------------------------|---|---|-----|---------|------|--|
| | PARAMETER | CONDITIONS | НС | нст | UNIT | |
| t _{PHL} / t _{PLH} | propagation delay | $C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$ | | | | |
| | D_n to \overline{Q}_n | | 14 | 16 | ns | |
| | LE to \overline{Q}_n | | 18 | 19 | ns | |
| C _I | input capacitance | | 3.5 | 3.5 | pF | |
| C _{PD} | power dissipation capacitance per latch | notes 1 and 2 | 34 | 34 | pF | |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

 f_0 = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

 C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

ORDERING INFORMATION

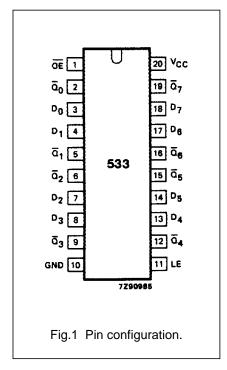
See "74HC/HCT/HCU/HCMOS Logic Package Information".

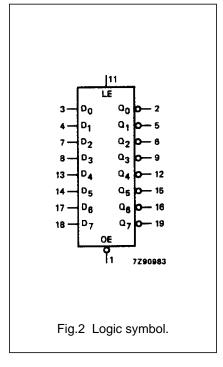
Octal D-type transparent latch; 3-state; inverting

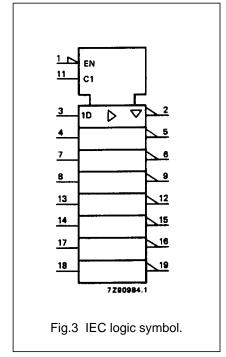
74HC/HCT533

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION | | | | | |
|----------------------------|--------------------------------------|--|--|--|--|--|--|
| 1 | ŌĒ | 3-state output enable input (active LOW) | | | | | |
| 2, 5, 6, 9, 12, 15, 16, 19 | \overline{Q}_0 to \overline{Q}_7 | 3-state latch outputs | | | | | |
| 3, 4, 7, 8, 13, 14, 17, 18 | D ₀ to D ₇ | data inputs | | | | | |
| 10 | GND | ground (0 V) | | | | | |
| 11 | LE | latch enable input (active HIGH) | | | | | |
| 20 | V _{CC} | positive supply voltage | | | | | |

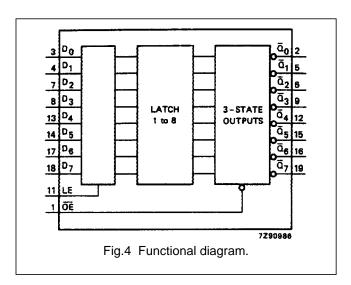


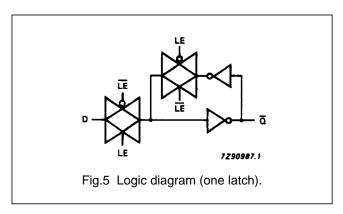




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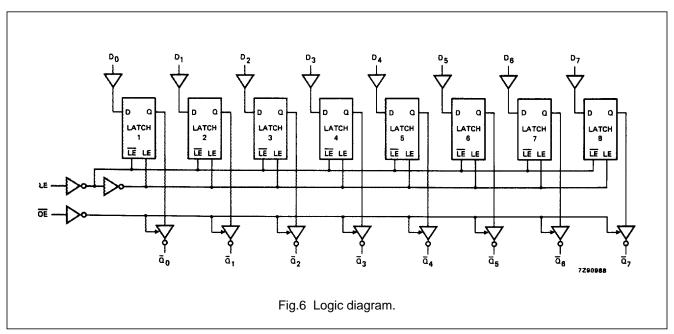


FUNCTION TABLE

| OPERATING | II | NPUT | S | INTERNAL | OUTPUTS | | |
|--|--------|--------|----------------|----------|--------------------------------------|--|--|
| MODES | ŌΕ | LE | D _n | LATCHES | \overline{Q}_0 TO \overline{Q}_7 | | |
| enable and read register (transparent mode) | L L | H H | L H | L H | H | | |
| latch and read register | L L | L L | l h | L H | Η | | |
| latch register and disable outputs | H H | X X | X X | X X | Z Z | | |

Notes

- 1. H = HIGH voltage level
 - h = HIGH voltage level one set-up prior to the HIGH-to-LOW LE transition
 - L = LOW voltage level
 - I = LOW voltage level one set-up prior to the HIGH-to-LOW LE transition
 - X = don't care
 - Z = high impedance OFF-state



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74HC/HCT533

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

| | PARAMETER | T _{amb} (°C) | | | | | | | | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|-------------------|-----------|
| SYMBOL | | | 74HC | | | | | | | | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | UNIT | V _{CC} | WAVEFORMS |
| | | min. | typ. | max. | min. | max. | min. | max. | - | (•, | |
| t _{PHL} / t _{PLH} | $\begin{array}{c} \text{propagation delay} \\ D_n \text{ to } \overline{Q}_n \end{array}$ | | 47 17 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay LE to $\overline{\mathbf{Q}}_{\mathbf{n}}$ | | 58 21 17 | 175 35 30 | | 220 44 37 | | 265 53 45 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PZH} / t _{PZL} | 3-state output enable time \overline{OE} to \overline{Q}_n | | 44 16 13 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{PHZ} / t _{PLZ} | | | 50 18 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _W | LE pulse width HIGH | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{su} | set-up time D _n to LE | 50 10 9 | 3 1 1 | | 65 13 11 | | 75 15 13 | | ns | 2.0 4.5 6.0 | Fig.10 |
| t _h | hold time D _n to LE | 35 7 6 | 3 1 1 | | 45 9 8 | | 55 11 9 | | ns | 2.0 4.5 6.0 | Fig.10 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT | | | | | | |
|----------------|-----------------------|--|--|--|--|--|--|
| D _n | 0.15 | | | | | | |
| LE | 0.30 | | | | | | |
| ŌE | 0.55 | | | | | | |

AC CHARACTERISTICS FOR 74HCT

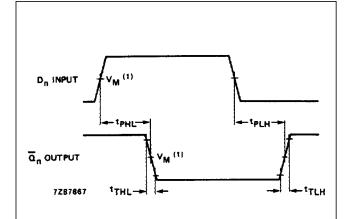
 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|-------|------|------------|------|-------------|------|------|-----------------|-----------|
| | | | 74HCT | | | | | | | | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | UNIT | V _{CC} | WAVEFORMS |
| | | min. | typ. | max. | min. | max. | min. | max. | | (•) | |
| t _{PHL} / t _{PLH} | $\begin{array}{c} \text{propagation delay} \\ D_n \text{ to } \overline{Q}_n \end{array}$ | | 19 | 34 | | 43 | | 51 | ns | 4.5 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay LE to \overline{Q}_n | | 22 | 38 | | 48 | | 57 | ns | 4.5 | Fig.8 |
| t _{PZH} / t _{PZL} | 3-state output enable time \overline{OE} to \overline{Q}_n | | 19 | 35 | | 44 | | 53 | ns | 4.5 | Fig.9 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time \overline{OE} to \overline{Q}_n | | 18 | 30 | | 38 | | 45 | ns | 4.5 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.7 |
| t _W | LE pulse width HIGH | 16 | 5 | | 20 | | 24 | | ns | 4.5 | Fig.8 |
| t _{su} | set-up time D _n to LE | 10 | 3 | | 13 | | 15 | | ns | 4.5 | Fig.10 |
| t _h | hold time D _n to LE | 8 | 2 | | 10 | | 12 | | ns | 4.5 | Fig.10 |

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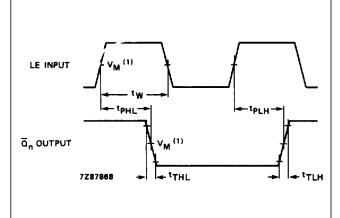
74HC/HCT533

AC WAVEFORMS



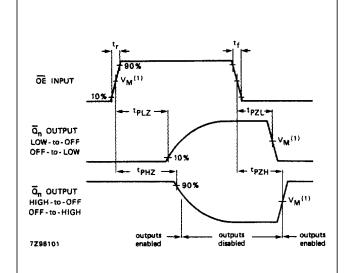
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the data input (D_n) to output (\overline{Q}_n) propagation delays and the output transition times.



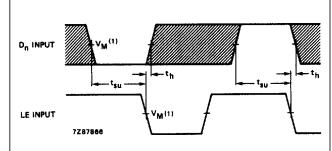
(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (\overline{Q}_n) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M = 50\%$; $V_I = GND \text{ to } V_{CC}$. HCT: $V_M = 1.3 \text{ V}$; $V_I = GND \text{ to } 3 \text{ V}$.

Fig.10 Waveforms showing the data set-up and hold times for D_n input to LE input.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".