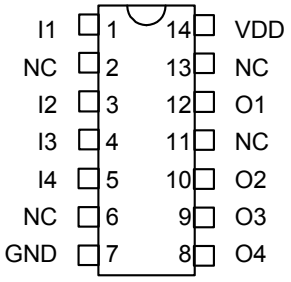
MONOLITHIC QUAD FIXED DELAY LINE (SERIES 3D3314)

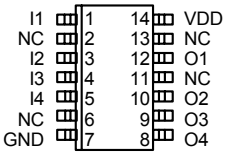
FEATURES

- All-silicon, low-power 3.3V CMOS technology
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- Low ground bounce noise
- Leading- and trailing-edge accuracy
- **Delay range:** 10ns through 400ns
- **Delay tolerance:** 2% or 0.5ns (3.3V, 25C)
- **Temperature stability:** ±1% typical (0C-70C)
- **Vdd stability:** ±1% typical (3.0V-3.6V)
- **Static Idd:** 1.3ma typical
- **Minimum input pulse width:** 25% of total delay

PACKAGES



3D3314-xx DIP-14



3D3314D-xx SOIC-14

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D3314 device is a small, versatile, quad fixed monolithic delay line. Delay values ranging from 10ns through 400ns may be specified via the device dash number. Each input is reproduced at the corresponding output without inversion, shifted in time as per user selection. The 3D3314 is 3.3V CMOS-compatible and features both rising- and falling-edge accuracy. The device is offered in a standard 14-pin auto-insertable DIP and a space saving surface mount 14-pin SOIC.

PIN DESCRIPTIONS

I1-I4	Signal Inputs
O1-O4	Signal Outputs
VDD	3.3V
GND	Ground
NC	No Connection

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DELAY AND TOLERANCE (ns)	INPUT RESTRICTIONS			
		RECOMMENDED		ABSOLUTE	
		Max Freq	Min P.W.	Max Freq	Min P.W.
3D3314-10	10.0 ± 1.0	40.0 MHz	12.5 ns	166 MHz	3.0 ns
3D3314-15	15.0 ± 1.0	26.6 MHz	18.8 ns	166 MHz	3.0 ns
3D3314-20	20.0 ± 1.0	20.0 MHz	25.0 ns	166 MHz	3.0 ns
3D3314-25	25.0 ± 1.0	16.0 MHz	31.3 ns	166 MHz	3.0 ns
3D3314-30	30.0 ± 1.0	13.3 MHz	37.5 ns	166 MHz	3.0 ns
3D3314-40	40.0 ± 1.0	10.0 MHz	50.0 ns	125 MHz	4.0 ns
3D3314-50	50.0 ± 1.0	8.00 MHz	62.5 ns	100 MHz	5.0 ns
3D3314-75	75.0 ± 1.5	5.33 MHz	93.8 ns	66.6 MHz	7.5 ns
3D3314-100	100 ± 2.0	4.00 MHz	125.0 ns	50.0 MHz	10.0 ns
3D3314-125	125 ± 2.5	3.20 MHz	156.3 ns	40.0 MHz	12.5 ns
3D3314-150	150 ± 3.0	2.66 MHz	187.5 ns	33.3 MHz	15.0 ns
3D3314-200	200 ± 4.0	2.00 MHz	250.0 ns	25.0 MHz	20.0 ns
3D3314-250	250 ± 5.0	1.60 MHz	312.5 ns	20.0 MHz	25.0 ns
3D3314-300	300 ± 6.0	1.33 MHz	375.0 ns	16.6 MHz	30.0 ns
3D3314-400	400 ± 8.0	1.00 MHz	500.0 ns	12.5 MHz	40.0 ns

NOTES: Any dash number between 10 and 400 not shown is also available as standard

APPLICATION NOTES

OPERATIONAL DESCRIPTION

The 3D3314 quad fixed delay line architecture is shown in Figure 1. Each delay line is composed of a number of delay cells connected in series. Each delay line produces at its output a replica of the signal present at its input, shifted in time. The delay lines are matched and share the same compensation signals, which minimizes line-to-line delay deviations over temperature and supply voltage variations.

INPUT SIGNAL CHARACTERISTICS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a **Recommended Maximum** and an **Absolute Maximum** operating input frequency and a **Recommended Minimum** and an **Absolute Minimum** operating pulse width have been specified.

OPERATING FREQUENCY

The **Absolute Maximum Frequency** specification, tabulated in Table 1, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The **Recommended Maximum Frequency** specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed. To guarantee the Table 1 delay accuracy for input frequencies higher than the Recommended Maximum Frequency, the 3D3314 must be tested at the user operating frequency. Therefore, to facilitate production and device identification, the part number will include a custom reference designator identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

OPERATING PULSE WIDTH

The **Absolute Minimum Pulse Width** (high or low) specification, tabulated in Table 1, determines the smallest Pulse Width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The **Recommended Minimum Pulse Width** (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in Table 1 is guaranteed.

To guarantee the Table 1 delay accuracy for input pulse width smaller than the Recommended Minimum Pulse Width, the 3D3314 must be tested at the user operating pulse width. Therefore, to facilitate production and device identification, the part number will include a custom reference designator identifying the

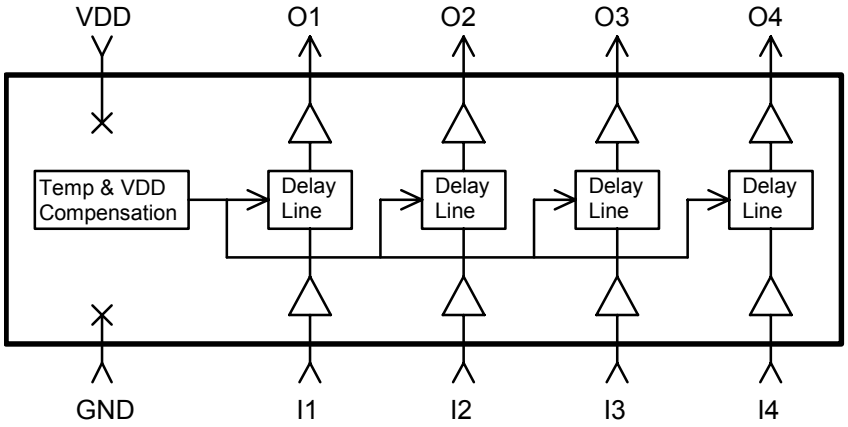


Figure 1: 3D3314 Functional Diagram

intended frequency and duty cycle of operation.

APPLICATION NOTES (CONT'D)

The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D3314 delay line utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature. The thermal coefficient is reduced to 200 PPM/C, which is equivalent to a variation, over the 0C-70C operating range, of ±1% or 0.25ns (whichever is greater) from the 25C delay settings. The power supply coefficient is reduced, over the 3.0V-3.6V operating range, to ±1% or 1ns (whichever is greater) of the delay settings at the nominal 3.3VDC power supply.

It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.

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DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-1.0	1.0	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(0C to 70C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		1.3	2.0	mA	V_{DD} = 3.6V
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}	-0.1	0.0	0.1	µA	V_{IH} = V_{DD}
Low Level Input Current	I_{IL}	-0.1	0.0	0.1	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-8.0	-6.0	mA	V_{DD} = 3.0V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	6.0	7.5		mA	V_{DD} = 3.0V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2		ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 4 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

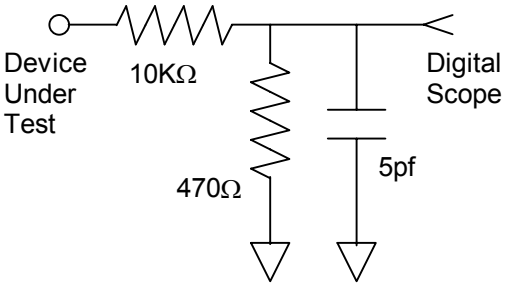
Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 3.3V ± 0.1V
Input Pulse: High = 3.3V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V
)
Pulse Width: PW_{IN} = 1.5 x Total Delay
Period: PER_{IN} = 3.0 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

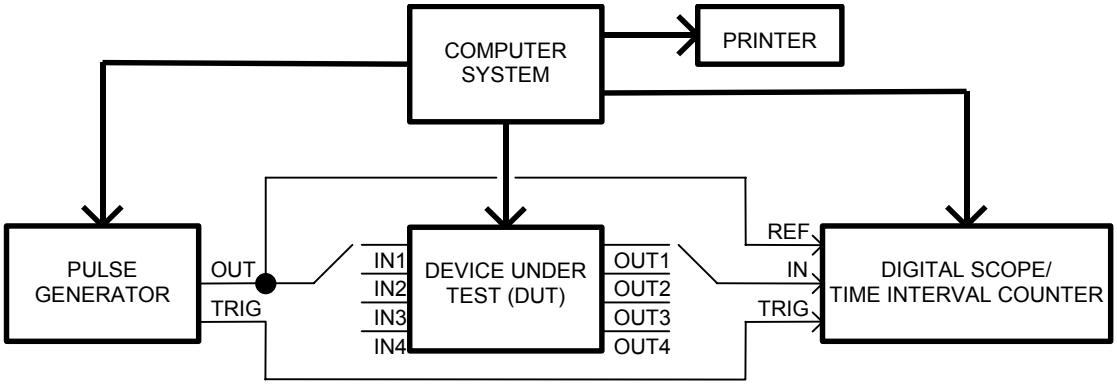


Figure 2: Test Setup

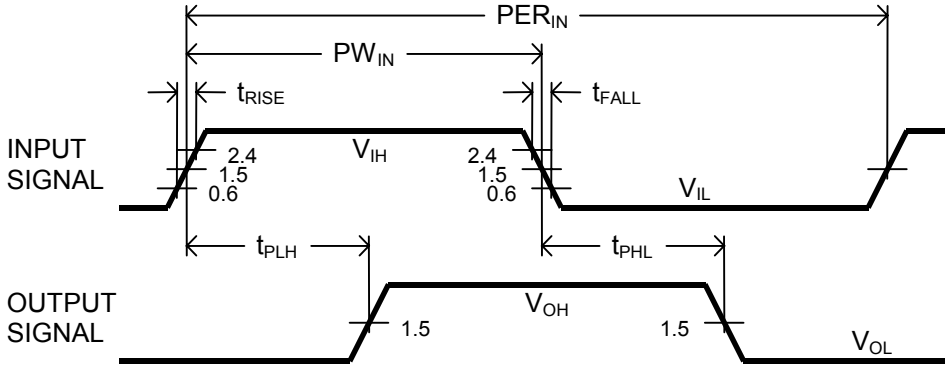


Figure 3: Timing Diagram