

Driver Transistors

MMBTA05L, MMBTA06L

NPN Silicon

Features

- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

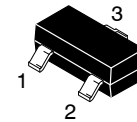
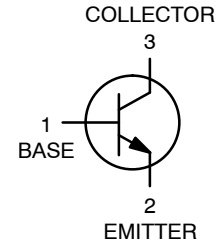
Rating	Symbol	Value	Unit
Collector – Emitter Voltage MMBTA05L MMBTA06L	V_{CEO}	60 80	Vdc
Collector – Base Voltage MMBTA05L MMBTA06L	V_{CBO}	60 80	Vdc
Emitter – Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Electrostatic Discharge	ESD	HBM Class 3B MM Class C CDM Class IV	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

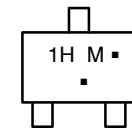
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

- FR-5 = $1.0 \times 0.75 \times 0.062$ in.
- Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.

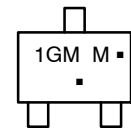


SOT-23
CASE 318
STYLE 6

MARKING DIAGRAM



MMBTA05LT1



MMBTA06LT1,
SMMBTA06L

1H, 1GM = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MMBTA05L, MMBTA06L

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (Note 3) ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	60 80	–	Vdc
Emitter–Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)	I_{CES}	–	0.1	μAdc
Collector Cutoff Current ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$)	I_{CBO}	– –	0.1 0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 10\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 100\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	100 100	– –	–
Collector–Emitter Saturation Voltage ($I_C = 100\text{ mAdc}$, $I_B = 10\text{ mAdc}$)	$V_{CE(sat)}$	–	0.25	Vdc
Base–Emitter On Voltage ($I_C = 100\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	$V_{BE(on)}$	–	1.2	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain–Bandwidth Product (Note 4) ($I_C = 10\text{ mA}$, $V_{CE} = 2.0\text{ V}$, $f = 100\text{ MHz}$)	f_T	100	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

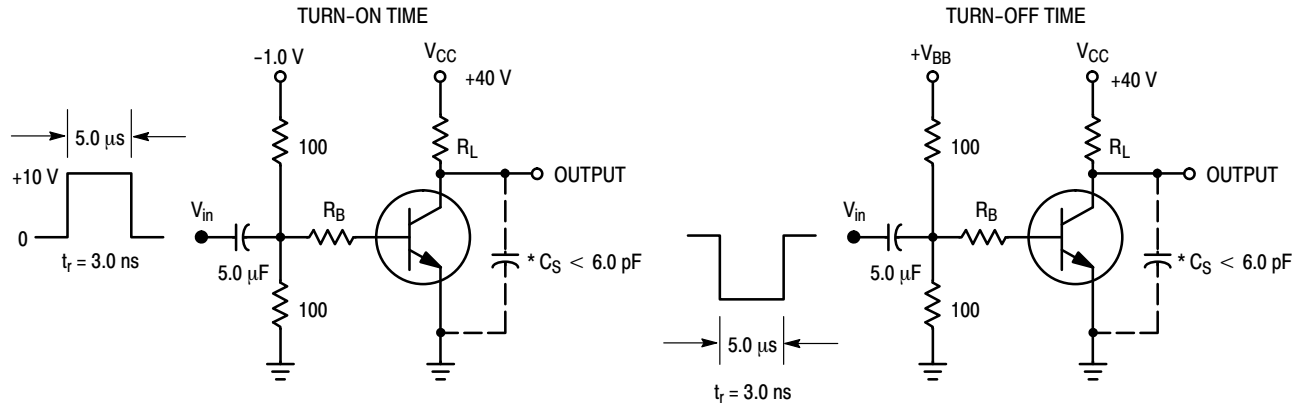


Figure 1. Switching Time Test Circuits

MMBTA05L, MMBTA06L

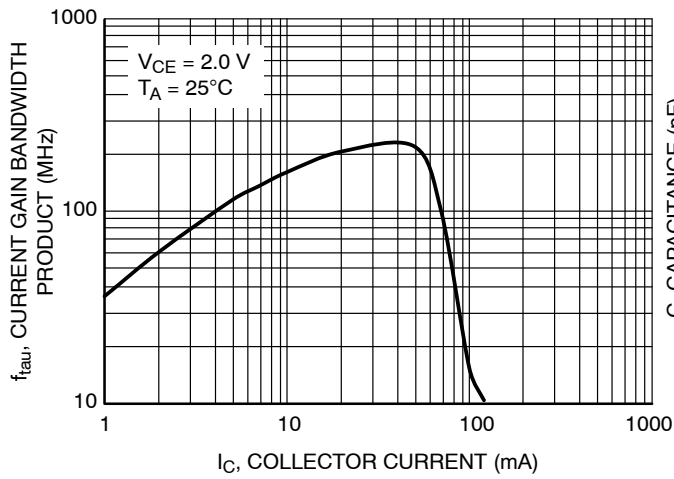


Figure 2. Current Gain Bandwidth Product vs. Collector Current

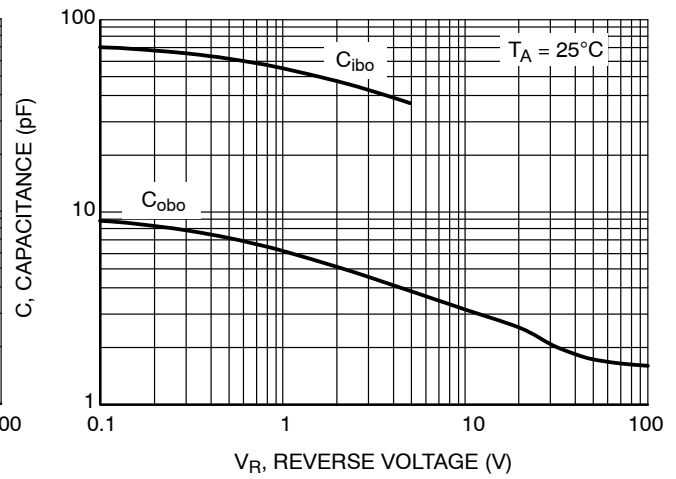


Figure 3. Capacitance

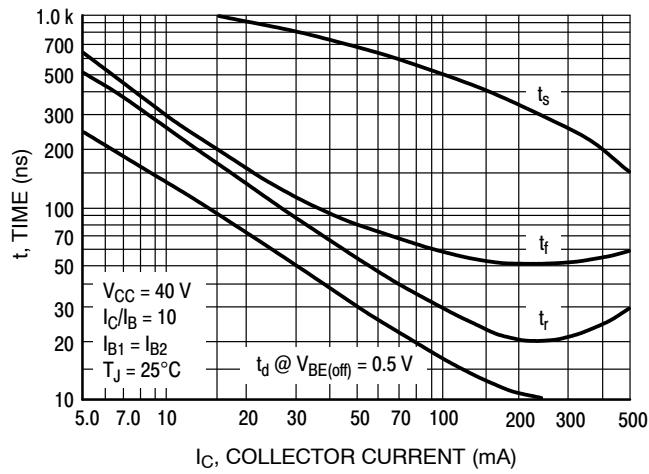


Figure 4. Switching Time

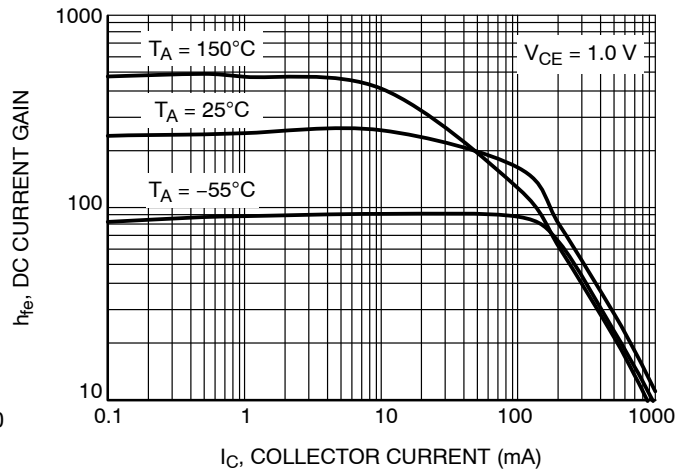


Figure 5. DC Current Gain vs. Collector Current

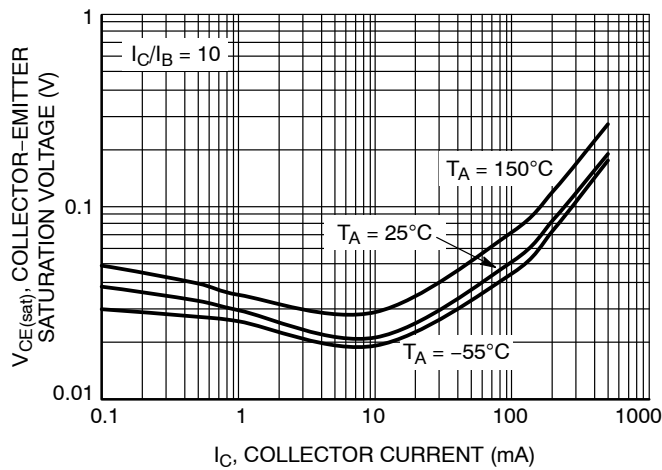


Figure 6. Collector Emitter Saturation Voltage vs. Collector Current

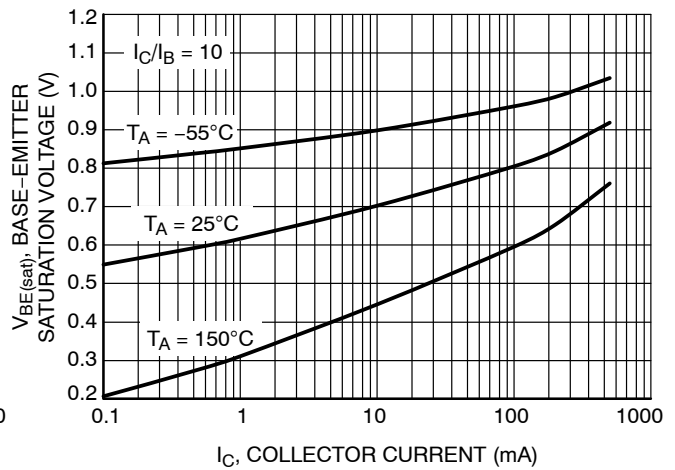


Figure 7. Base Emitter Saturation Voltage vs. Collector Current

MMBTA05L, MMBTA06L

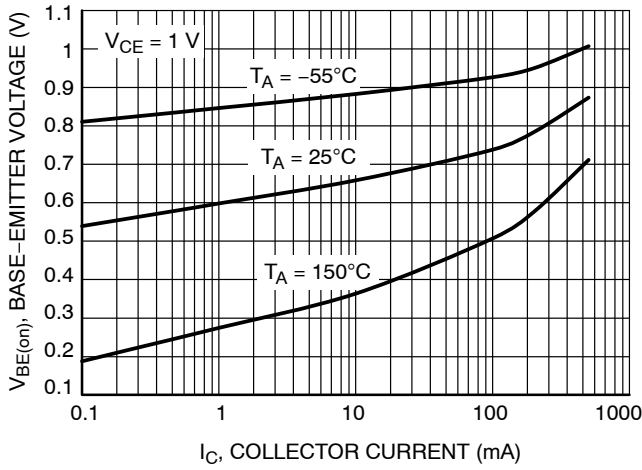


Figure 8. Base-Emitter Turn-ON Voltage vs. Collector Current

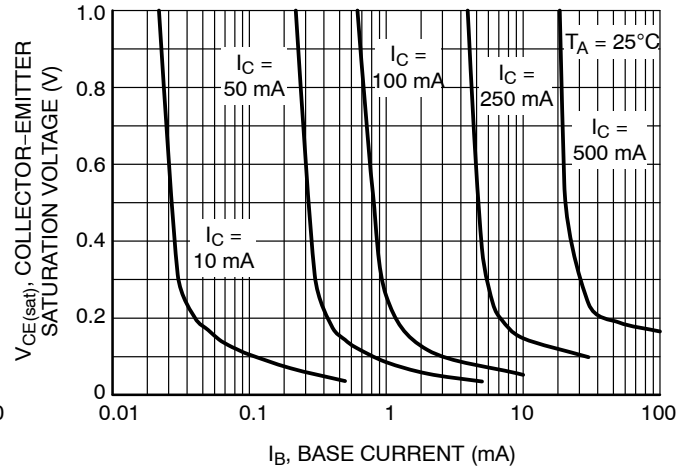


Figure 9. Saturation Region

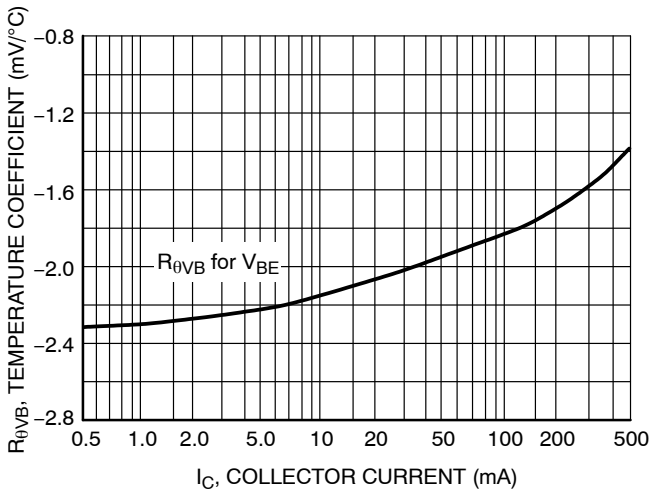


Figure 10. Base-Emitter Temperature Coefficient

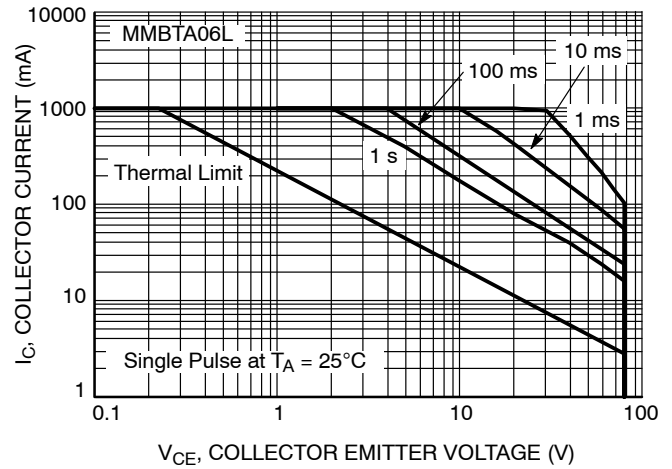


Figure 11. Safe Operating Area

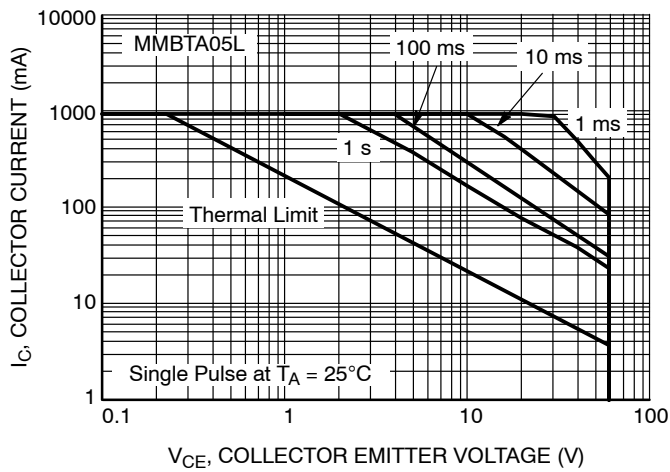


Figure 12. Safe Operating Area

MMBTA05L, MMBTA06L

ORDERING INFORMATION

Device	Package	Shipping†
MMBTA05LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
NSVMMBTA05LT1G*	SOT-23 (Pb-Free)	3,000 / Tape & Reel
MMBTA05LT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel
MMBTA06LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
SMMBTA06LT1G*	SOT-23 (Pb-Free)	3,000 / Tape & Reel
MMBTA06LT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel
SMMBTA06LT3G*	SOT-23 (Pb-Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DATE 14 AUG 2024

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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