National Semiconductor

MICROCIRCUIT DATA SHEET

MNCD40161BM-X REV 2A0

Original Creation Date: 10/06/95
Last Update Date: 08/24/98
Last Major Revision Date: 07/27/98

BINARY COUNTER WITH ASYNCHRONOUS CLEAR

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of QA and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Industry Part Number

CD40161BM

NS Part Numbers

CD40161BMJ/883

Prime Die

U161

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45Vdd (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14161B
- Equivalent to MM74C161

(Absolute Maximum Ratings)

(Note 1, 2)

DC Supply Voltage (Vdd)	-0.5 to +18Vdc
Input Voltage (Vin)	-0.5V to Vdd +0.5Vdc
Storage Temperature Range (Ts)	-65 C to +150 C
Power Dissipation (Pd)	
Dual-In-Line	700mW
Small Outline	500mW
Lead Temperature (Soldering, 10 seconds)	260 C

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of Recommended Operating Conditions and Electrical Characteristics provides conditions for actual device operation.
Note 2: Vss = 0V unless otherwise specified.

Recommended Operating Conditions

(Note 1)

DC Supply Voltage (Vdd)	3V to 15Vdc
Input Voltage (Vin)	0 to Vdd Vdc
Operating Temperature Range (TA)	
CD40161BM	-55 C to +125 C

Note 1: Vss = 0V unless otherwise specified.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IDD	Quiescent Device Current	Vcc = 5V		VDD		5	uA	1, 3
				VDD		150	uA	2
		Vcc = 10V		VDD		10	uA	1, 3
				VDD		300	uA	2
		Vcc = 15V		VDD		20	uA	1, 3
				VDD		600	uA	2
Iin	Input Current	Vcc = 15V, Vin = 0V		INPUTS		-100	nA	1, 3
				INPUTS		-1000	nA	2
		Vcc = 15V, Vin = 15V		INPUTS		100	nA	1, 3
				INPUTS		1000	nA	2
VOL	Logical "0" Output Voltage	Vcc = 5V, |IO| < 1uA		OUTPUTS		.05	V	1, 2, 3
		Vcc = 10V, |IO| < 1uA		OUTPUTS		.05	V	1, 2, 3
		Vcc = 15V, |IO| < 1uA		OUTPUTS		.05	V	1, 2, 3
VOH	Logical "1" Output Voltage	Vcc = 5V, |IO| < 1uA		OUTPUTS	4.95		V	1, 2, 3
		Vcc = 10V, |IO| < 1uA		OUTPUTS	9.95		V	1, 2, 3
		Vcc = 15V, |IO| < 1uA		OUTPUTS	14.95		V	1, 2, 3
IOL	Logical "0" Output Current	Vcc = 5V, Vout = .4V		OUTPUTS	510		uA	1
				OUTPUTS	360		uA	2
				OUTPUTS	640		uA	3
		Vcc = 10V, Vout = .5V		OUTPUTS	1.3		mA	1
				OUTPUTS	0.9		mA	2
				OUTPUTS	1.6		mA	3
		Vcc = 15V, Vout = 1.5V		OUTPUTS	3.4		mA	1
				OUTPUTS	2.4		mA	2
				OUTPUTS	4.2		mA	3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IOH	Logical "1" Output Current	Vcc = 5V, Vout = 4.6V		OUTPUTS	-510		uA	1
				OUTPUTS	-360		uA	2
				OUTPUTS	-640		uA	3
		Vcc = 10V, Vout = 9.5V		OUTPUTS	-1.3		mA	1
				OUTPUTS	-0.9		mA	2
				OUTPUTS	-1.6		mA	3
		Vcc = 15V, Vout = 13.5V		OUTPUTS	-3.4		mA	1
				OUTPUTS	-2.4		mA	2
				OUTPUTS	-4.2		mA	3
VIL	Logical "0" Input Voltage	VCC = 5.0V, VO = 0.5V or 4.5V	1	INPUTS		1.5	V	1, 2, 3
		VCC = 10.0V, VO = 1V or 9V	1	INPUTS		3	V	1, 2, 3
		VCC = 15.0V, VO = 1.5V or 13.5V	1	INPUTS		4	V	1, 2, 3
VIH	Logical "1" Input Voltage	VCC = 5.0V, VO = 0.5V or 4.5V	1	INPUTS	3.5		V	1, 2, 3
		VCC = 10.0V, VO = 1V or 9V	1	INPUTS	7		V	1, 2, 3
		VCC = 15.0V, VO = 1.5V or 13.5V	1	INPUTS	11		V	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Cl = 50pF, Rl = 200K

tPLH	Propagation Delay Time: Clock to Q	Vdd = 5V	3			400	nS	9
			3			500	nS	10, 11
		Vdd = 10V	3			160	nS	9
			3			200	nS	10, 11
		Vdd = 15V	2			130	nS	9
tPHL	Propagation Delay Time: Clock to Q	Vdd = 5V	3			400	nS	9
			3			500	nS	10, 11
		Vdd = 10V	3			160	nS	9
			3			200	nS	10, 11
		Vdd = 15V	2			130	nS	9

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Cl = 50pF, Rl = 200K

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHL	Propagation Delay Time: Clock to Carry Out	Vdd = 5V	3			450	nS	9
			3			562	nS	10, 11
		Vdd = 10V	3			190	nS	9
			3			237	nS	10, 11
		Vdd = 15V	2			160	nS	9
tPLH	Propagation Delay Time: Clock to Carry Out	Vdd = 5V	3			450	nS	9
			3			562	nS	10, 11
		Vdd = 10V	3			190	nS	9
			3			237	nS	10, 11
		Vdd = 15V	2			160	nS	9
tPLH	Propagation Delay Time: T Enable to Carry Out	Vdd = 5V	3			290	nS	9
			3			362	nS	10, 11
		Vdd = 10V	3			130	nS	9
			3			162	nS	10, 11
		Vdd = 15V	2			110	nS	9
tPHL	Propagation Delay Time: T Enable to Carry Out	Vdd = 5V	3			290	nS	9
			3			362	nS	10, 11
		Vdd = 10V	3			130	nS	9
			3			162	nS	10, 11
		Vdd = 15V	2			110	nS	9
tPHL	Propagation Delay Time: Clear To Q	Vdd = 5V	3			300	nS	9
			3			375	nS	10, 11
		Vdd = 10V	3			150	nS	9
			3			187	nS	10, 11
		Vdd = 15V	2			120	nS	9
tSU	SET UP TIME: Clock to Enable P or T	Vdd = 5V	1			280	nS	9
		Vdd = 10V	1			120	nS	9
		Vdd = 15V	2			100	nS	9
tSU	SET UP TIME: Clock to Data or Load	Vdd = 5V	1			335	nS	9

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Cl = 50pF, Rl = 200K

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
FMAX	Maximum Clock Frequency	Vdd = 5V	1		2		MHz	9
		Vdd = 10V	1		5.5		MHz	9
		Vdd = 15V	2		7		MHz	9
tWL	Maximum Clock Pulse Width	Vdd = 5V	1			250	nS	9
		Vdd = 10V	1			90	nS	9
		Vdd = 15V	2			70	nS	9
tWH	Maximum Clock Pulse Width	Vdd = 5V	1			250	nS	9
		Vdd = 10V	1			90	nS	9
		Vdd = 15V	2			70	nS	9
tRLC	Maximum Clock Rise Time	Vdd = 5V	2			15	uS	9
		Vdd = 10V	2			5	uS	9
		Vdd = 15V	2			5	uS	9
tFLC	Maximum Clock Fall Time	Vdd = 5V	2			15	uS	9
		Vdd = 15V	2			5	uS	9
tTLH	Transition Time (all outputs)	Vdd = 5V	3			200	nS	9
			3			250	nS	10, 11
		Vdd = 10V	3			100	nS	9
			3			125	nS	10, 11
		Vdd = 15V	2			80	nS	9
tTHL	Transition Time (all outputs)	Vdd = 5V	3			200	nS	9
			3			250	nS	10, 11
		Vdd = 10V	3			100	nS	9
			3			125	nS	10, 11
		Vdd = 15V	2			80	nS	9
Cin	Input Capacitance	Any Input	2			7.5	pF	9

Note 1: Parameter tested go-no-go only.
Note 2: Guaranteed parameter, not tested.
Note 3: Tested at 25C; Guaranteed but not tested at +125C and -55C.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
2A0	M0002967	08/24/98	Donald B. Miller	1) Added tSU - set up time: clock to enable P or T, tSU - set up time: clock to data or load, tWL - maximum clock pulse width, tWH - maximum clock pulse width, tRLC - maximum clock rise time, tFLC - maximum clock fall time. 2) Deleted ordering code CD40161BMW/883.