



3.3V CMOS 18-BIT REGISTERED TRANSCEIVER

IDT74FCT163501A/C

FEATURES:

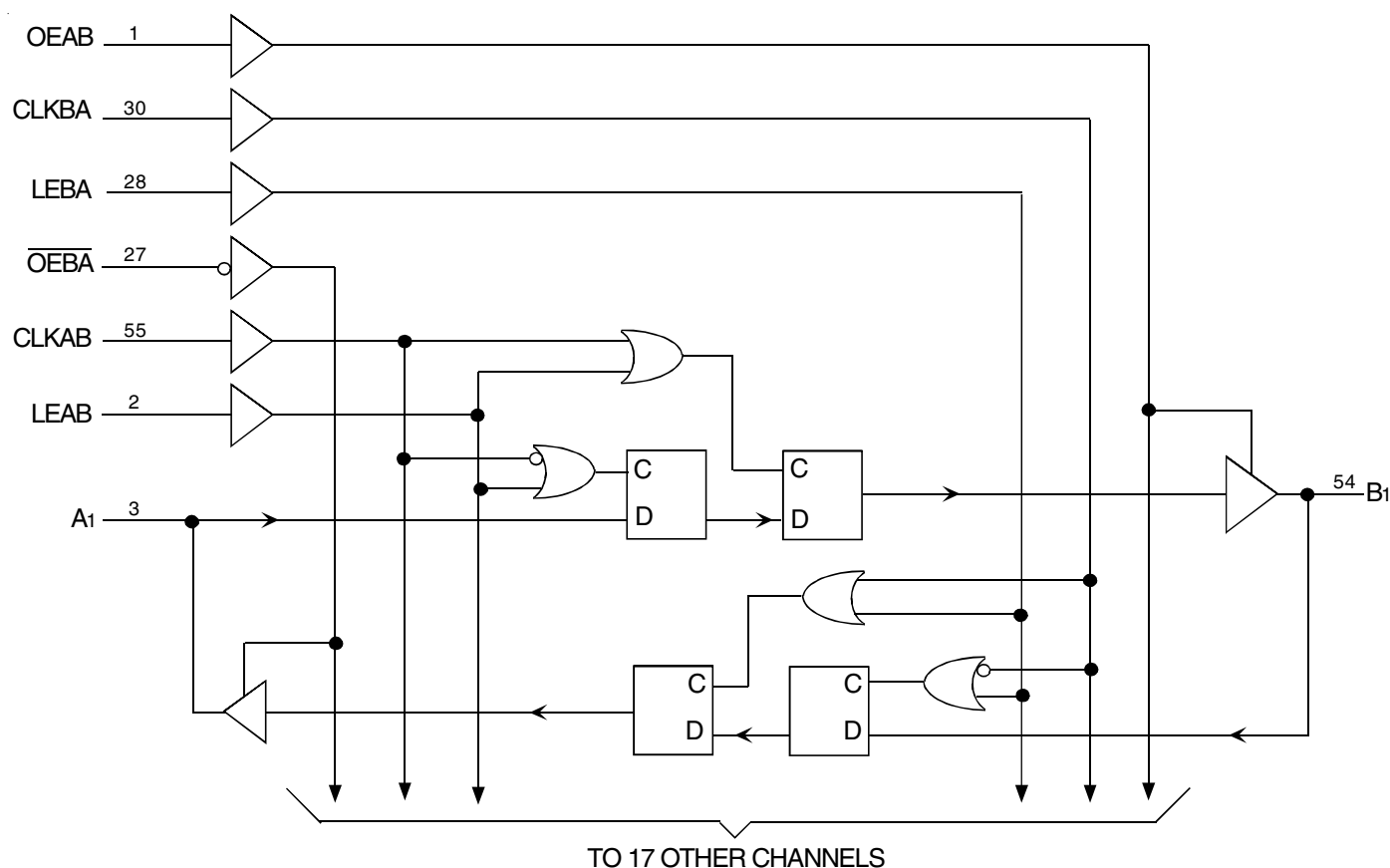
- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range, or $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components
- Available in SSOP, TSSOP, and TVSOP packages

DESCRIPTION:

The FCT163501 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable ($OEAB$ and $\overline{OEBA}$), latch enable ($LEAB$ and $LEBA$) and clock ($CLKAB$ and $CLKBA$) inputs. For A-to-B data flow, the device operates in transparent mode when $LEAB$ is high. When $LEAB$ is low, the A data is latched if $CLKAB$ is held at a high or low logic level. If $LEAB$ is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of $CLKAB$. $OEAB$ performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{OEBA}$, $LEBA$ and $CLKBA$. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163501 has series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM

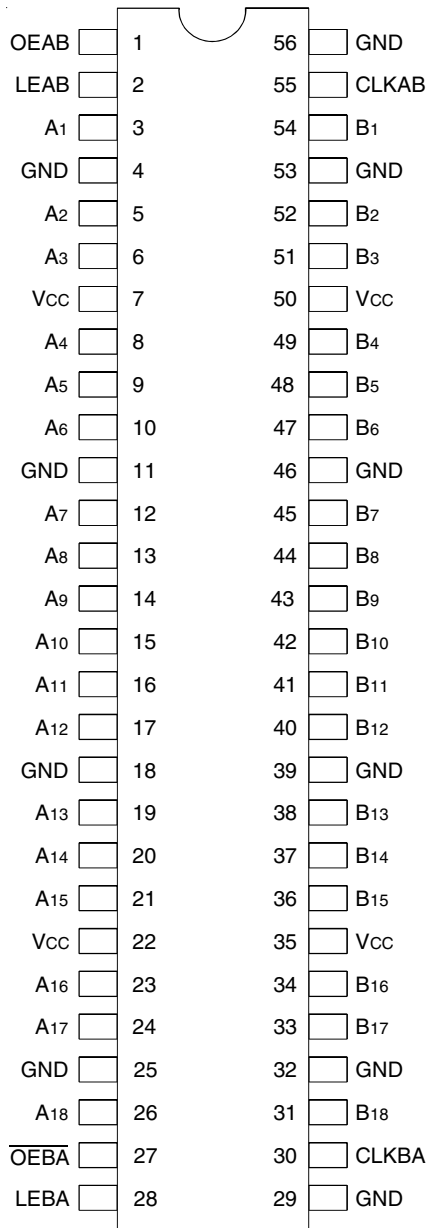


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INDUSTRIAL TEMPERATURE RANGE

APRIL 2002

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
$V_{\text{TERM}}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{\text{TERM}}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to 7	V
$V_{\text{TERM}}^{(4)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{\text{CC}}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $F = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	$V_{\text{IN}} = 0\text{V}$	3.5	6	pF
COUT	Output Capacitance	$V_{\text{OUT}} = 0\text{V}$	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	$\uparrow$	L	L
H	L	$\uparrow$	H	H
H	L	L	X	$B^{(2)}$
H	L	H	X	$B^{(3)}$

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
 $\uparrow$ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	$V_{CC}+0.5$	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.4	3	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -8\text{mA}$	2.4 ⁽⁵⁾	3	—	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$					
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.55	
		$V_{CC} = 3\text{V}$	$I_{OL} = 24\text{mA}$	—	0.3	0.5	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.1	10	μA

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC}-0.6\text{V}$ at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$		—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $OEAB = \overline{OEBA} = V_{CC} \text{ or GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (xCLKAB)}$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.6	1	
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (xCLKAB)}$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ $f_i = 2.5\text{MHz}$ 50% Duty Cycle Eighteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3	5 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	3	5.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

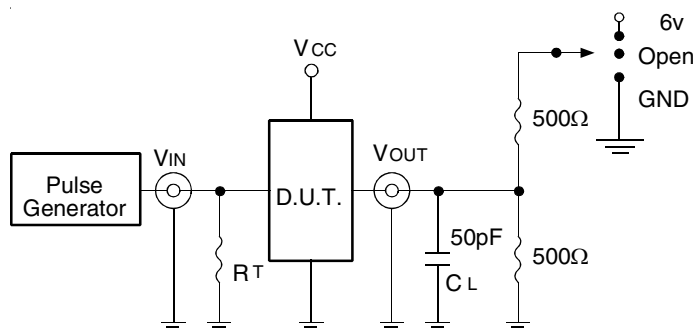
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Condition ⁽²⁾	FCT163501A		FCT163501C		Unit
			Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	
f _{MAX}	CLKAB or CLKBA frequency	CL = 50pF RL = 500Ω	—	150	—	150	ns
t _{PLH}	Propagation Delay		1.5	5.1	1.5	4.6	ns
t _{PHL}	Ax to Bx or Bx to Ax						
t _{PLH}	Propagation Delay		1.5	5.6	1.5	5.3	ns
t _{PHL}	LEBA to Ax, LEAB to Bx						
t _{PLH}	Propagation Delay		1.5	5.6	1.5	5.3	ns
t _{PHL}	CLKBA to Ax, CLKAB to Bx						
t _{PZH}	Output Enable Time		1.5	6	1.5	5.6	ns
t _{PZL}	$\overline{\text{OEBA}}$ to Ax, OEAB to Bx						
t _{PHZ}	Output Disable Time		1.5	5.6	1.5	5.2	ns
t _{PLZ}	$\overline{\text{OEBA}}$ to Ax, OEAB to Bx						
t _{SU}	Set-up Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		3	—	3	—	ns
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	ns
t _{SU}	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	3	—	3	—	ns
		Clock HIGH	1.5	—	1.5	—	
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	ns
t _w	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		3	—	3	—	ns
t _w	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾		3	—	3	—	ns
t _{sk(o)}	Output Skew ⁽⁵⁾		—	0.5	—	0.5	ns

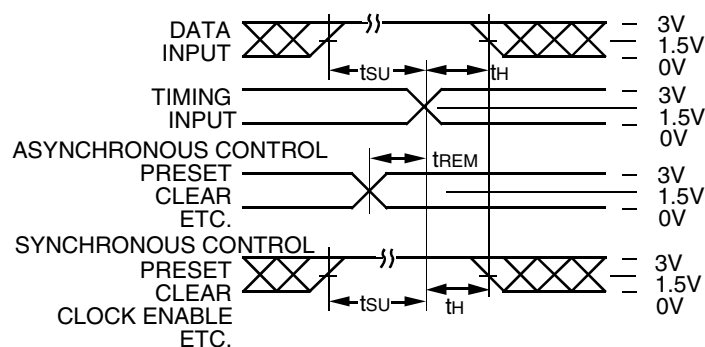
NOTES:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

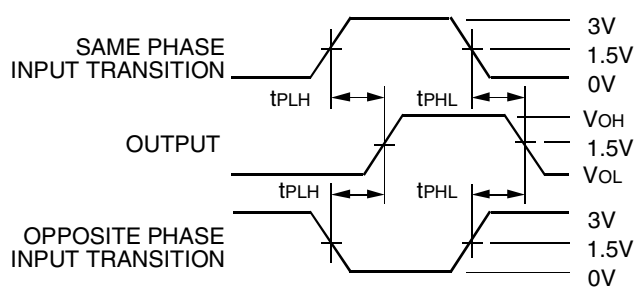
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

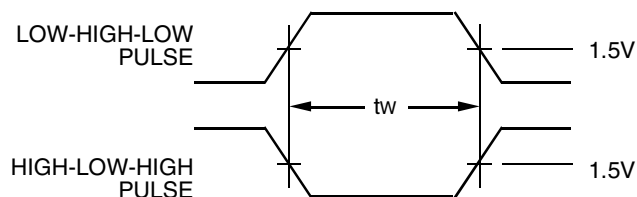
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

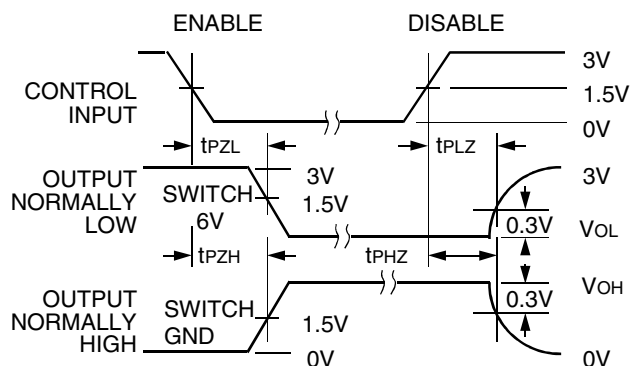
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
3. If VCC is below 3V, input voltage swings should be adjusted not to exceed VCC.

ORDERING INFORMATION

IDT	XX	FCT	XXX	XXXX	X	
Temp. Range	Family	Device Type	Package			
				PV PA PF	Shrink Small Outline Package Thin Shrink Small Outline Package Thin Very Small Outline Package	
			501A 501C	Non-Inverting 18-Bit Registered Transceiver		
			163	Double-Density 3.3Volt		
			74	– 40°C to +85°C		

DATA SHEET DOCUMENT HISTORY

4/22/2002 Removed blank speed grade



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459