

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)} \text{ max}$	I_D $T_A = +25^\circ\text{C}$
60V	140m Ω @ $V_{GS} = 10\text{V}$	2.3A
	170m Ω @ $V_{GS} = 4.5\text{V}$	2.1A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions
- Analog Switch

Features and Benefits

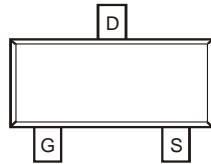
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

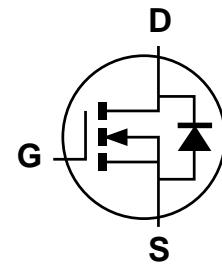
- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.0072 grams (Approximate)



Top View



Pin Configuration



Equivalent Circuit

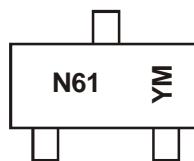
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN6140L-7	SOT23	3,000/Tape & Reel
DMN6140L-13	SOT23	10,000/Tape & Reel

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



N61 = Marking Code
 YM = Date Code Marking
 Y = Year (ex: Y = 2011)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017					
Code	Y	Z	A	B	C	D	E					
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	1.6 1.2	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	2.0 1.6	A
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	2.3 1.8	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	2.9 2.3	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	1.5	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	10	A

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.7	W
	$T_A = +70^\circ\text{C}$		0.4	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	183	°C/W
	$t < 10\text{s}$		115	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.3	W
	$T_A = +70^\circ\text{C}$		0.8	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	94	°C/W
	$t < 10\text{s}$		61	
Thermal Resistance, Junction to Case		$R_{\theta JC}$	39	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(\text{th})}$	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	92	140	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 1.8\text{A}$
			115	170		$V_{GS} = 4.5\text{V}, I_D = 1.3\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	2.2	—	S	$V_{DS} = 15\text{V}, I_D = 1.8\text{A}$
Diode Forward Voltage	V_{SD}	—	0.75	1.0	V	$V_{GS} = 0\text{V}, I_S = 0.45\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	315	—	pF	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	18	—		
Reverse Transfer Capacitance	C_{rss}	—	16	—		
Gate Resistnace	R_g	—	0.65	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	8.6	—	nC	$V_{DS} = 30\text{V}, I_D = 1.8\text{A}$
Total Gate Charge ($V_{GS} = 5\text{V}$)	Q_g	—	4.1	—		
Gate-Source Charge	Q_{gs}	—	1.0	—		
Gate-Drain Charge	Q_{gd}	—	1.7	—		
Turn-On Delay Time	$t_{D(\text{on})}$	—	2.6	—	ns	$V_{DS} = 30\text{V}, V_{GS} = 10\text{V}, R_g = 6.0\Omega, I_D = 1.8\text{A}$
Turn-On Rise Time	t_r	—	3.6	—		
Turn-Off Delay Time	$t_{D(\text{off})}$	—	16.3	—		
Turn-Off Fall Time	t_f	—	2.7	—		
Reverse Recovery Time	t_{rr}	—	16.8	—	ns	$I_F = 1.8\text{A}, \text{di}/\text{dt} = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}	—	9.0	—	nC	

Notes:

5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1in. square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

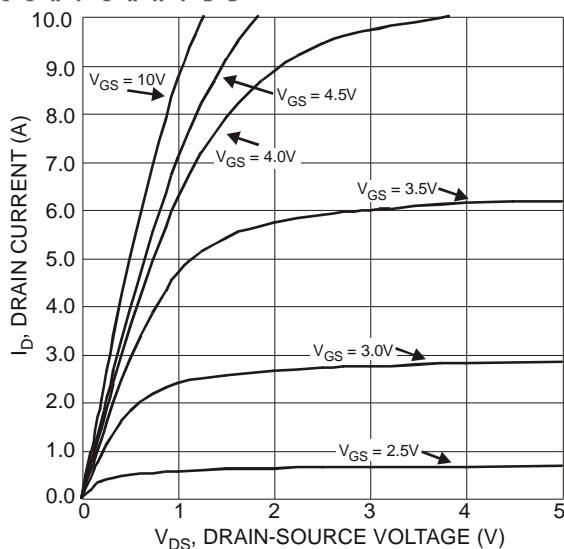


Figure 1 Typical Output Characteristic

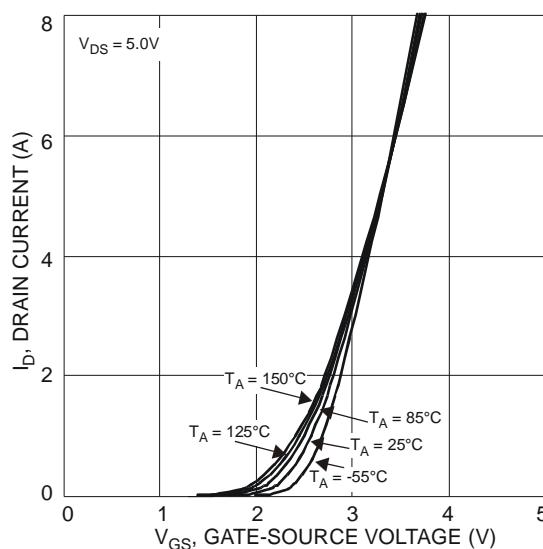


Figure 2 Typical Transfer Characteristics

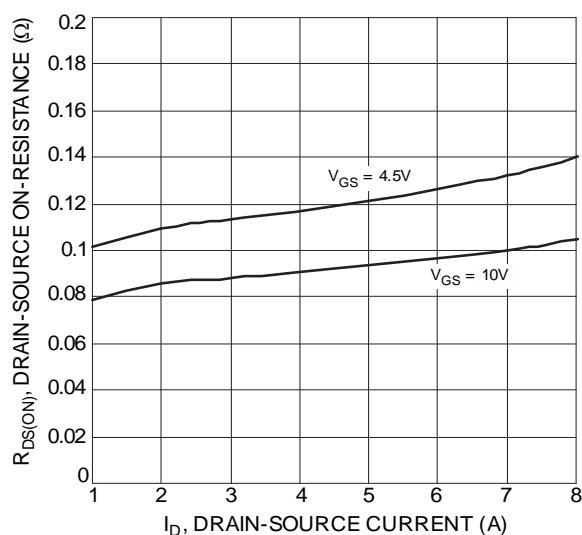


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

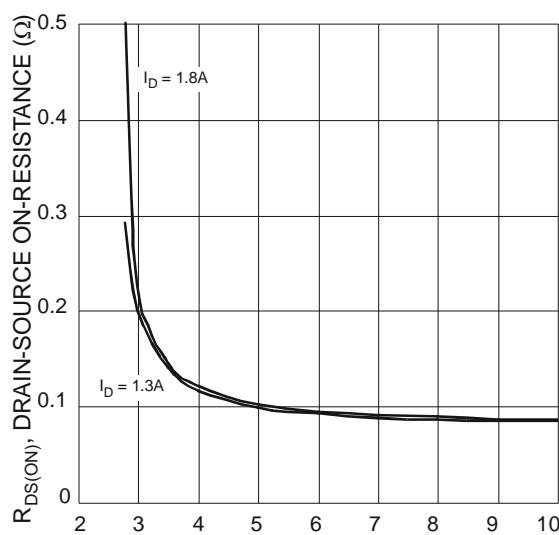


Figure 4 Typical Drain-Source On Resistance
vs. Gate-Source Voltage

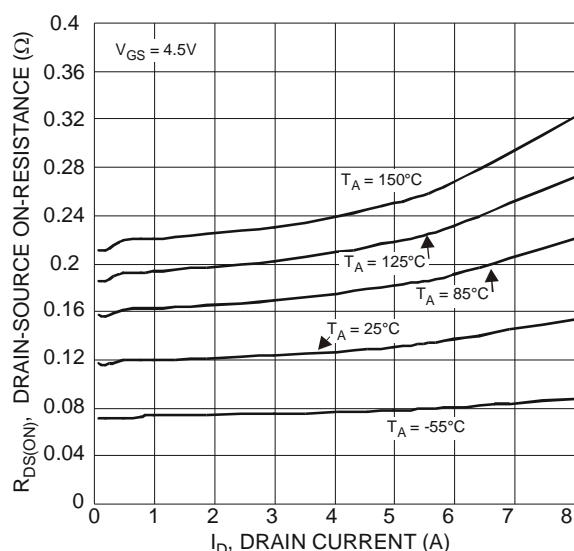


Figure 5 Typical On-Resistance vs.
Drain Current and Temperature

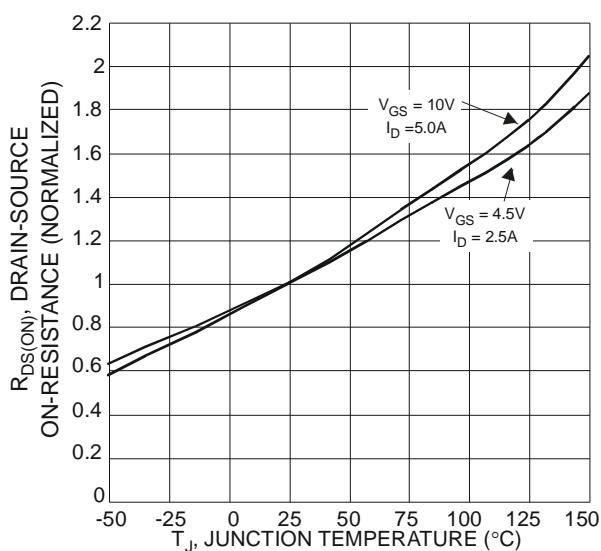


Figure 6 On-Resistance Variation with Temperature

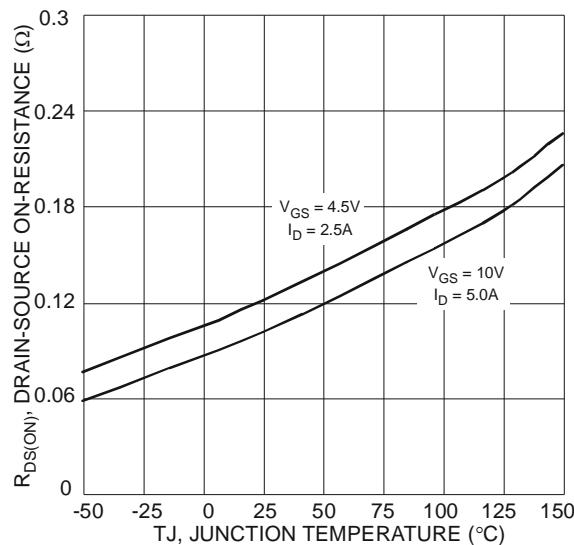


Figure 7 On-Resistance Variation with Temperature

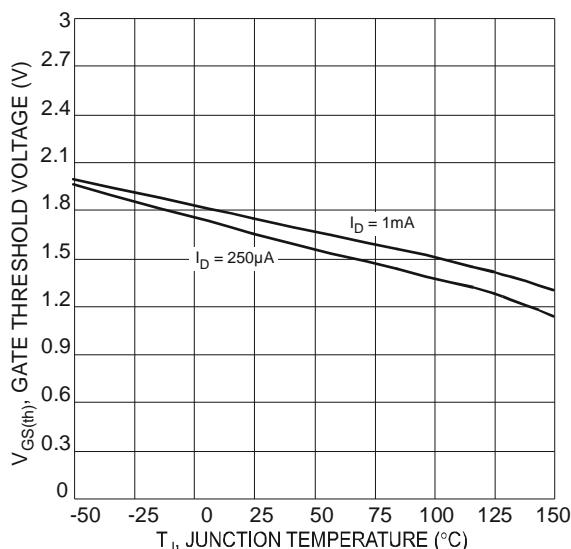


Figure 8 Gate Threshold Variation vs. Ambient Temperature

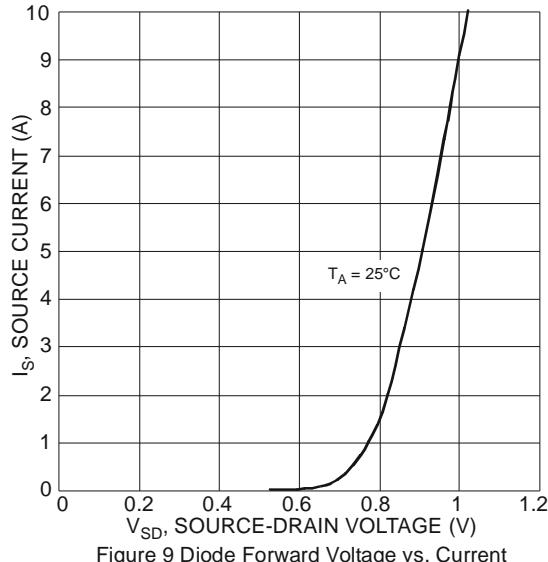


Figure 9 Diode Forward Voltage vs. Current

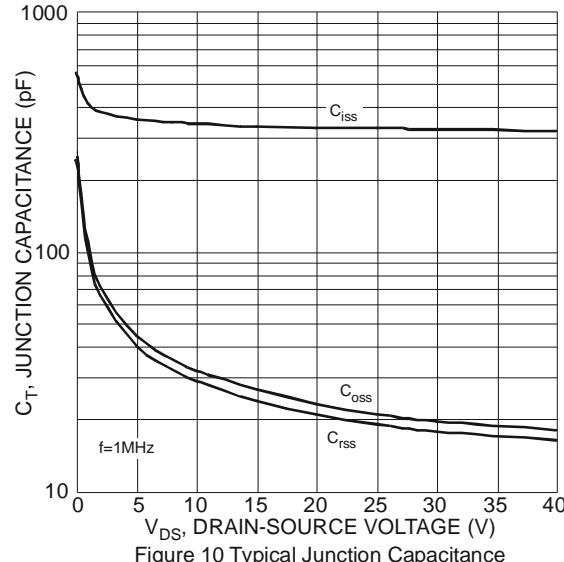


Figure 10 Typical Junction Capacitance

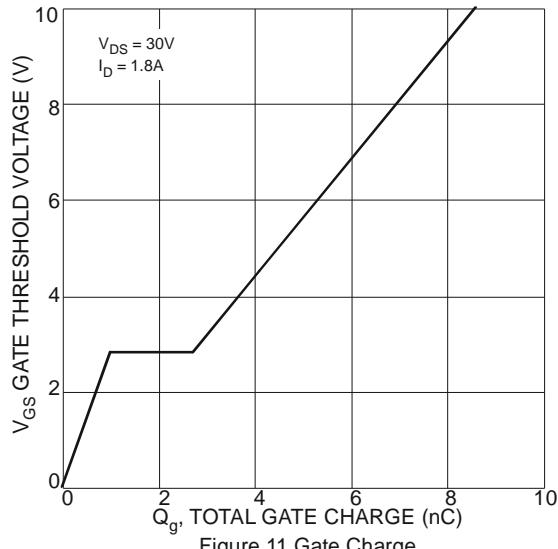


Figure 11 Gate Charge

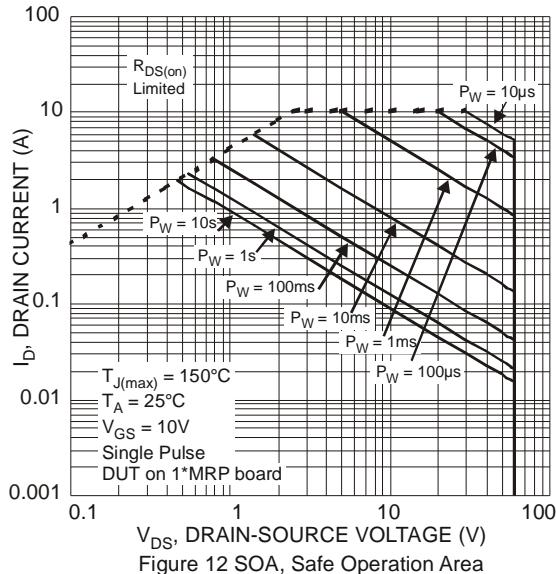
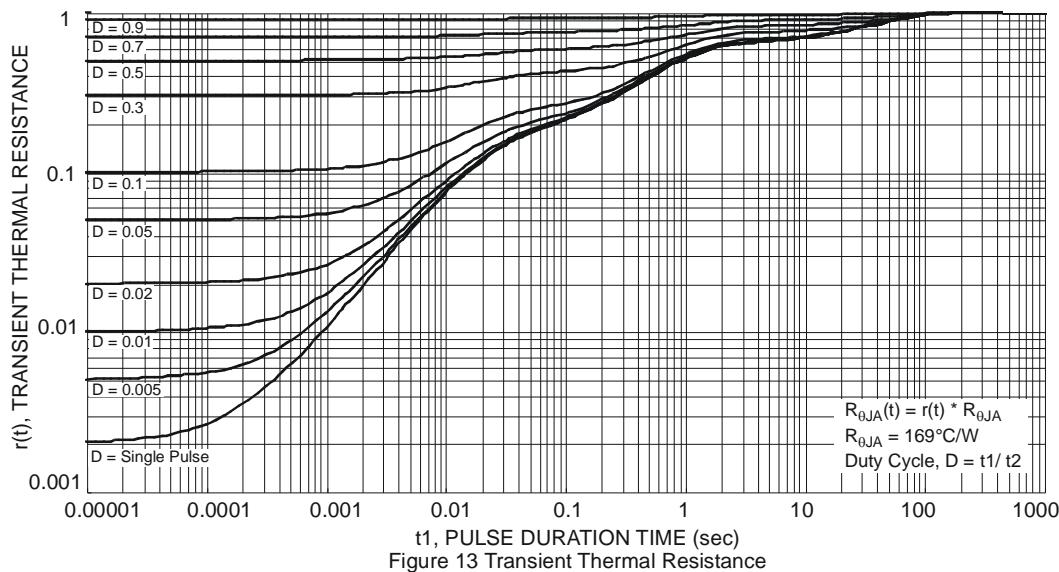
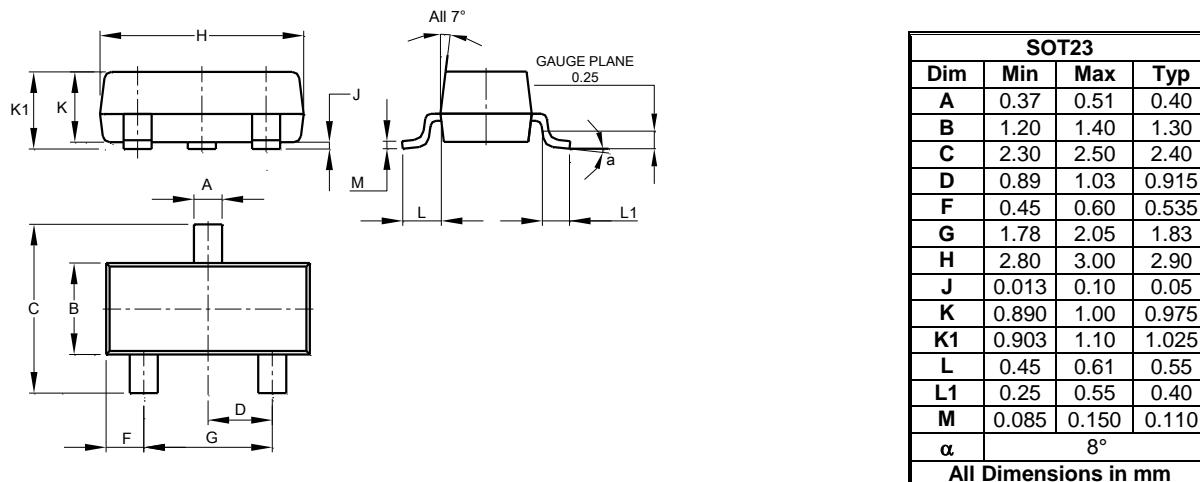


Figure 12 SOA, Safe Operation Area



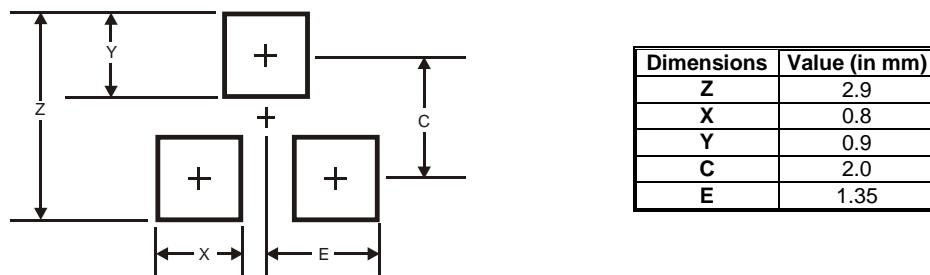
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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