STRUCTURE: Silicon Monolithic Integrated Circuit

PRODUCT NAME: 1ch DC／DC Converter Controller IC with Built-in Synchronous Rectifier

TYPE: **BD9120HFN**

FEATURES:
- Output Voltage：Adjustable(1.0～1.5V), Output Current：0.8A
- Low Operating Voltage
- High Efficiency and Fast Transient Response

○ABSOLUTE MAXIMUM RATING（Ta=25℃）

Parameter	Symbol	Limit	Unit
Supply Voltage	VCC	-0.3～+7 *1	V
	PVCC	-0.3～+7 *1	V
EN Voltage	EN	-0.3～+7	V
SW・ITH Voltage	SW, ITH	-0.3～+7	V
SW Output Current	Isw	1.1 *1	A
Power Dissipation 1	Pd1	1350 *2	mW
Power Dissipation 2	Pd2	1750 *3	mW
Operating Temperature Range	Topr	-25～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Pd, ASO, and Tjmax=150℃ should not be exceeded.
*2 Derating is 92.6℃/W for temperatures above Ta=25℃
(when mounted on 70mm×70mm×1.6mm glass epoxy PCB which has 1 layer (7%) of copper on the back side).
*3 Derating is 71.4℃/W for temperatures above Ta=25℃
(when mounted on 70mm×70mm×1.6mm glass epoxy PCB which has 1 layer (65%) of copper on the back side).

○OPERATING CONDITIONS（Ta=-25～+85℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	2.7	3.3	4.5	V
	PVCC	2.7	3.3	4.5	V
EN Voltage	EN	0	-	VCC	V
Output Voltage Range	VOUT	1.0	-	1.5	V
SW Average Output Current	Isw	-	-	0.8*4	A

*4 Pd and ASO should not be exceeded.

The product described in this specification is a strategic product (and/or Service) subject to COCOM regulations.
It may not be exported without proper authorization from the government with jurisdiction.
This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the formal specification. This translated version is exclusively intended as a reference, and may only be used as an auxiliary aid in reading the formal version. If there are any differences between the Japanese and translated versions of this document, the formal version takes priority.

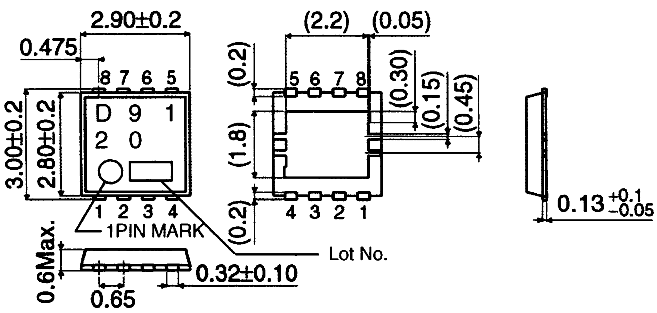
○ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃ VCC=PVCC=3.3V, EN=VCC, R_1=20kΩ, R_2=10kΩ)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Standby Current	ISTB	-	0	10	μA	EN=GND
Bias Current	ICC	-	200	400	μA	
EN Low Voltage	VENL	-	GND	0.8	V	Stand-by Mode
EN High Voltage	VENH	2.0	Vcc	-	V	Active Mode
EN Input Current	IEN	-	1	10	μA	VEN=3.3V
Oscillation Frequency	FOSC	0.8	1	1.2	MHz	
Pch FET ON Resistance*5	RONP	-	0.35	0.60	Ω	PVCC=3.3V
Nch FET ON Resistance*5	RONN	-	0.25	0.50	Ω	PVCC=3.3V
ADJ Reference Voltage	VADJ	0.780	0.800	0.820	V	
Output Voltage*5	VOUT	-	1.200	-	V	
ITH SINK Current	ITHSI	10	20	-	μA	VOUT =H
ITH Source Current	ITHSO	10	20	-	μA	VOUT =L
UVLO Threshold Voltage	VUVLO1	2.400	2.500	2.600	V	VCC=H→L
UVLO Release Voltage	VUVLO2	2.425	2.550	2.700	V	VCC=L→H
Soft Start Time	TSS	0.5	1	2	ms	
Timer Latch Time	TLATCH	1	2	3	ms	SCP/TSD Operational Mode
Output Short circuit Threshold Voltage	VSCP	-	VOUT×0.5	VOUT×0.7	V	VOUT=H→L

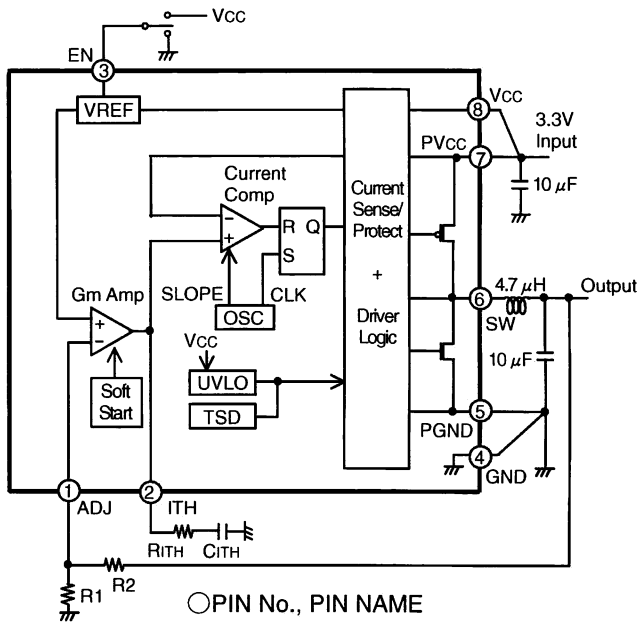
*5 Design Guarantee (Outgoing inspection is not performed on all products)

○PHYSICAL DIMENSION

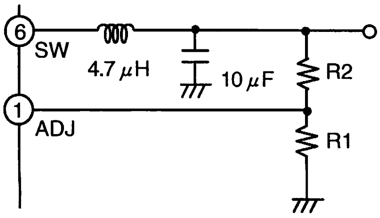


HSON8 (Unit:mm)

○BLOCK DIAGRAM・APPLICATION CIRCUIT



○SETTING THE OUTPUT VOLTAGE



The Output Voltage is set by the external resistor divider and is calculated as :

$Vout=(R2/R1+1) \times VADJ$ ・・・ ① VADJ : ADJ pin reference Voltage (0.8V typ)

It' s possible to adjust the output voltage by R1 and R2. (The Vout must be set from 1.0V to 1.5V.)
Resistance R1≒10kΩ is recommended. Please confirm the ripple voltage, if you can use the resistance more than 100kΩ.

○PIN No., PIN NAME

PIN No.	PIN Name
1	ADJ
2	ITH
3	EN
4	GND
5	PGND
6	SW
7	PVCC
8	VCC

○NOTES FOR USE

(1) Absolute maximum rating
Although the quality of this IC is rigorously controlled and will function properly in normal operating conditions, the IC may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because short mode or open mode cannot be specified when the IC is destroyed, it is important to take physical safety measures such as fusing if a special mode in excess of absolute rating limits is to be implemented.

(2) GND potential
Make sure the potential for the GND pin is always kept at the minimum, regardless of the operating mode. In addition, verify that the GND voltage is lower than the potential of all terminals except SW, PGND and GND in all conditions, including electric transient events.

(3) Thermal design
Do not exceed the power dissipation (Pd) of the package specification rating under actual operation. Provide sufficient margin in the thermal design to account for the Pd expected in actual use.

(4) Short-circuits between pins and incorrect mounting position
When mounting the IC onto the set PCB, be extremely careful about the orientation and position of the IC. The IC may be destroyed if it is incorrectly positioned for mounting. Do not short-circuit between pins, or between a pin and the power supply or ground terminal. Note that introducing foreign matter in these paths will cause shorts and may damage the IC.

(5) Operation in strong electromagnetic fields
Use in strong electromagnetic fields may cause malfunctions. Use extreme caution with electromagnetic fields.

(6) ASO (Area of Safe Operation)
Do not exceed the maximum ASO parameter or the absolute maximum ratings of the output driver.

(7) TSD (Thermal Shutdown) circuit
This product is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the IC chip temperature rises to the threshold value. In this case, TSD automatically latches output OFF. Output is restored when the EN block is activated again, or when UVLO is deactivated. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

(8) GND wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the standard point on the circuit set board) is recommended. This will separate the small-signal and high current patterns, and serves to ensure that the high current flow and wire impedance will not change the small-signal GND voltage. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(9) Operation in supply voltage range
Circuit functionality is guaranteed within the operating ambient temperature, as long as the operation is within the supply voltage range. The standard electrical characteristics cannot be guaranteed.
However, any variation in these values will be small, as long as the operation is within the supply voltage range.

(10) The application schematic presented above is an example of recommended circuit layout. Although the circuit example is sound, actual circuit characteristics should be checked carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the Vcc and PVcc pins, and a Schottky barrier diode established between the SW and PGND pins.

(11) Overcurrent protection circuit/Output short protection circuit

The overcurrent protection circuit is built into output, and functions as the current limit.

Note that if the protection circuit operates more than a specified time period (when the output short-circuit protection circuit detects a load short or other similar state) the output will be latched OFF.

Output is restored when the EN block is activated again, or when UVLO is deactivated. Although the protection circuits effectively prevent IC destruction under fault conditions, they should not be employed continuously.

(12) Selection of inductor

Please use an inductor with a series resistance element (DCR) under 0.2Ω. Note that use of a high DCR inductor will cause an inductor loss, resulting in decreased voltage output. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.2Ω, be careful to ensure adequate margins for variation between eternal devices and this IC, including transient as well as static characteristics.

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