

HUFA76413DK8T_F085

N-Channel Logic Level UltraFET® Power MOSFET 60V, 4.8A, 56mΩ

General Description

These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching convertors, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

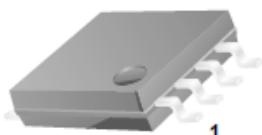


Applications

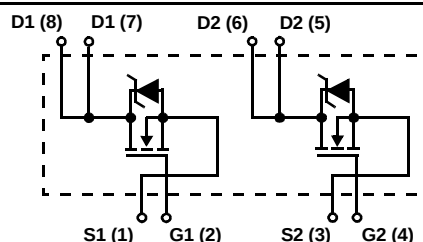
- Motor and Load Control
- Powertrain Management

Features

- 150°C Maximum Junction Temperature
- UIS Capability (Single Pulse and Repetitive Pulse)
- Ultra-Low On-Resistance $r_{DS(ON)} = 0.049\Omega$, $V_{GS} = 10V$
- Ultra-Low On-Resistance $r_{DS(ON)} = 0.056\Omega$, $V_{GS} = 5V$
- Qualified to AEC Q101
- RoHS Compliant



SO-8



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 16	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$)	5.1	A
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 5V$)	4.8	A
	Continuous ($T_C = 125^\circ\text{C}$, $V_{GS} = 5V$, $R_{\theta JA} = 228^\circ\text{C/W}$)	1	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	260	mJ
P_D	Power dissipation	2.5	W
	Derate above 25°C	0.02	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient SO-8 (Note 2)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SO-8 (Note 3)	191	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SO-8 (Note 4)	228	$^\circ\text{C/W}$

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
76413DK8	HUFA76413DK8T_F085	SO-8	330mm	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{V}$ $V_{GS} = 0\text{V}$ $T_A = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 5.1\text{A}$, $V_{GS} = 10\text{V}$	-	0.041	0.049	Ω
		$I_D = 4.8\text{A}$, $V_{GS} = 5\text{V}$	-	0.048	0.056	
		$I_D = 4.8\text{A}$, $V_{GS} = 5\text{V}$ $T_A = 150^\circ\text{C}$	-	0.091	0.106	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	620	-	pF
C_{OSS}	Output Capacitance		-	180	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	30	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 30\text{V}$ $I_D = 4.8\text{A}$ $I_g = 1.0\text{mA}$	18	23	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V		10	13	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V		0.6	0.8	nC
Q_{gs}	Gate to Source Gate Charge			1.8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			5	-	nC

Switching Characteristics ($V_{GS} = 5\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 30\text{V}$, $I_D = 1\text{A}$ $V_{GS} = 5\text{V}$, $R_{GS} = 16\Omega$	-	-	44	ns
$t_{d(ON)}$	Turn-On Delay Time		-	10	-	ns
t_r	Rise Time		-	19	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	45	-	ns
t_f	Fall Time		-	27	-	ns
t_{OFF}	Turn-Off Time		-	-	108	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 4.8\text{A}$	-	-	1.25	V
		$I_{SD} = 2.4\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4.8\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	43	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 4.8\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	55	nC

Notes:

- 1: Starting $T_J = 25^\circ\text{C}$, $L = 20\text{mH}$, $I_{AS} = 5.1\text{A}$
- 2: $R_{\theta JA}$ is $50^\circ\text{C}/\text{W}$ when mounted on a 0.5in^2 copper pad on FR-4 at 1 second.
- 3: $R_{\theta JA}$ is $191^\circ\text{C}/\text{W}$ when mounted on a 0.027in^2 copper pad on FR-4 at 1000 seconds.
- 4: $R_{\theta JA}$ is $228^\circ\text{C}/\text{W}$ when mounted on a 0.006in^2 copper pad on FR-4 at 1000 seconds.

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

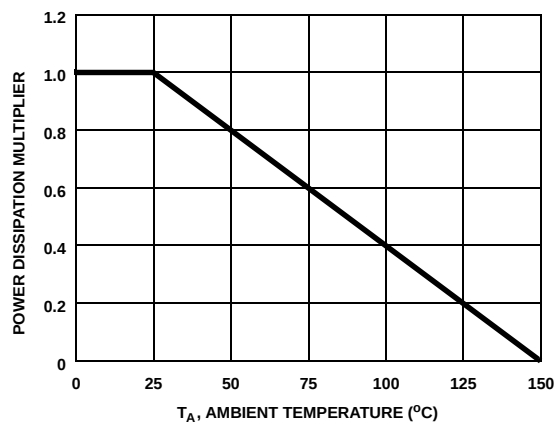


Figure 1. Normalized Power Dissipation vs Ambient Temperature

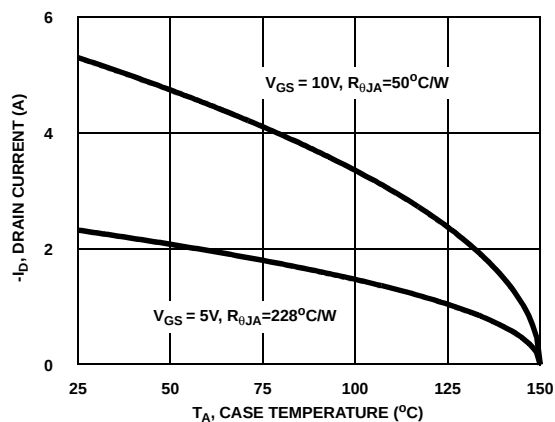


Figure 2. Maximum Continuous Drain Current vs Case Temperature

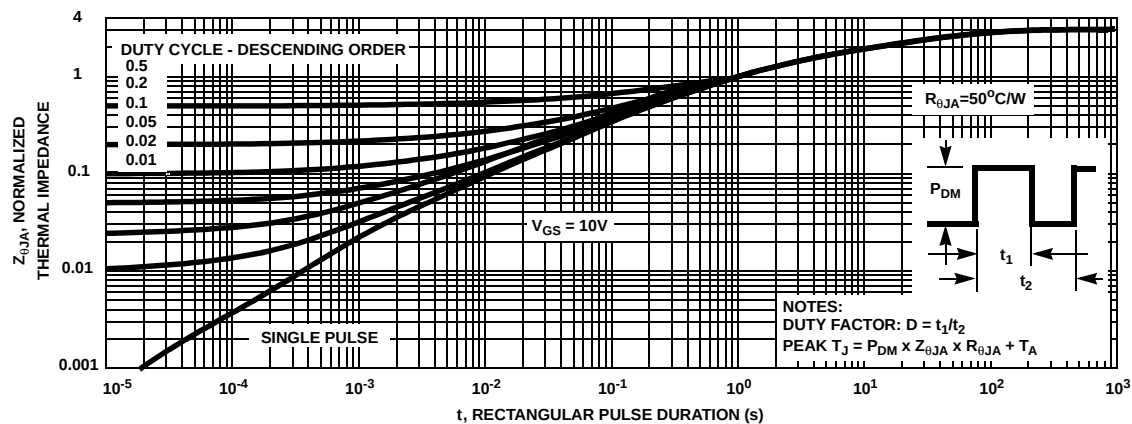


Figure 3. Normalized Maximum Transient Thermal Impedance

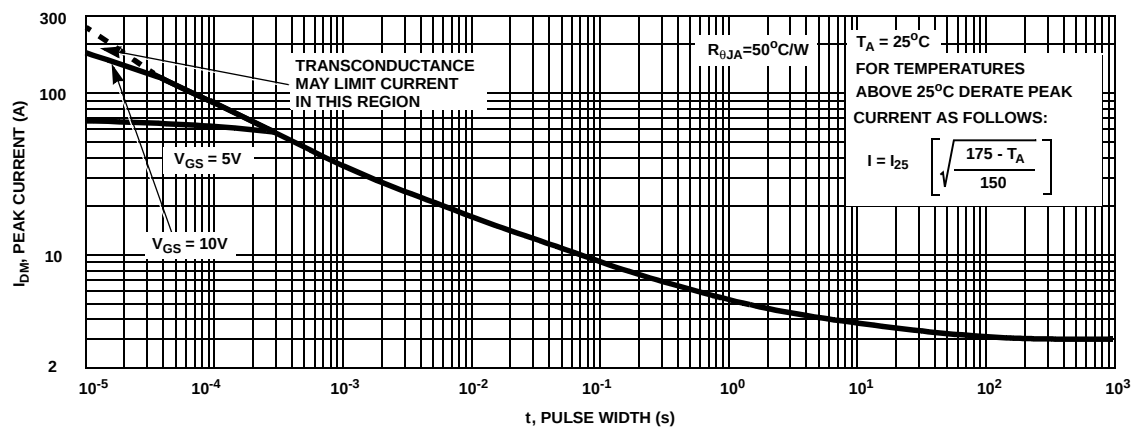


Figure 4. Peak Current Capability

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

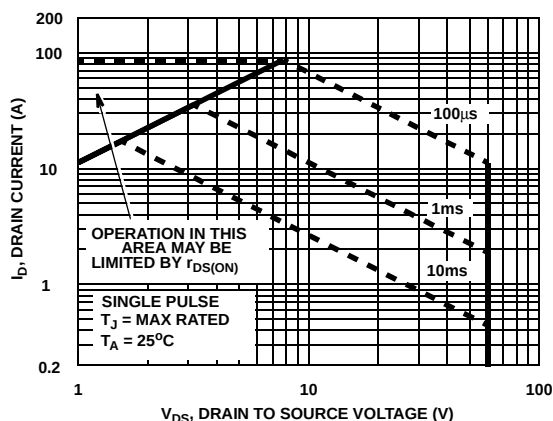


Figure 5. Forward Bias Safe Operating Area

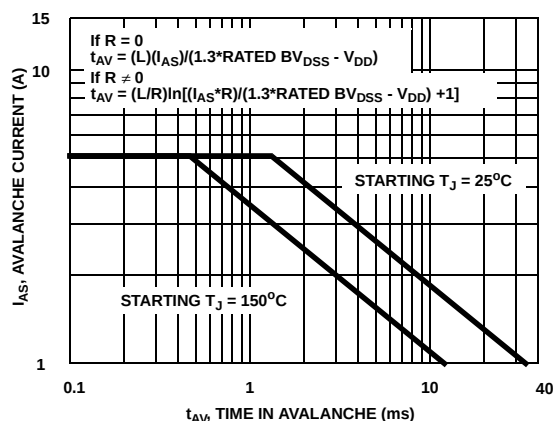


Figure 6. Unclamped Inductive Switching Capability

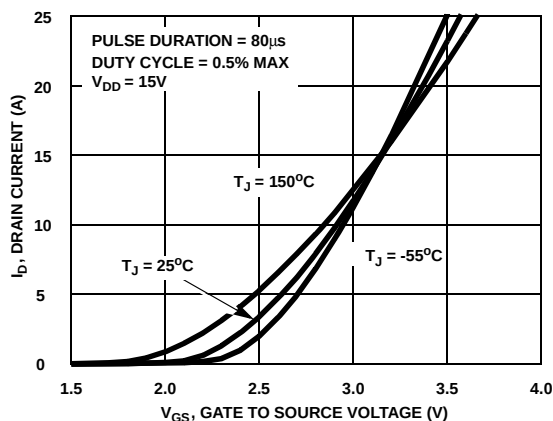


Figure 7. Transfer Characteristics

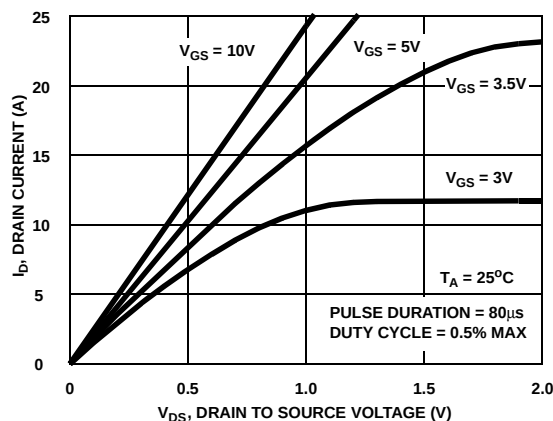


Figure 8. Saturation Characteristics

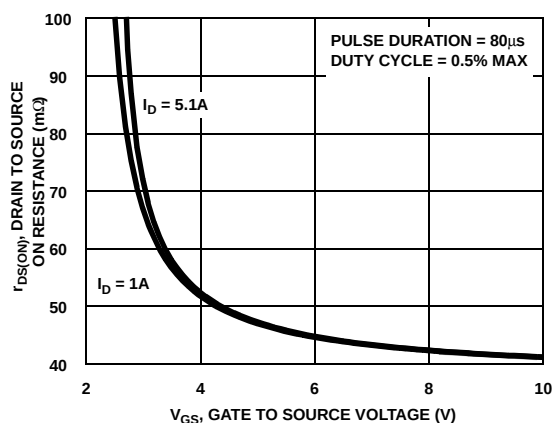


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

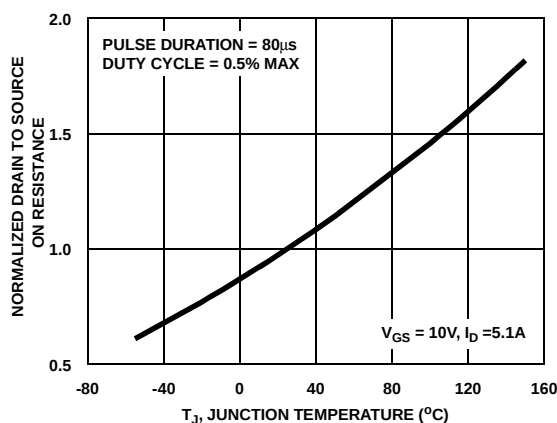


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

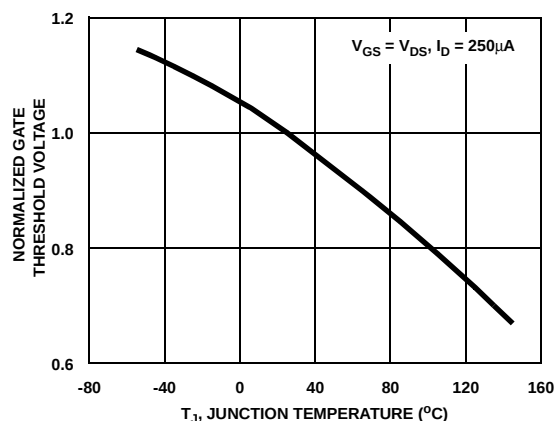


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

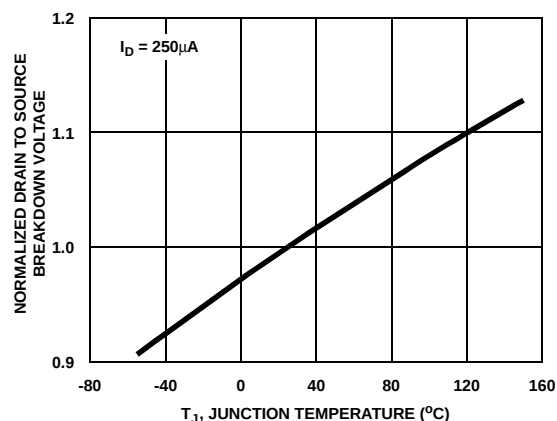


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

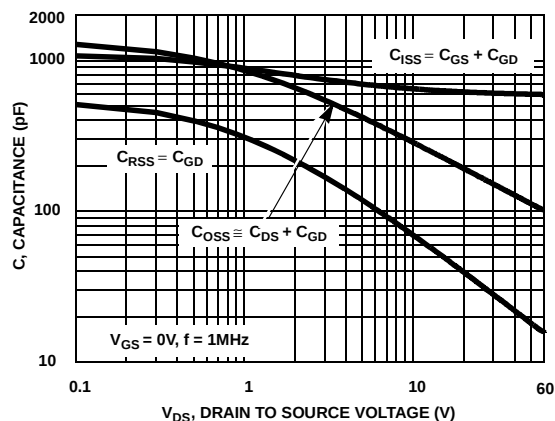


Figure 13. Capacitance vs Drain to Source Voltage

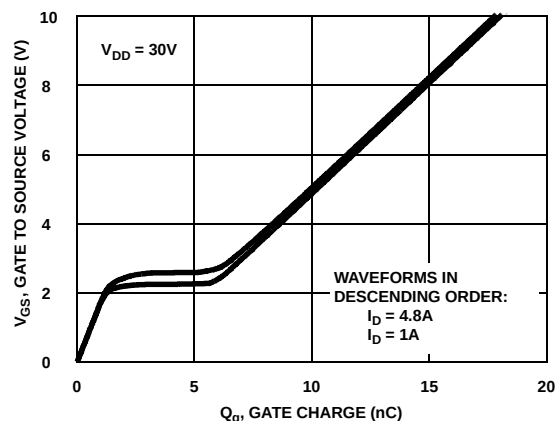


Figure 14. Gate Charge Waveforms for Constant Gate Currents

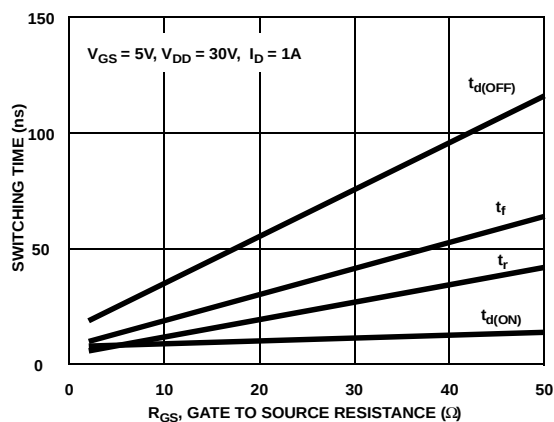


Figure 15. Switching Time vs Gate Resistance

Test Circuits and Waveforms

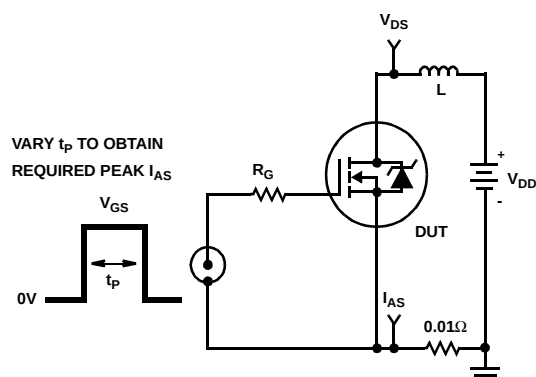


Figure 16. Unclamped Energy Test Circuit

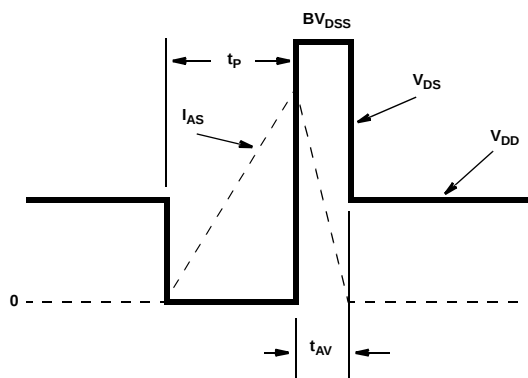


Figure 17. Unclamped Energy Waveforms

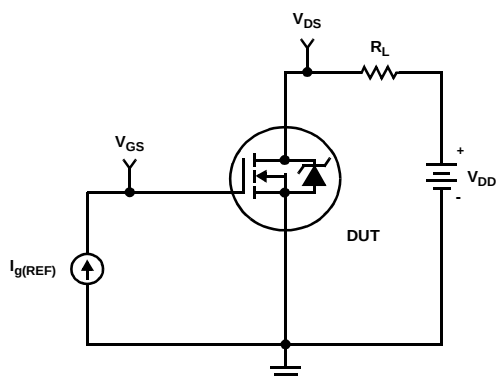


Figure 18. Gate Charge Test Circuit

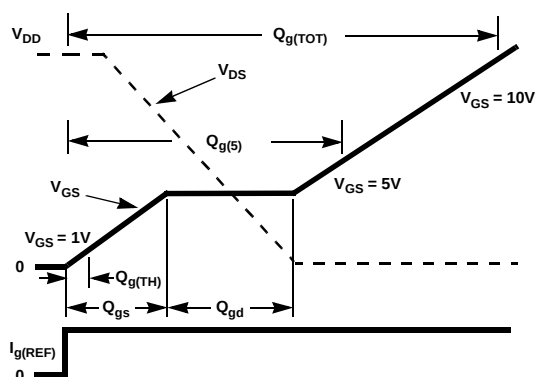


Figure 19. Gate Charge Waveforms

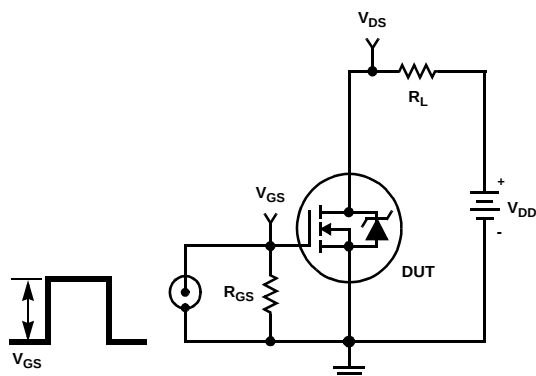


Figure 20. Switching Time Test Circuit

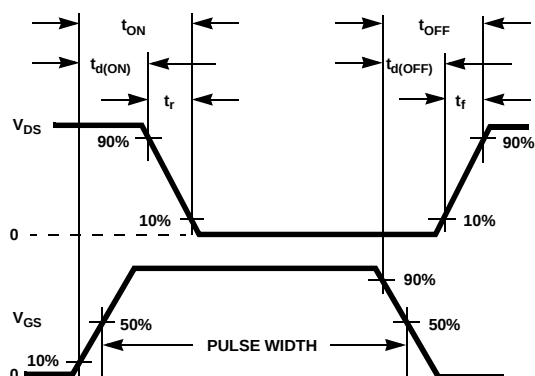


Figure 21. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}\text{C}$), and thermal resistance $R_{\theta JA}$ ($^{\circ}\text{C/W}$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the SO-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 22 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 22 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 103.2 - 24.3 \ln(\text{Area}) \quad (\text{EQ. 2})$$

The dual die SO-8 package introduces an additional thermal coupling resistance, $R_{\theta B}$. Equation 3 describes $R_{\theta B}$ as a function of the top copper mounting pad area.

$$R_{\theta B} = 46.4 - 21.7 \ln(\text{Area}) \quad (\text{EQ. 3})$$

The thermal coupling resistance vs. copper area is also graphically depicted in Figure 22.

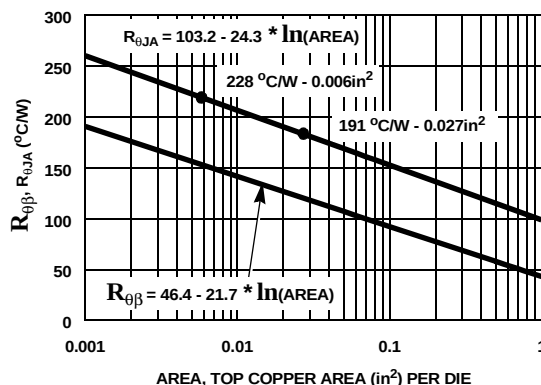


Figure 22. Thermal Resistance vs Mounting Pad Area

SPICE Thermal Model

REV April 2002
HUFA76413DK8T
Copper Area = 0.493in²

CTHERM1 th 8 8.5e-4
CTHERM2 8 7 1.8e-3
CTHERM3 7 6 5.0e-3
CTHERM4 6 5 1.3e-2
CTHERM5 5 4 4.0e-2
CTHERM6 4 3 1.5e-1
CTHERM7 3 2 7.5e-1
CTHERM8 2 tl 3

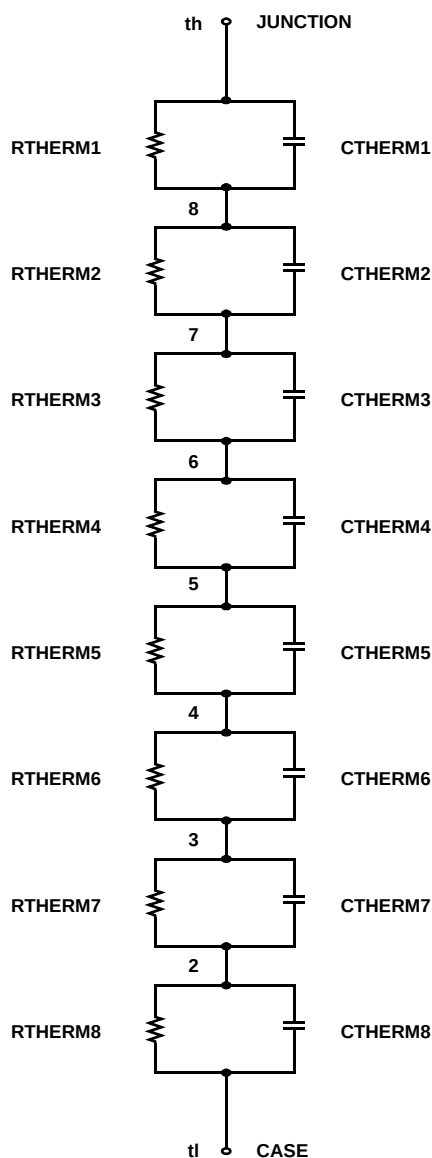
RTHERM1 th 8 3.5e-2
RTHERM2 8 7 6.0e-1
RTHERM3 7 6 2
RTHERM4 6 5 8
RTHERM5 5 4 18
RTHERM6 4 3 20
RTHERM7 3 2 23
RTHERM8 2 tl 25

SABER Thermal Model

SABER thermal model HUFA76413DK8T
Copper Area = 0.493in²
template thermal_model th tl
thermal_c th, tl

```
{
  ctherm.ctherm1 th 8 =8.5e-4
  ctherm.ctherm2 8 7 =1.8e-3
  ctherm.ctherm3 7 6 =5.0e-3
  ctherm.ctherm4 6 5 =1.3e-2
  ctherm.ctherm5 5 4 =4.0e-2
  ctherm.ctherm6 4 3 =1.5e-1
  ctherm.ctherm7 3 2 =7.5e-1
  ctherm.ctherm8 2 tl =3
}
```

```
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rtherm.rtherm2 8 7 =6.0e-1
rtherm.rtherm3 7 6 =2
rtherm.rtherm4 6 5 =8
rtherm.rtherm5 5 4 =18
rtherm.rtherm6 4 3 =20
rtherm.rtherm7 3 2 =23
rtherm.rtherm8 2 tl =25
}
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I48

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