

LC87F7NJ2A



CMOS LSI

8-bit Microcontroller

with LCD Controller Driver

192K-byte Flash ROM / 8K-byte RAM / 100-pin

ON Semiconductor®

www.onsemi.com

Features

- LCD Driver 4COM × 54SEG
- Infrared Remote Control Receiver Circuit × 2
- Full duplex UART × 2

Performance

- Minimum Bus Cycle Time
56ns (CF=18MHz)
- Minimum Instruction Cycle Time (T_{cyc})
167ns (CF=18MHz)
- Operating Supply Voltage
2.7V to 3.6V
- Operating Ambient Temperature
-40°C to +85°C

Function Descriptions

1) Ports

- I/O Ports 29
- LCD Common Ports 4
- LCD Segment Ports 54 (I/O port combined use)
- Bias Power Source For LCD 3
- Power Pins (VSS1, VDD1) 6

2) Timer × 8

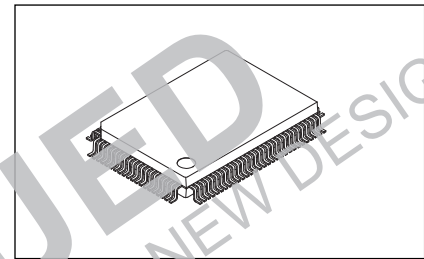
- Timer 0 : 16-bit timer/counter with capture registers
- Timer 1 : 16-bit timer that supports PWM/toggle outputs
- Timer 4 : 8-bit timer with a 6-bit prescaler
- Timer 5 : 8-bit timer with a 6-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 8 : 16-bit timer with an 8-bit prescaler
- Base timer

3) Full duplex UART × 2

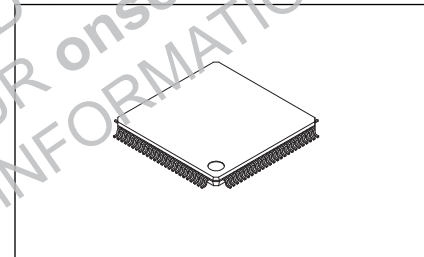
4) Infrared Remote Control Receiver Circuit × 2

Application

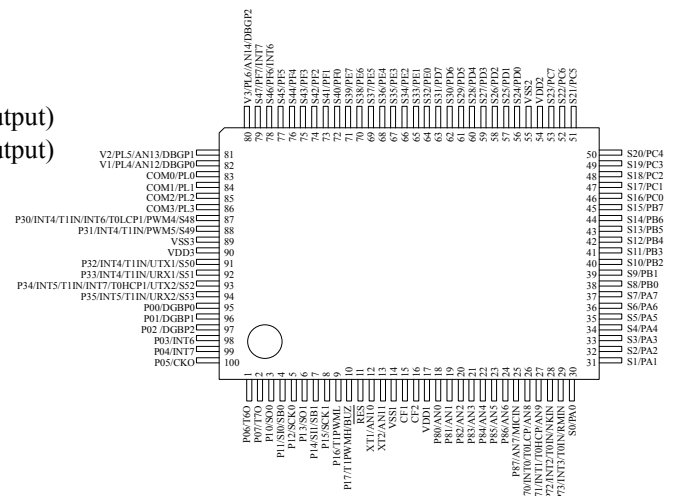
- AV apparatus
- Household appliance mounted with LCD panel



QIP100E(14X20)



TQFP100(14X14)
[Under Development]



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ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

Function Details

■ Ports

- Normal withstand voltage I/O ports
Ports whose I/O direction can be designated in 1 bit units : 29 (P0n, P1n, P70 to P73, P8n, XT2)
- Normal withstand voltage input port : 1 (XT1)
- LCD ports
 - Segment output : 54 (S00 to S53)
 - Common output : 4 (COM0 to COM3)
 - Bias power sources for LCD driver : 3 (V1 to V3)
- Other functions
 - Input/output ports : 54 (P3n, PAn, PBn, PCn, PDn, PEn, PFn)
 - Input ports : 7 (PLn)
- Dedicated oscillator ports : 2 (CF1, CF2)
- Reset pins : 1 (RES)
- Power pins : 6 (VSS1 to VSS3, VDD1 to VDD3)

■ LCD Controller

- 1) Seven display modes are available (static, 1/2, 1/3, 1/4 duty × 1/2, 1/3 bias)
- 2) Segment output and common output can be switched to general-purpose input/output ports

■ Small Signal Detection (MIC signals etc.)

- 1) Counts pulses with a level which is greater than a preset value
- 2) 2-bit counter

■ Timers

- Timer 0 : 16-bit timer/counter with two capture registers.
 - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
 - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
 - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
 - Mode 3 : 16-bit counter (with two 16-bit capture registers)
- Timer1 : 16-bit counter timer that supports PWM/toggle outputs
 - Mode 0 : 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer counter with an 8-bit prescaler (with toggle outputs)
 - Mode 1 : 8-bit PWM with an 8-bit prescaler × 2 channels
 - Mode 2 : 16-bit counter timer with an 8-bit prescaler (with toggle outputs)
(toggle outputs also possible from the lower-order 8 bits)
 - Mode 3 : 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer4 : 8-bit timer with a 6-bit prescaler
- Timer5 : 8-bit timer with a 6-bit prescaler
- Timer6 : 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer7 : 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer8 : 16-bit timer
 - Mode 0 : 8-bit timer with an 8-bit prescaler × 2 channels
 - Mode 1 : 16-bit timer with an 8-bit prescaler
- Base Timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes
- Day and time counter
 - 1) Used with a base timer, the day and time counter can be used as a 65000 day + minute + second counter.

■ High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- 2) Can generate output real-time.

■ Serial Interfaces

- SIO0 : 8-bit synchronous serial interface
 - 1) LSB first/MSB first made selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1 : 8-bit asynchronous/synchronous serial interface
 - Mode 0 : Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1 : Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART1

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■ UART2

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■ AD Converter : 12 bits × 15 channels**■ PWM : Multi frequency 12-bit PWM × 2 channels****■ Infrared Remote Control Receiver Circuit1**

- 1) Noise reduction function (Time constant of noise reduction filter : approx. 120μs, when selecting a 32.768kHz crystal oscillator as a reference clock)
- 2) Supporting reception formats with a guide-pulse of half-clock/clock/none.
- 3) Determines a end of reception by detecting a no-signal periods (No carrier).
(Supports same reception format with a different bit length.)
- 4) X'tal HOLD mode cancellation function

■ Infrared Remote Control Receiver Circuit2

- 1) Noise reduction function
(Time constant of noise reduction filter: approx. 120μs, when selecting a 32.768kHz crystal oscillator as a reference clock.)
- 2) Supporting reception formats with a guide-pulse of half-clock/clock/none.
- 3) Determines a end of reception by detecting a no-signal periods (No carrier).
(Supports same reception format with a different bit length.)
- 4) X'tal HOLD mode cancellation function

■ Watchdog Timer

- 1) External RC watchdog timer
- 2) Interrupt and reset signals selectable

■ Clock Output Function

- 1) Can output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 as a system clock.
- 2) Can output the source oscillation clock for the sub clock.

■ Interrupt Source Flags

- 31 sources, 10 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/remote control receiver1
4	0001BH	H or L	INT3/base timer/INT5/ remote control receiver2
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/ UART2 receive/T8L/T8H
8	0003BH	H or L	SIO1/UART1 transmit/ UART2 transmit
9	00043H	H or L	ADC/MIC/T6/T7/PWM4/PWM5
10	0004BH	H or L	Port 0/T4/T5

- Priority levels $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

• IFLG (List of interrupt source flag function)

- 1) Shows a list of interrupt source flags that caused a branching to a particular vector address.

■ Subroutine Stack Levels

- 4096/2048 levels maximum (The stack is allocated in RAM.)

■ High-speed Multiplication/Division Instructions

- 16 bits $\times$ 8 bits (5 tCYC execution time)
- 24 bits $\times$ 16 bits (12 tCYC execution time)
- 16 bits $\div$ 8 bits (8 tCYC execution time)
- 24 bits $\div$ 16 bits (12 tCYC execution time)

■ Oscillation Circuits

- RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf and external Rd
- Crystal oscillation circuit : For low-speed system clock, with internal Rf and external Rd
- Multifrequency RC oscillation circuit (internal) : For system clock
 - 1) Adjustable in $\pm 4\%$ (typ) increments from the selected center frequency.
 - 2) Measures the frequency of the source oscillation clock using the input signal from XT1 as the reference.

■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2 μ s, 2.4 μ s, 4.8 μ s, 9.6 μ s, 19.2 μ s, 38.4 μ s, and 76.8 μ s (at a main clock rate of 10MHz).

■ Standby Function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation (Some parts of the serial transfer function stop operation).
 - 1) Oscillation is not stopped automatically.
 - 2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, X'tal, and multifrequency RC oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
- X'tal HOLD mode : Suspends instruction execution and the operation of the peripheral circuits except the base timer and infrared remote controller circuit.
 - 1) The CF, RC, and multifrequency RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are five ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit
 - (5) Having an interrupt source established in the infrared remote control receiver circuit

■ On-chip Debugger Function

- Supports software debugging with the IC mounted on the target board.

■ Package Form

- QIP100E(14×20) : Pb-Free / Halogen Free type
- TQFP100(14×14) : Pb-Free / Halogen Free type [Under Development]

■ Development Tools

- On-chip Debugger : TCB87 TypeB +LC87F7Nxx A or TCB87 TypeC (3Lines Cable) +LC87F7NxxA

■ Flash ROM Programming boards

Package	Programming Boards
QIP100E(14×20)	W87FQ100
TQFP100(14×14)	W87FSQ100

■ Flash ROM Programmer

Maker		Model	Supported Version	Device
Flash Support Group, Inc (FSG)	Single Programmer	AF9709C	(Note 2)	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
	Gang Programmer	AF9723/AF9723B(main unit) (including models manufactured by Ando Electric Co., Ltd.)	(Note 2)	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
		AF9833(unit) (including models manufactured by Ando Electric Co., Ltd.)	(Note 2)	
Flash Support Group, Inc (FSG) +Our company (Note 1)	In-circuit Single/Gang Programmer	AF9101/AF9103(main unit) (manufactured by FSG)	(Note 2)	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
		SIB87 Type C (Interface Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK Type B / Type C (SanyoFWS)	Application Version 1.08or later Chip Data Version 2.44 later	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
	In-circuit Single/Gang Programmer	SKK-DBG Type B /Type C (SanyoFWS)		

Contact information about the AF series :

Flash Support Group Company (TOA ELECTRONICS, Inc.)

Phone : 81-53-428-8380

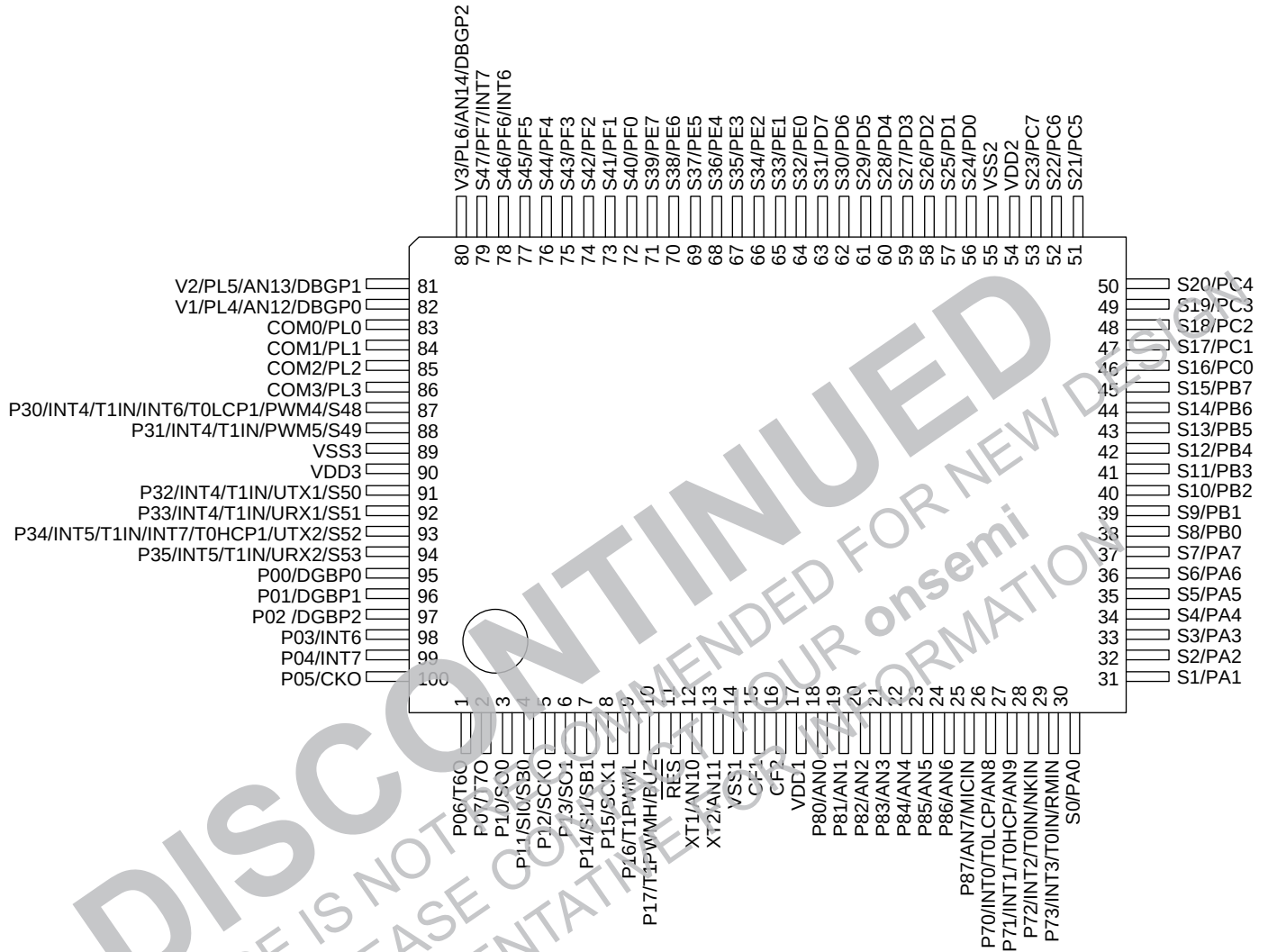
E-mail : sales@j-fsg.co.jp

Note1 : On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from our company (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

Note2 : It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

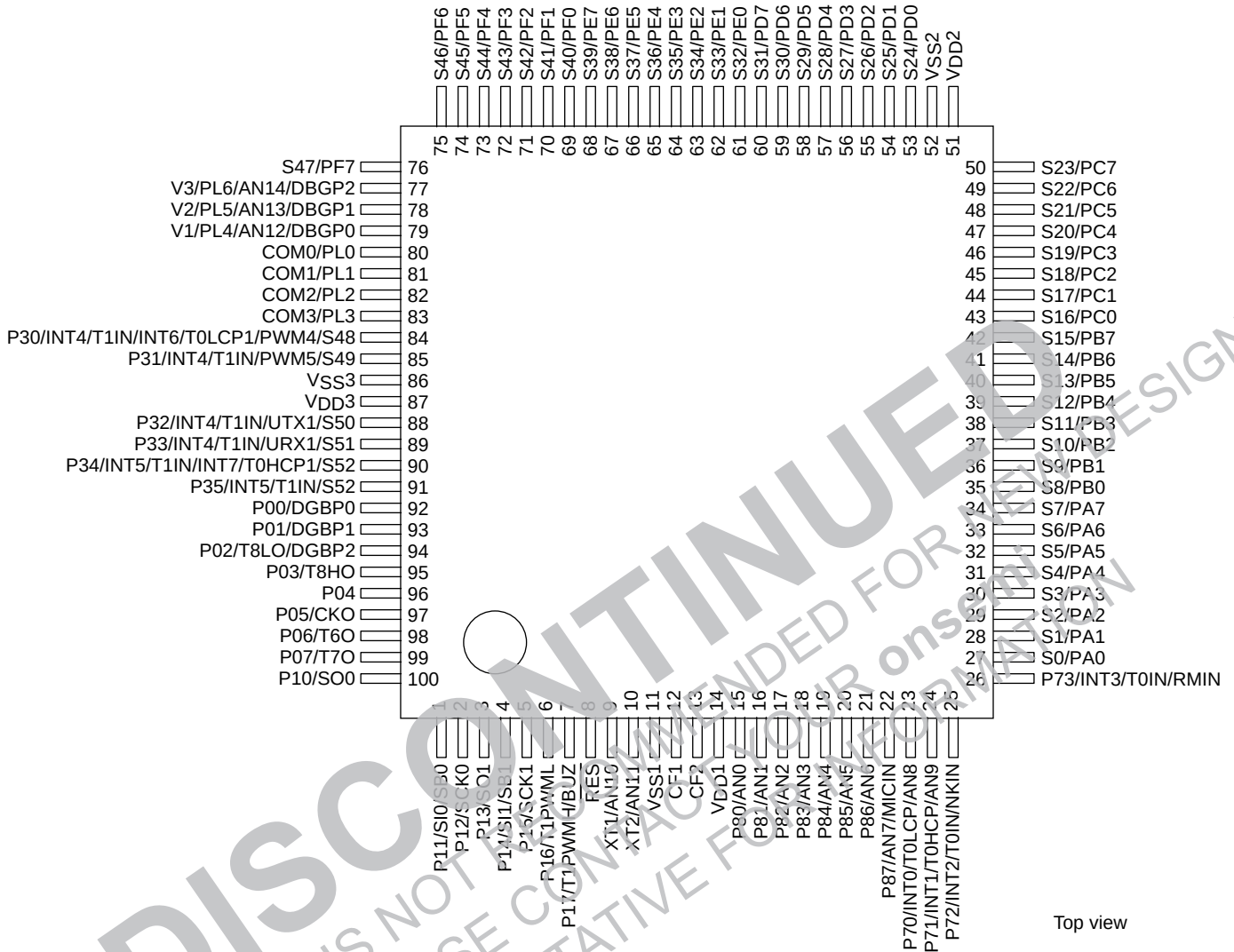
Pin Assignment

QIP100E(14×20), Pb-Free/Halogen Free type



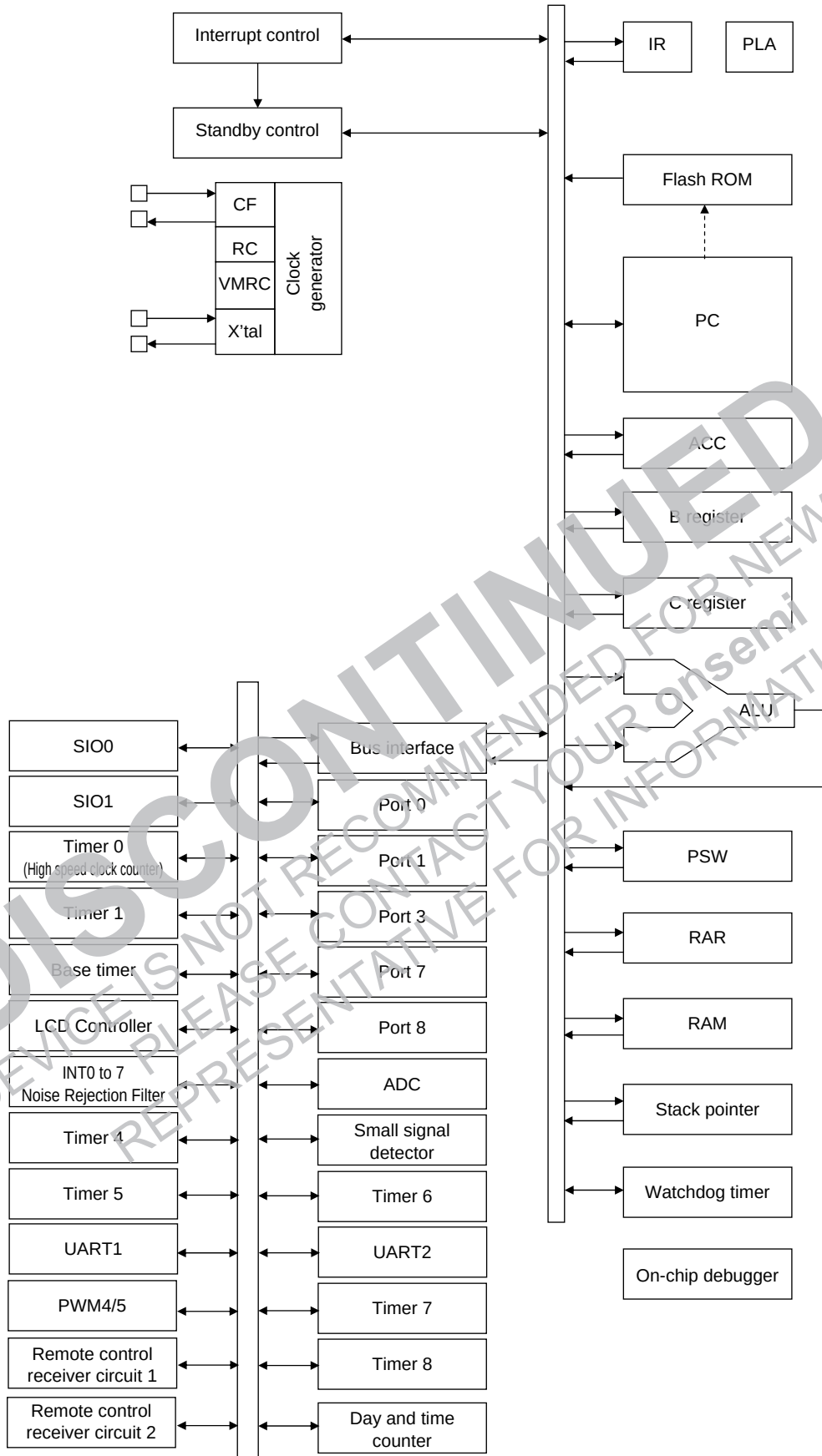
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TQFIP100(14×14), Pb-Free/Halogen Free type [Under Development]



Top view

System Block Diagram



Pin Description

Pin Name	I/O	Description	Option																														
VSS1 VSS2 VSS3	-	– power supply pin	No																														
VDD1 VDD2 VDD3	-	+ power supply pin	No																														
Port 0	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Input for HOLD release • Input for port 0 interrupt • Shared pins - P03: INT6 input - P04: INT7 input - P05: Clock output (system clock/can selected from sub clock) - P06: Timer 6 toggle output - P07: Timer 7 toggle output - On chip debugger pins: DBGP0 to DBGP2(P00 to P02)	Yes																														
P00 to P07																																	
Port 1	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Shared pins - P10: SIO0 data output - P11: SIO0 data input/bus I/O - P12: SIO0 clock I/O - P13: SIO1 data output - P14: SIO1 data input/bus I/O - P15: SIO1 clock I/O - P16: Timer 1P/WMH output - P17: Timer 1P/WMH output/deeper output	Yes																														
P10 to P17																																	
Port 3	I/O	• 6-bit I/O port • Segment output for LCD • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Shared pins - P30 to P33: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/timer 0H capture input - P34 to P35: INT5 input/HOLD release input/timer 1 event input/timer 0L capture input/timer 0H capture input - P30: PWM4 output/INT6 input/timer 0L capture 1 input - P31: PWM5 output - P32: UART1 transmit - P33: UART1 receive - P34: UART2 transmit/INT7 input/timer 0H capture 1 input - P35: UART2 receive Interrupt acknowledge type <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising & Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising & Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	INT6	enable	enable	enable	disable	disable	INT7	enable	enable	enable	disable	disable	Yes
			Rising	Falling	Rising & Falling	H level	L level																										
INT4	enable	enable	enable	disable	disable																												
INT5	enable	enable	enable	disable	disable																												
INT6	enable	enable	enable	disable	disable																												
INT7	enable	enable	enable	disable	disable																												
P30 to P35																																	

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Pin Name	I/O	Description	Option																														
Port 7	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Shared pins P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output P71: INT1 input/HOLD release input/timer 0H capture input P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/ high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/ remote control receiver input AD converter input ports: AN8 (P70), AN9 (P71) Interrupt acknowledge type <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising & Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising & Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
			Rising	Falling	Rising & Falling	H level	L level																										
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
P70 to P73																																	
Port 8	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Shared pins AD converter input ports: AN0 to AN7 Small signal detector input port: MICIN (P87)	No																														
P80 to P87																																	
S0/PA0 to S7/PA7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PA)	No																														
S8/PB0 to S15/PB7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PB)	No																														
S16/PC0 to S23/PC7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PC)	No																														
S24/PD0 to S31/PD7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PD)	No																														
S32/PE0 to S39/PE7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PE)	No																														
S40/PF0 to S47/PF7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PF) PF6: INT6 input PF7: INT7 input	No																														
COM0/PL0 to COM3/PL3	I/O	• Common output for LCD • Can be used as general-purpose input port (PL)	No																														
V1/PL4 to V3/PL6	I/O	• LCD output bias power supply • Can be used as general-purpose input port (PL) • Shared pins AD converter input ports: AN12 (V1) to AN14 (V3) On-chip debugger pins: DBGPO (V1) to DBGP2 (V3)	No																														
RES	Input	Reset pin	No																														
XT1	Input	• 32.768kHz crystal oscillator input pin • Shared pins General-purpose input port Must be connected to V_{DD1} if not to be used. AD converter input port: AN10	No																														
XT2	I/O	• 32.768kHz crystal oscillator output pin • Shared pins General-purpose I/O port Must be set for oscillation and kept open if not to be used. AD converter input port: AN11	No																														
CF1	Input	Ceramic resonator input pin	No																														
CF2	Output	Ceramic resonator output pin	No																														

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode

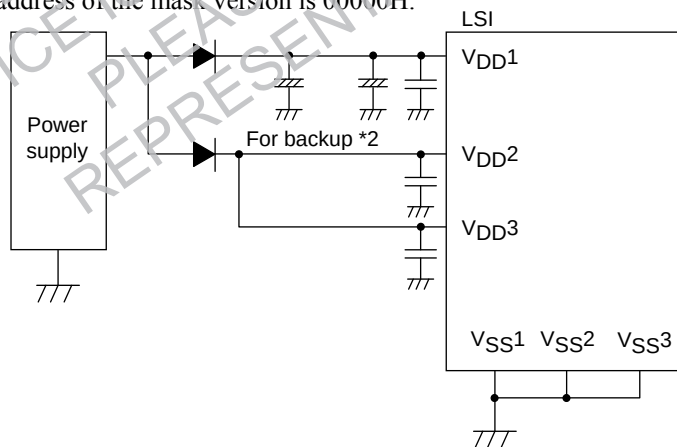
Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	each bit	1	CMOS	Programmable (Note)
		2	Nch-open drain	Programmable
P10 to P17	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P35	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	Nch-open drain	No
S0/PA0 to S47/PF7	-	No	CMOS	Programmable
COM0/PL0 to COM3/PL3	-	No	Input only	No
V1/PL4 to V3/PL6	-	No	Input only	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

User Option List

Option Name	Option Type	Mask Version *1	Flash Version	Option Selected in Units of	Specified Item
Port output form	P00 to P07	○	○	each bit	CMOS
					Nch-open drain
	P10 to P17	○	○	each bit	CMOS
					Nch-open drain
	P30 to P35	○	○	each bit	CMOS
					Nch-open drain
Program start address	-	x	○	-	00000H
					1FF00H

*1: Mask option selection - No change possible after the mask is completed.

*2: Program start address of the mask version is 00000H.



*1: Connect the IC as shown below to minimize the noise input to the VDD1 pin.
Be sure to electrically short the VSS1, VSS2, and VSS3 pins.

*2: The internal memory is sustained by VDD1. If none of VDD2 and VDD3 are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.
Make sure that the port outputs are held at the low level in the HOLD backup mode.

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Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			
						min	typ	max	unit
Maximum supply voltage		V _{DD} max	V _{DD1} , V _{DD2} , V _{DD3}	V _{DD1} =V _{DD2} =V _{DD3}		-0.3		+4.6	V
supply voltage for LCD		VLCD	V1/PL4, V2/PL5, V3/PL6	V _{DD1} =V _{DD2} =V _{DD3}		-0.3		V _{DD}	
Input voltage		V _I (1)	Port L XT1, CF1, $\overline{\text{RES}}$			-0.3		V _{DD} +0.3	
		V _I (2)	V _{DD2} , V _{DD3}			V _{SS}		V _{DD} +0.1	
Input/output voltage		V _{IO} (1)	Ports 0, 1, 3, 7, 8 Ports A, B, C, D, E, F, XT2			-0.3		V _{DD} +0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 32 to 35	• CMOS output selected • Current at each pin		-10			mA
		IOPH(2)	Ports 30, 31	• CMOS output selected • Current at each pin		-20			
		IOPH(3)	Ports 71 to 73	Current at each pin		-5			
		IOPH(4)	Ports A, B, C, D, E, F	Current at each pin		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 32 to 35	• CMOS output selected • Current at each pin		-7.5			
		IOMH(2)	Ports 30, 31	• CMOS output selected • Current at each pin		-15			
		IOMH(3)	Ports 71 to 73	Current at each pin		-3			
		IOMH(4)	Ports A, B, C, D, E, F	Current at each pin		-3			
	Total output current	ΣIOAH(1)	Ports 0, 1, 32 to 35	Total of all pins		-25			
		ΣIOAH(2)	Ports 30, 31	Total of all pins		-25			
		ΣIOAH(3)	Ports 0, 1, 3	Total of all pins		-45			
		ΣIOAH(4)	Ports 71 to 73	Total of all pins		-5			
		ΣIOAH(5)	Ports A, B, C	Total of all pins		-25			
		ΣIOAH(6)	Ports D, E, F	Total of all pins		-25			
		ΣIOAH(7)	Ports A, B, C, D, E, F	Total of all pins		-45			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 32 to 35	Current at each pin				20	
		IOPL(2)	Ports 30, 31	Current at each pin				30	
		IOPL(3)	Ports 7, 8 XT2	Current at each pin				10	
		IOPL(4)	Ports A, B, C, D, E, F	Current at each pin				10	
	Mean output current (Note 1-1)	IOML(1)	Ports 0, 1, 32 to 35	Current at each pin				15	
		IOML(2)	Ports 30, 31	Current at each pin				20	
		IOML(3)	Ports 7, 8 XT2	Current at each pin				7.5	
		IOML(4)	Ports A, B, C, D, E, F	Current at each pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0,1,32 to 35	Total of all pins				45	
		ΣIOAL(2)	Ports 30, 31	Total of all pins				45	
		ΣIOAL(3)	Ports 0, 1, 3	Total of all pins				80	
		ΣIOAL(4)	Ports 7, 8 XT2	Total of all pins				20	
		ΣIOAL(5)	Ports A, B, C	Total of all pins				45	
ΣIOAL(6)		Ports D, E, F	Total of all pins				45		
ΣIOAL(7)		Ports A, B, C, D, E, F	Total of all pins				80		
Maximum power dissipation		Pd max	QIP100E(14×20)	Ta=-40 to +85°C				215	mW
			TQFP100(14×14)	Ta=-40 to +85°C				under	
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Allowable Operating Range at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				$V_{DD} [\text{V}]$	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD1}=V_{DD2}=V_{DD3}$	$0.167\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.7		3.6	V
			$0.356\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.5		3.6	
Memory sustaining supply voltage	VHD	V_{DD1}	RAM and register contents sustained in HOLD mode.		2.0		3.6	
High level input voltage	$V_{IH}(1)$	Ports 0, 3, 8 Ports A, B, C, D, E, F Port L	Output disabled	2.5 to 3.6	$0.3V_{DD} + 0.7$		V_{DD}	
	$V_{IH}(2)$	Port 1 Ports 71 to 73 P70 port input/ interrupt side	• Output disabled • When $INT1VTSL=0$ (P71 only)	2.5 to 3.6	$0.3V_{DD} + 0.7$		V_{DD}	
	$V_{IH}(3)$	P71 interrupt side	• Output disabled • When $INT1VTSL=1$	2.5 to 3.6	$0.85V_{DD}$		V_{DD}	
	$V_{IH}(4)$	P87 small signal input side	Output disabled	2.5 to 3.6	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(5)$	P70 watchdog timer side	Output disabled	2.5 to 3.6	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(6)$	XT1, XT2, CF1, RES		2.5 to 3.6	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 0, 3, 8 Ports A, B, C, D, E, F Port L	Output disabled	2.5 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Port 1 Ports 71 to 73 P70 port input/ interrupt side	• Output disabled • When $INT1VTSL=0$ (P71 only)	2.5 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	P71 interrupt side	• Output disabled • When $INT1VTSL=1$	2.5 to 3.6	V_{SS}		$0.45V_{DD}$	
	$V_{IL}(4)$	P87 small signal input side	Output disabled	2.5 to 3.6	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(5)$	P70 watchdog timer side	Output disabled	2.5 to 3.6	V_{SS}		$0.8V_{DD} - 1.0$	
	$V_{IL}(6)$	XT1, XT2, CF1, RES		2.5 to 3.6	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	t_{CYC}			2.7 to 3.6	0.167		200	μs
				2.5 to 3.6	0.356		200	
External system clock frequency	$F_{EXCF}(1)$	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	2.5 to 3.6	0.1		18	MHz
			• CF2 pin open • System clock frequency division ratio=1/2	2.5 to 3.6	0.2		36	

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between t_{CYC} and oscillation frequency is $3/F_{mCF}$ at a division ratio of 1/1 and $6/F_{mCF}$ at a division ratio of 1/2.

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• 18MHz ceramic oscillation • See Fig. 1.	2.7 to 3.6		18		MHz
	FmCF(2)	CF1, CF2	• 8MHz ceramic oscillation • See Fig. 1.	2.5 to 3.6		8		
	FmRC		Internal RC oscillation	2.5 to 3.6	0.3	1.0	2.0	
	FmVMRC(1)		• Frequency variable RC source oscillation • When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSEL4M=0	2.5 to 3.6		10		
	FmVMRC(2)		• Frequency variable RC source oscillation • When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSEL4M=1	2.5 to 3.6		4		
	FsX'tal	XT1, XT2	• 32.768kHz crystal oscillation • See Fig. 2.	2.5 to 3.6		32.768		kHz
Frequency variable RC oscillation usable range	OpVMRC(1)		When VMSEL4M=0	2.5 to 3.6	8	10	12	MHz
	OpVMRC(2)		When VMSEL4M=1	2.5 to 3.6	3.5	4	4.5	
Frequency variable RC oscillation adjustment range	VmADJ(1)		Each step of VMRAJn (Wide range)	2.5 to 3.6	8	24	64	%
	VmADJ(2)		Each step of VMFAJn (Small range)	2.5 to 3.6	1	4	8	

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 3, 7, 8 Ports A, B, C, D, E, F Port L	• Output disabled • Pull-up resistor off • V _{IN} =V _{DD} (Including output Tr's off leakage current)	2.5 to 3.6			1	μA
	I _{IH} (2)	RES	V _{IN} =V _{DD}	2.5 to 3.6			1	
	I _{IH} (3)	XT1, XT2	• For input port specification • V _{IN} =V _{DD}	2.5 to 3.6			1	
	I _{IH} (4)	CF1	V _{IN} =V _{DD}	2.5 to 3.6			15	
	I _{IH} (5)	P87 small signal input side	V _{IN} =VBIS+0.5V (VBIS: Bias voltage)	2.5 to 3.6	1.5	5.5	10	
Low level input current	I _{IL} (1)	Ports 0, 1, 3, 7, 8 Ports A, B, C, D, E, F Port L	• Output disabled • Pull-up resistor off • V _{IN} =V _{SS} (Including output Tr's off leakage current)	2.5 to 3.6	-1			μA
	I _{IL} (2)	RES	V _{IN} =V _{SS}	2.5 to 3.6	-1			
	I _{IL} (3)	XT1, XT2	• For input port specification • V _{IN} =V _{SS}	2.5 to 3.6	-1			
	I _{IL} (4)	CF1	V _{IN} =V _{SS}	2.5 to 3.6	-15			
	I _{IL} (5)	P87 small signal input side	V _{IN} =VBIS-0.5V (VBIS: Bias voltage)	2.5 to 3.6	-10	-5.5	-1.5	

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High level output voltage	V _{OH} (1)	Ports 0, 1, 32 to 35	I _{OH} =-0.4mA	2.5 to 3.6	V _{DD} -0.4			V
	V _{OH} (2)	Ports 30, 31	I _{OH} =-1.6mA	2.5 to 3.6	V _{DD} -0.4			
	V _{OH} (3)	Ports 71 to 73	I _{OH} =-0.4mA	2.5 to 3.6	V _{DD} -0.4			
	V _{OH} (4)	Ports A, B, C Ports D, E, F	I _{OH} =-0.4mA	2.5 to 3.6	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 32 to 35 Ports 30, 31 (PWM function output mode)	I _{OL} =1.6mA	2.5 to 3.6			0.4	V
	V _{OL} (2)	Ports 30, 31 (Port function output mode)	I _{OL} =5mA	2.5 to 3.6			0.4	
	V _{OL} (3)	Ports 7, 8 XT2	I _{OL} =1.6mA	2.5 to 3.6			0.4	
	V _{OL} (4)	Ports A, B, C Ports D, E, F	I _{OL} =1.6mA	2.5 to 3.6			0.4	
LCD output voltage regulation	VODLS	S0 to S53	- I_O=0mA - V_{LCD}, 2/3V_{LCD}, 1/3V_{LCD} level output - See Fig. 8.	2.5 to 3.6	0		±0.2	V
	VODLC	COM0 to COM3	- I_O=0mA - V_{LCD}, 2/3V_{LCD}, 1/2V_{LCD}, 1/3V_{LCD} level output - See Fig. 8.	2.5 to 3.6	0		±0.2	
LCD bias resistor	RLCD(1)	Resistance per one bias resistor	See Fig. 8.	2.5 to 3.6		60		kΩ
	RLCD(2)	Resistance per one bias resistor 1/2R mode	See Fig. 8.	2.5 to 3.6		30		
Resistance of pull-up MOS Tr.	Rpu(1)	Ports 0, 1, 3, 7 Ports A, B, C, D, E, F	V _{OH} =0.9V _{DD}	2.5 to 3.6	18	50	50	V
Hysteresis voltage	VHYS(1)	Ports 1, 7 RES		2.5 to 3.6		0.1V _{DD}		V
	VHYS(2)	P87 small signal input side		2.5 to 3.6		0.1V _{DD}		
Pin capacitance	CP	All pins	- For pins other than that under test: - V_{IN}=V_{SS} - f=1MHz - Ta=25°C	2.5 to 3.6		10		pF
Input sensitivity	Vsen	P87 small signal input side		2.5 to 3.6	0.12V _{DD}			V _{pp}

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Serial I/O Characteristics at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$, $0.190\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$

SIO0 Serial I/O Characteristics (Note 4-1-1) at $V_{DD} = 2.7\text{V}$ to 3.6V $0.190\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			
						min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 3.6	2		tCYC
		Low level pulse width	tSCKL(1)				1		
		High level pulse width	tSCKH(1)				1		
			tSCKHA(1)	- Continuous data transmission/reception mode - See Fig. 6. (Note 4-1-2)			4		
	Output clock	Frequency	tSCK(2)	SCK0(P12)	- CMOS output selected - See Fig. 6.	2.5 to 3.6	4/3		tSCK
		Low level pulse width	tSCKL(2)				1/2		
		High level pulse width	tSCKH(2)				1/2		
			tSCKHA(2)	- Continuous data transmission/reception mode - CMOS output selected - See Fig. 6.			tSCKH(2) + 2tCYC	tSCKH(2) + (10/3)tCYC	
Serial input	Data setup time	tsDI(1)	SB0(P11), SIO(P11)	- Must be specified with respect to rising edge of SIOCLK. - See Fig. 6.	2.5 to 3.6	0.03			
	Data hold time	thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	Continuous data transmission/reception mode (Note 4-1-3)	2.5 to 3.6			(1/3)tCYC + 0.05	μs
			tdD0(2)	Synchronous 8-bit mode (Note 4-1-3)				1tCYC + 0.05	
	Output clock		tdD0(3)	(Note 4-1-3)				(1/3)tCYC + 0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIO0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			
						min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.5 to 3.6	2		tCYC
		Low level pulse width	tSCKL(3)				1		
		High level pulse width	tSCKH(3)				1		
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	2		tSCK
		Low level pulse width	tSCKL(4)				1/2		
		High level pulse width	tSCKH(4)				1/2		
Serial input	Data setup time	tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03		μs	
	Data hold time	thDI(2)			2.5 to 3.6	0.03			
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.5 to 3.6		(1/3)tCYC ±0.05		

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			
					min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P30 to P33), INT5(P34 to P35), INT6(P30), INT7(P34)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	256			
	tPIH(5) tPIL(5)	MICIN(P87)	Condition that signal is accepted to small signal detection counter.	2.5 to 3.6	1			
	tPIH(6) tPIL(6)	RMIN(P73)	Condition that signal is accepted to remote control receiver circuit.	2.5 to 3.6	4			RMCK (Note 5-1)
	tPIL(7)	RES	Resetting is enabled.	2.5 to 3.6	200			μs

Note 5-1: RMCK is an unit for the base clock (40tCYC/50tCYC/Sub-Clock) of remote control receiver circuit.

AD Converter Characteristics at $V_{SS1} = V_{SS2} = V_{SS3} = 0V$

<12bits AD Converter Mode at $T_a = -30$ to $+70^\circ C$ >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		2.5 to 3.6		12		bit
Absolute accuracy	ET	AN7(P87), AN8(P70),	(Note 6-1)	2.5 to 3.6			± 16	LSB
Conversion time	tCAD	AN9(P71), AN10(XT1), AN11(XT2)	• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	64		115	μs
				2.7 to 3.6	128		230	
				2.5 to 3.6	256		460	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		$VAIN = V_{DD}$	2.5 to 3.6			1	μA
	IAINL		$VAIN = V_{SS}$	2.5 to 3.6	-1			

<8bits AD Converter Mode at $T_a = -30$ to $+70^\circ C$ >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		2.5 to 3.6		8		bit
Absolute accuracy	ET	AN7(P87), AN8(P70),	(Note 6-1)	2.5 to 3.6			± 1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1), AN11(XT2)	• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	39		71	μs
				2.7 to 3.6	79		140	
				2.5 to 3.6	157		280	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		$VAIN = V_{DD}$	2.5 to 3.6			1	μA
	IAINL		$VAIN = V_{SS}$	2.5 to 3.6	-1			

<Conversion time calculation formulas>

12bits AD Converter Mode: tCAD(Conversion time) = $((52/(\text{division ratio})) + 2) \times (1/3) \times tCYC$

8bits AD Converter Mode: tCAD(Conversion time) = $((32/(\text{division ratio})) + 2) \times (1/3) \times tCYC$

Note 6-1: The quantization error ($\pm 1/2$ LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				VDD [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	VDD1 = VDD2 = VDD3	- FmCF=18MHz ceramic oscillation mode - FmX'tal=32.768kHz crystal oscillation mode - System clock set to 12MHz side - Internal RC oscillation stopped. - Frequency variable RC oscillation stopped. 1/1 frequency division ratio	2.7 to 3.6		6.1	15.6	mA
	IDDOP(2)		- FmCF=8MHz ceramic oscillation mode - FmX'tal=32.768kHz crystal oscillation mode - System clock set to 12MHz side - Internal RC oscillation stopped. - Frequency variable RC oscillation stopped. 1/1 frequency division ratio	2.5 to 3.6		3.9	8.8	
	IDDOP(3)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz crystal oscillation mode - System clock set to internal RC oscillation - Frequency variable RC oscillation stopped. 1/2 frequency division ratio	2.5 to 3.6		0.4	1.7	
	IDDOP(4)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz crystal oscillation mode - Internal RC oscillation stopped. - System clock set to 10MHz with frequency variable RC oscillation 1/1 frequency division ratio	2.5 to 3.6		4.3	12.0	
	IDDOP(5)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz crystal oscillation mode - Internal RC oscillation stopped. - System clock set to 4MHz with frequency variable RC oscillation 1/1 frequency division ratio	2.5 to 3.6		2.1	6.6	
	IDDOP(6)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz crystal oscillation mode - System clock set to 32.768kHz side - Internal RC oscillation stopped. - Frequency variable RC oscillation stopped. 1/2 frequency division ratio	2.5 to 3.6		19.3	73	μA

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V _{DD1} =V _{DD2} =V _{DD3}	• HALT mode • FmCF=18MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		2.7	6.8	mA
	IDDHALT(2)		• HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.5 to 3.6		1.4	3.1	
	IDDHALT(3)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		0.2	0.75	
	IDDHALT(4)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		1.6	4.5	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		0.7	1.75	
	IDDHALT(6)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		12.4	54.9	μA
HOLD mode consumption current	IDDHOLD(1)	V _{DD1}	• HOLD mode • CF1=V_{DD} or open (External clock mode)	2.5 to 3.6		0.08	18.4	
Timer HOLD mode consumption current	IDDHOLD(2)		• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FmX'tal=32.768kHz crystal oscillation mode	2.5 to 3.6		10.14	34.4	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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F-ROM Write Characteristics at $T_a = +10^{\circ}\text{C}$ to $+55^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	V_{DD1}	• Without CPU current	3.0 to 3.6		7	11	mA
Programming time	tFW(1)		• 2K-byte erase operation	3.0 to 3.6		12	15	ms
	tFW(2)		• 2K-byte writing operation	3.0 to 3.6		35	45	μs

UART (Full Duplex) Operating Conditions at $T_a = +40$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

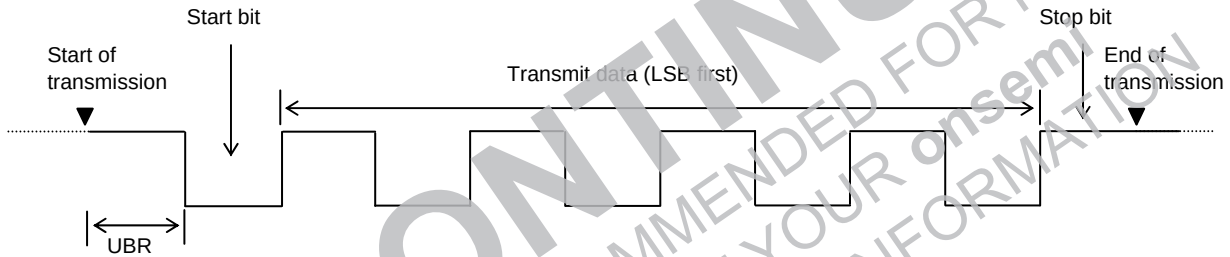
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR	UTX(S32), URX(S33)		2.5 to 3.6	16/3		8192/3	tCYC

Data length : 7/8/9 bits (LSB first)

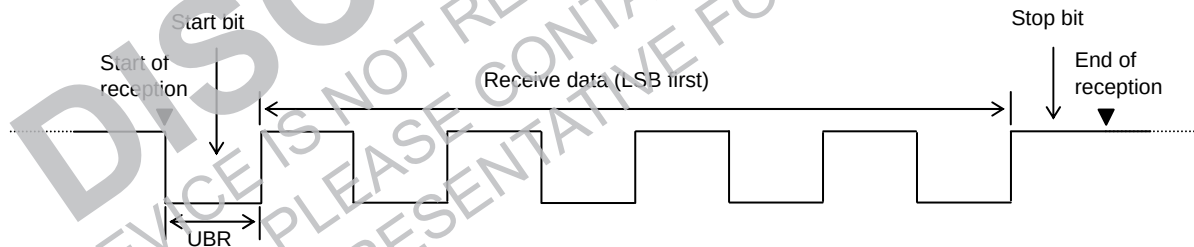
Stop bits : 1 bit (2-bit in continuous data transmission)

Parity bits : None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
18MHz	MURATA	CSTCE18M0V51-R0	(5)	(5)	OPEN	150	2.7 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS18M0X51-B0	(5)	(5)	OPEN	0	2.7 to 3.6	0.11	0.33	
10MHz	MURATA	CSTCE10M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS10M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS8M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillation Circuit with a Crystal Oscillation

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	9	9	Open	330k	2.5 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Fig. 4).

Caution: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

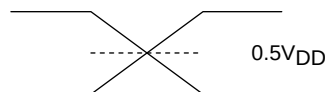
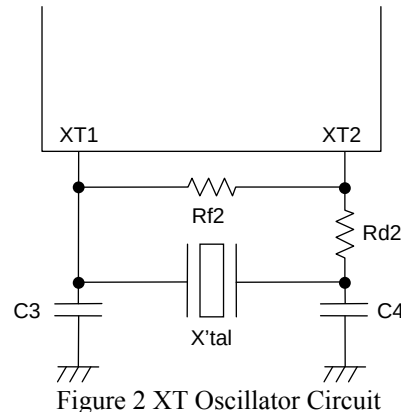
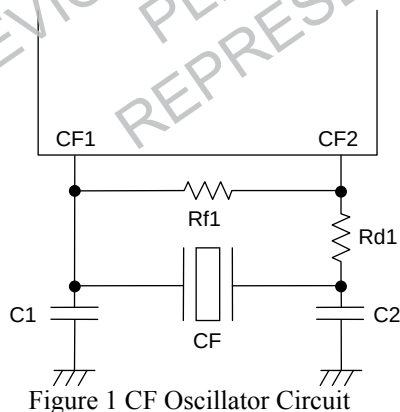
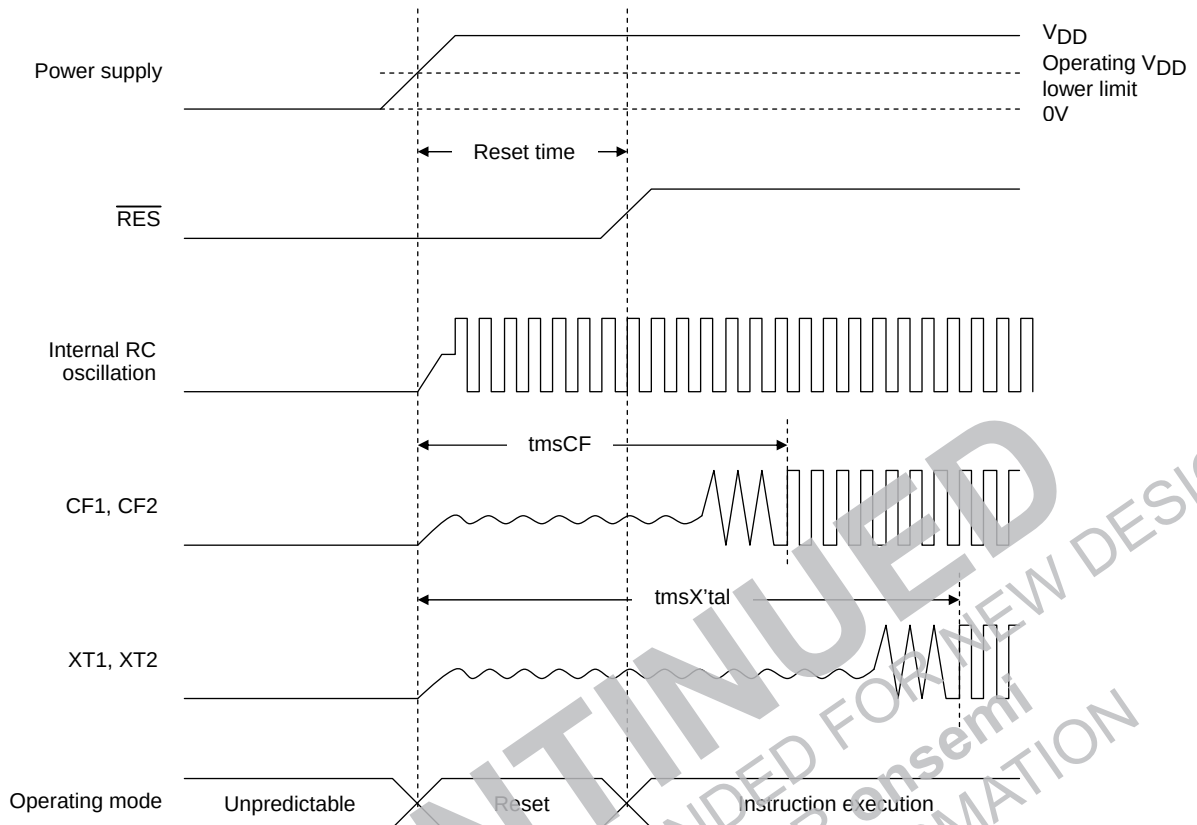
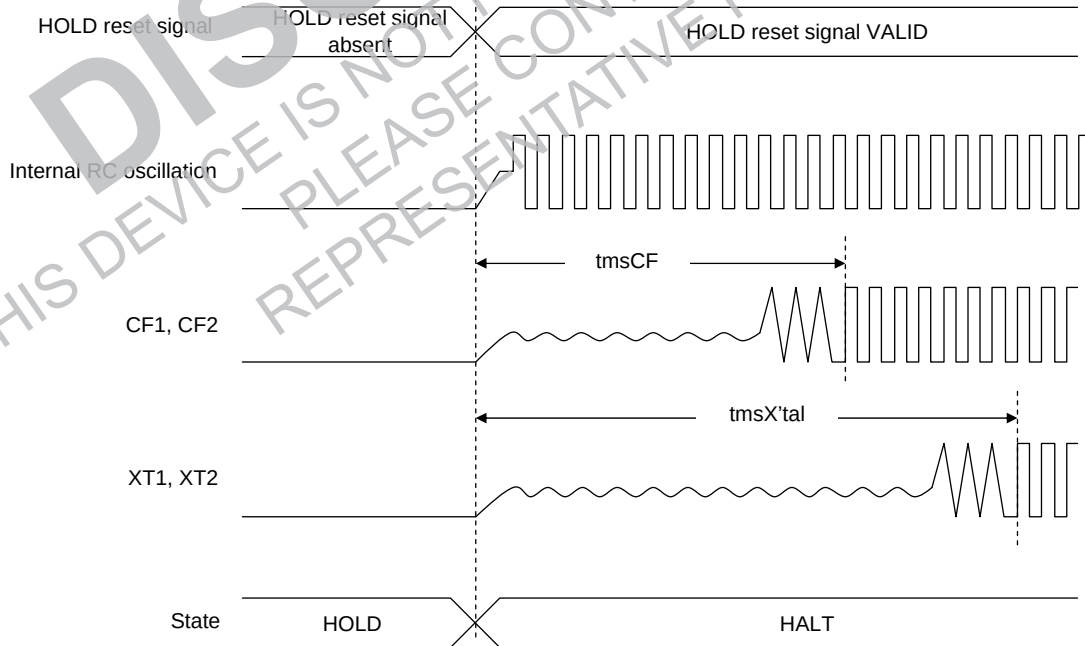


Figure 3 AC Timing Measurement Point

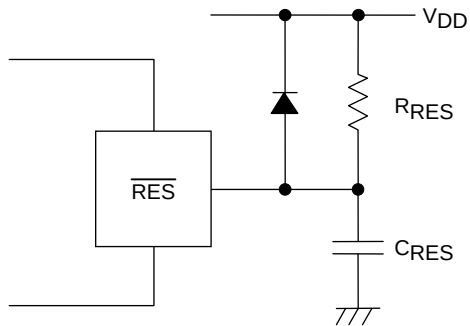


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note :

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of $200\mu s$ after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

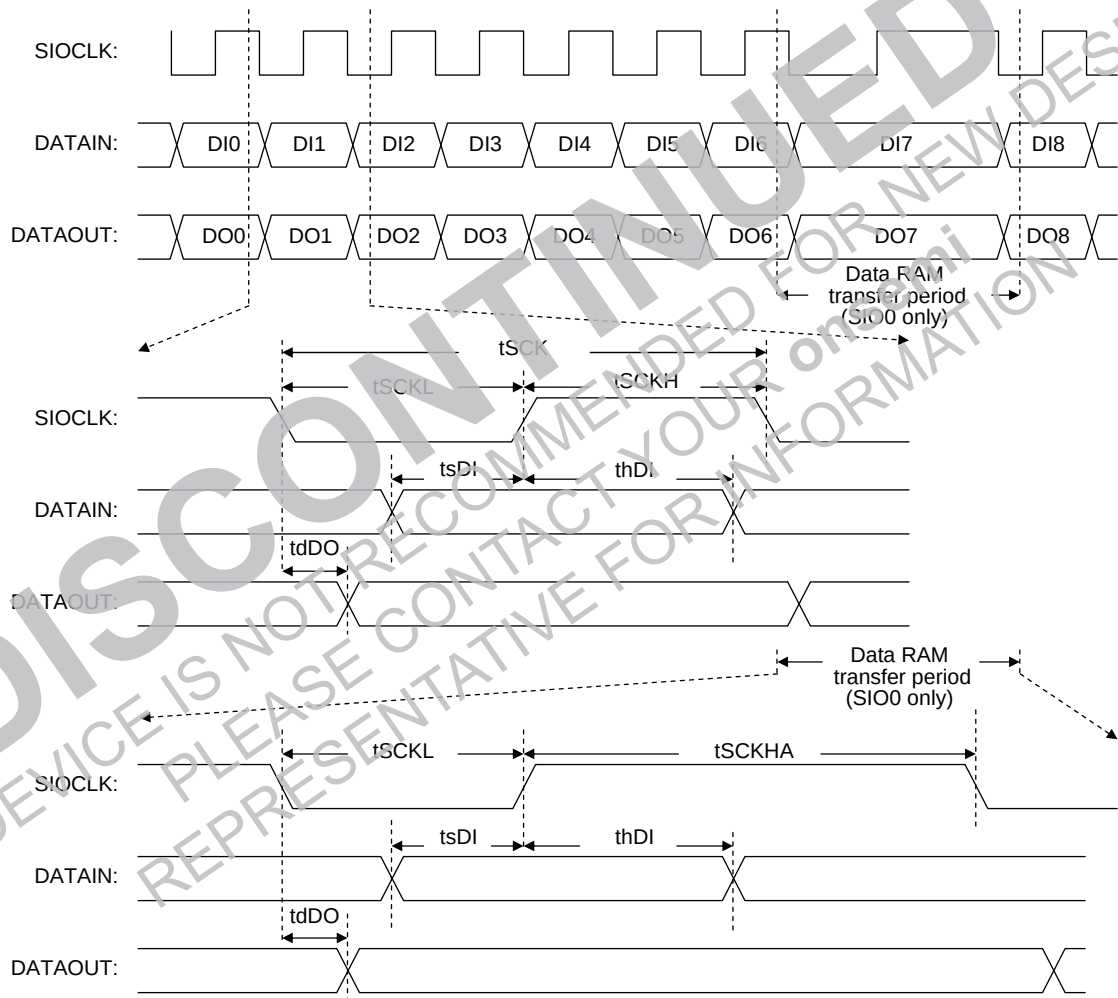


Figure 6 Serial I/O Waveforms

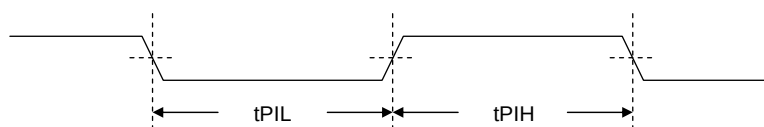


Figure 7 Pulse Input Timing Signal Waveform

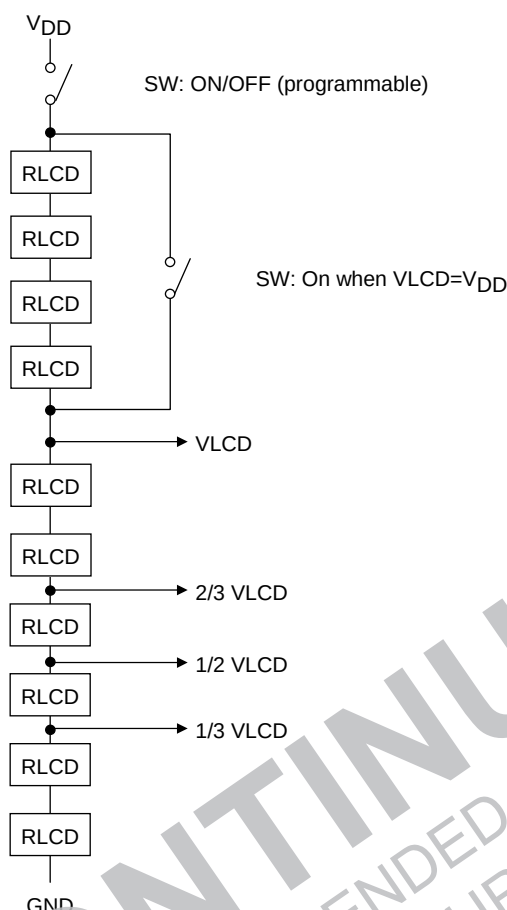


Figure 8 LCD bias resistor

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F7NC8AUEJ-2H	QIP100E(14×20) (Pb-Free / Halogen Free)	50 / Tray Foam
LC87F7NC8AVUEJ-2H	QIP100E(14×20) (Pb-Free / Halogen Free)	50 / Tray Foam

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