High Voltage Boost LED Driver with High-Side Current Sensing and LED Wiring Fault Detection

Features

- Switch mode controller for boost LED Driver
- High output current accuracy
- Constant frequency operation
- Hiccup mode protection for both short circuit and open circuit conditions
- High-side current sense

Applications

- RGB or white LED backlighting

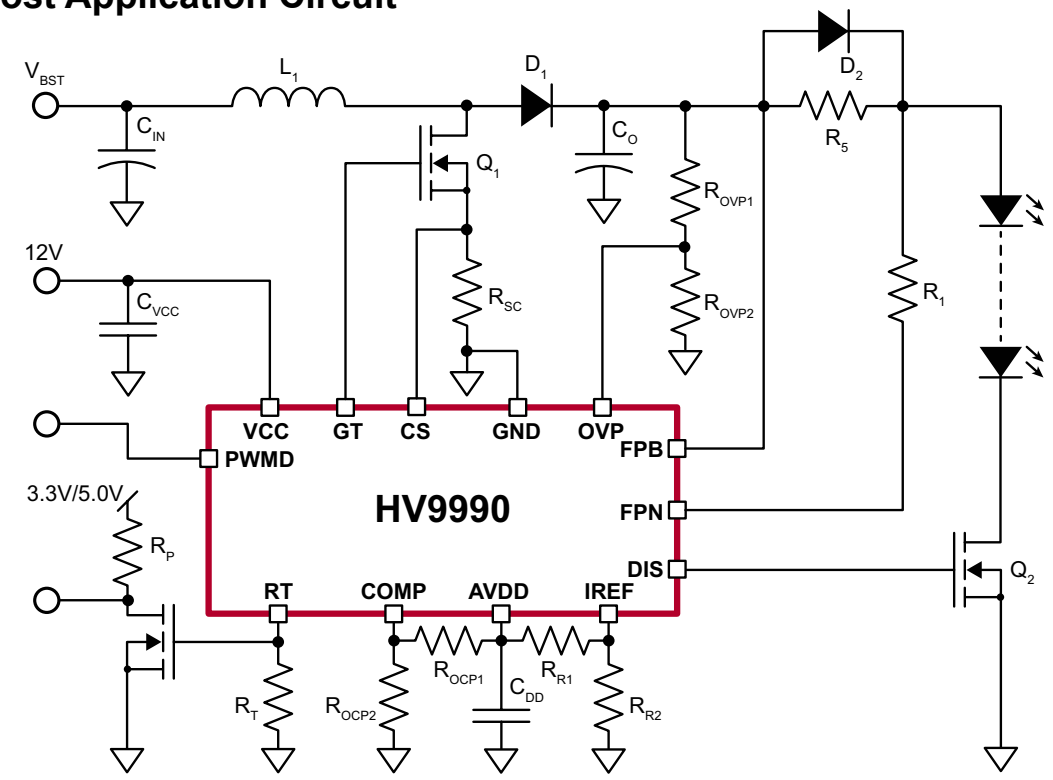
General Description

The HV9990 is a current mode control LED driver IC designed to control a boost LED driver in constant frequency mode. The controller uses a peak current-mode control scheme (with programmable slope compensation) and includes an internal transconductance amplifier to accurately control the output current over all line and load conditions. The IC also provides a disconnect switch gate drive output, which can be used to achieve good PWM rise and fall times for the LED current using an external disconnect FET.

HV9990 also provides a TTL compatible, low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz.

HV9990 includes a high side current sense which can be used to protect against the short circuiting of the LED wiring to the chassis .

Typical Boost Application Circuit

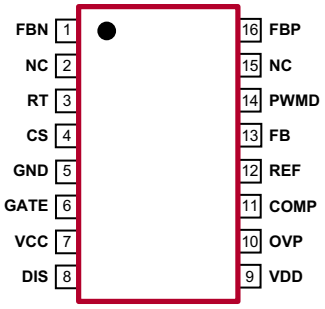


Ordering Information

Part Number	Package Option	Packing
HV9990NG-G	16-Lead SOIC (Narrow Body)	45/Tube
HV9990NG-G M934	16-Lead SOIC (Narrow Body)	2500/Reel

-G indicates package is RoHS compliant ('Green')

Pin Description



16-Lead SOIC (NG)

Absolute Maximum Ratings

Parameter	Value
VCC to GND	-0.5V to +16V
GATE, DIS to GND	-0.3V to (V_{CC} +0.3V)
VDD to GND	-0.3V to +3.8V
FBP, FBN to GND	-0.3V to +450V
REF to GND	-0.3V to +1.5V
All other pins to GND	-0.3V to (V_{DD} +0.3V)
Junction temperature	+150°C
Storage ambient temperature range	-65°C to +150°C
Continuous power dissipation *(T_A = +25°C)*	1000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Product Marking

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Typical Thermal Resistance

Package	θ_{ja}
16-Lead SOIC	83°C/W

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{CC} = 12V, C_{VCC} = 1µF, C_{DD} = 1µF, C_{GATE} = 1nF, C_{FLT} = 500pF, R_T = 374kΩ unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Unit	Conditions
Input							
V_{CC}	Input DC supply voltage range	-	10	12	14	V	DC input voltage
I_{CCSD}	Shut-down mode supply current	-	-	-	1.5	mA	PWMD to GND
$UVLO_{rise,VCC}$	V_{CC} under voltage lockout threshold	*	9.0	-	9.5	V	V_{CC} rising
$UVLO_{hyst,VCC}$	V_{CC} under voltage hysteresis	-	-	1.0	-	V	V_{CC} falling
Internal Low Voltage Regulator							
V_{DD}	Internally regulated voltage	-	3.23	3.30	3.37	V	PWMD = V_{DD}; f_S = 300kHz; I_{VDD_ext} = 0-500µA
$UVLO_{rise,VDD}$	V_{DD} under voltage lockout threshold	*	3.03	3.10	3.17	V	V_{DD} rising
$UVLO_{hyst,VDD}$	V_{DD} under voltage hysteresis	-	-	0.20	-	V	V_{DD} falling

Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{CC} = 12V, C_{VCC} = 1µF, C_{DD} = 1µF, C_{GATE} = 1nF, C_{FLT} = 500pF, R_T = 374kΩ unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Unit	Conditions
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	1.0	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull down resistor	-	50	100	150	kΩ	V_{PWMD} = 3.3V
Boost FET Driver							
I_{SOURCE}	GATE short circuit current, sourcing	*	0.20	-	-	A	V_{GATE} = 0V
I_{SINK}	GATE sinking current	*	0.50	-	-	A	V_{GATE} = V_{CC}
T_{RISE}	GATE output rise time	-	-	-	70	ns	---
T_{FALL}	GATE output fall time	-	-	-	35	ns	---
Disconnect FET Driver							
$_{ISOURCE,DIS}$	GATE short circuit current, sourcing	*	0.02	-	-	A	V_{GATE} = 0V
$I_{SINK,DIS}$	GATE sinking current	*	0.04	-	-	A	V_{GATE} = V_{CC}
$T_{RISE,DIS}$	GATE output rise time	-	-	-	300	ns	---
$T_{FALL,DIS}$	GATE output fall time	-	-	-	150	ns	---
Over Voltage Protection							
$V_{OVP,rising}$	Over voltage rising trip point	*	1.94	2.00	2.06	V	OVP rising
$V_{OVP,HYST}$	Over voltage hysteresis	-	-	0.20	-	V	OVP falling
T_{PROP_DELAY}	Propagation delay time	-	-	-	200	ns	50mV overdrive
V_{RESET}	Reset voltage to enable driver	*	0.18	0.20	0.22	V	---
Hiccup Timer							
T_{HICCUP}	Hiccup Time	-	-	2.56	-	-	f_S = 100kHz
Current Sense							
T_{BLANK}	Leading edge blanking	*	100	-	250	ns	---
T_{PROP_DELAY1}	Delay to GT falling	-	-	-	200	ns	COMP = AV_{DD}, 50mV overdrive at CS
R_{div}	Internal resistor divider ratio – COMP to CS	#	-	0.167	-	-	---
V_{OFFSET}	Comparator offset voltage	#	-10	-	+10	mV	---
$R_{PULLDOWN}$	Pull down FET resistance	*	-	-	100	Ω	---

Notes:

\# *Denotes specifications guaranteed by design*

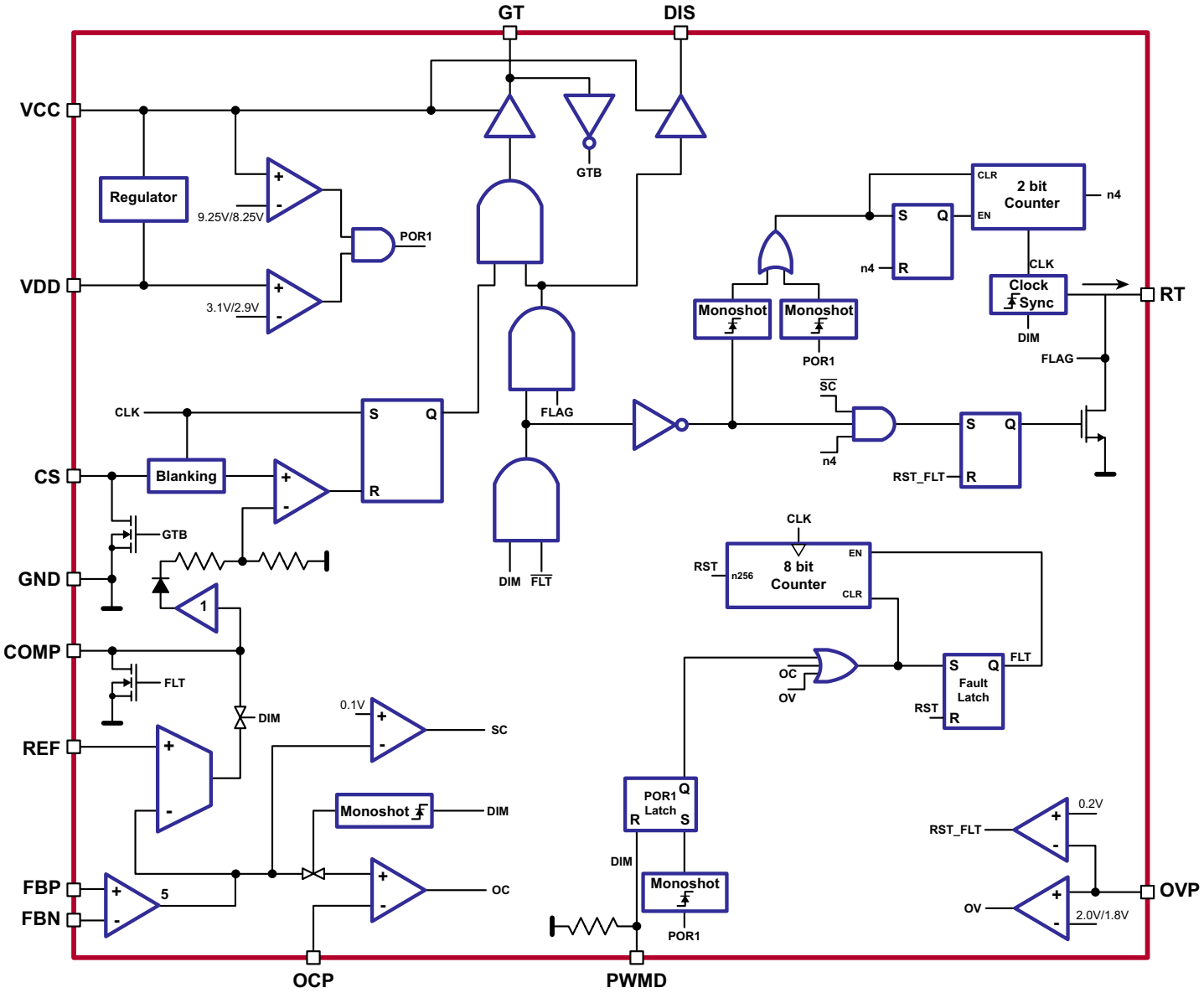
Electrical Characteristics *(cont.)*

*((The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{CC} = 12V, C_{VCC} = 1µF, C_{DD} = 1µF, C_{GATE} = 1nF, C_{FLT} = 500pF, R_T = 374kΩ unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Unit	Conditions
Internal Transconductance Opamp							
GB	Gain-bandwidth product	#	-	1.0	-	MHz	75pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output open
V_{CM}	Input common-mode range	#	-0.3	-	1.5	V	---
V_O	Output voltage range	#	0.7	-	V_{DD}-0.7	V	A_V > 65dB
G_M	Transconductance	-	-	500	-	µA/V	---
V_{OFFSET}	Input offset voltage	*	-3.0	-	3.0	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
$I_{COMP,DIS}$	Discharging current	-	10	-	-	mA	V_{COMP} = 2.0V
$I_{COMP,LKG}$	COMP leakage current	*	-	-	10	nA	PWMD = GND; COMP = 2.0V
GB_{BUFFER}	Gain-bandwidth of the buffer	#	20	-	-	kHz	---
Oscillator							
f_{OSC1}	Oscillator frequency	-	88	100	112	kHz	R_T = 374kΩ
f_{OSC2}	Oscillator frequency	-	220	250	280	kHz	R_T = 249kΩ
F_{OSC}	Output frequency range	#	80	-	300	kHz	---
D_{MAX}	Maximum duty cycle	*	87	-	93	%	---
Short Cathode Detect							
V_{REF2}	FB low comparator threshold	-	-	0.1	-	V	---
T_{PROP_DELAY}	Propagation delay time	-	-	-	200	ns	50mV overdrive
Over Current Protection							
$T_{BLANK,OCP}$	Blanking time for OCP	*	500	-	900	ns	---
T_{PROP_DELAY}	Propagation delay time	*	-	-	200	ns	50mV overdrive

Note:
 # Denotes specifications guaranteed by design

Functional Block Diagram



Note: *All SR latches are SET-dominant*

Description of Blocks

VCC, VDD and Gate Drivers

The external voltage applied at VCC is used to power the IC. The voltage at this pin is typically 12V +/-15% with a 16V absolute maximum rating.

An internal linear regulator is used to generate 3.3V at the VDD pin which is used to power the low voltage analog circuit. The voltage at VDD pin can also be used as a reference to set the LED current using a resistor divider from VDD to the REF pin.

Both VCC and VDD have built-in UVLO to disable the IC in case the voltages at the pins are lower than expected.

The gate drivers are powered off directly from the VCC pin. The switching gate driver currents are supplied from the low ESR capacitor connected externally at the VCC pin.

G_M Amplifier and PWM dimming

The G_M amplifier is used to control the LED current. The current level is set by the voltage at REF pin and the LED current is sensed by a current sense resistor connected to the FPB and FPN pins. Since the current sense amplifierhas a gain of five, the REF voltage has to be 5 times the sensed feedback voltage. The compensation capacitor is connected between COMP and GND.

When PWMD is high, the OTA is allowed to control the voltage at the COMP pin. When PWMD is low, the OTA is disconnected from the COMP pin. The leakage current at the COMP pin due to all circuitry connected to it (ESD protection, pull down transistor and disconnect switch) should be less than 10nA.

The pull down FET at the COMP pin is used to discharge the COMP capacitor at startup and during fault conditions.

Boost FET current sense

The current sense pin has a built in 100ns – 250ns blanking time. It also has a pull down FET which is turned on whenever the GT is off. This is to facilitate slope compensation using external resistor / capacitor network. Although most applications with this IC are expected to be DCM boost circuits which do not need slope compensation, the pull-down FET is included for to make the part usable for CCM boost converters as well.

Hiccup timer

Hiccup timing is achieved by using an internal 8-bit counter which counts 256 clock cycles. This makes the hiccup time dependent on the switching frequency.

Startup

When power is initially applied to the IC, POR1 goes high. At this point, two latches – Fault latch and POR1 latch – are set and FLT goes high. The POR1 latch output will be high till the first PWM pulse is applied at PWMD. This keeps the counter cleared and enabled till the PWMD pulse is applied. Once the first PWM dimming pulse is applied, the counter is allowed to count to 256 and at this point, the gate drivers and COMP pin are released and the converter can start regulating the LED current.

Over-Voltage and over current fault

Over voltage is detected using the voltage at the OVP pin. When the voltage at OVP exceeds 2.0V, over voltage is triggered and the over voltage condition is said to exist till the voltage at OVP drops below 1.8V (10% lower).

Over current condition is detected by the over current comparator which compares the voltage at FB pin to the voltage at OCP pin.

As long as these fault conditions exist, they set the Fault latch which turns off the gate drivers and clears the 8-bit counter and keeps the counter cleared. Once the fault disappers, the counter is allowed to count and the operation of the IC is identical to the startup case.

Short Circuit to Chassis

Short circuit to chassis occurs during the manufacturing process involving large LED strings. Consider a case of three LED light bars connected in series and driven from the same boost converter. The input to the boost converter is typically about 120V. Assume each LED light bar has a forward drop of about 80V (25 LEDs with 3.2V/per LED). If one of connections between the LED lght bars is shorted to ground (see Fig.1), then excessive current might flow through the LEDs.

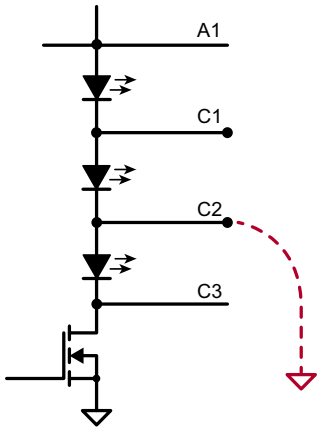


Fig.1 : Short Cathode Condition

This situation needs to be detected and prevented. Note that turning off the boost converter might not be sufficient in all cases. For example, if C1 was shorted in ground in Fig.1, the LED string voltage (one string; 80V) is lower than the input voltage (120V) and the turning off the boost converter will not prevent the short circuit current. Hence, the main solution – besides turning off the boost converter – is to signal the 120V power supply to turn off. This is achieved by means of the FLAG output (see typical application circuit).

In the HV9990, a short cathode condition is detected by sensing the current flowing in the sense resistor when PWMD=0.

Detection of Short Circuit to Chassis

There are two cases to consider when for short circuit protection.

Case 1: *Short circuit condition exists prior to the boost converter being powered on.*

Case 1 can be further subdivided into two more cases.

> ***Case 1a:*** *The short is at node C1. In this case, as soon as the boost power is applied, the high-side current sense amplifier outputs a large feedback voltage, which will typically be higher than the voltage at OCP pin. At this point, the 2-bit counter has completed and is looking for a short circuit condition. It will detect the short condition and pull RT pin down.*

> ***Case 1b:*** *The short is at nodes C2 or C3. In this case, since the input voltage is lower than the LED string voltage, when the boost power is applied, no current flows through the LEDs and nothing happens. When the IC is turned on by applying a PWMD signal, then the IC starts regulating the LED current. The current will be regulated to the programmed value even though there is a short to chassis since the IC is receiving the LED current signal through the high-side current sense amplifier. Short to chassis condition is detected when PWMD goes low, since even though PWMD goes low, the LED current will not be interrupted. This will cause the RT pin to be pulled low.*

Case 2: *Short circuit condition occurs during normal operation. In this case, OCP will be tripped when the short happens and this will cause the converter to go into fault mode. If this were a regular OCP, the current will go to zero when FLT goes high. However, if the short circuit is to chassis, the current will still be flowing once FLT goes high and this is used to detect the fault.*

Reset of the Fault Condition

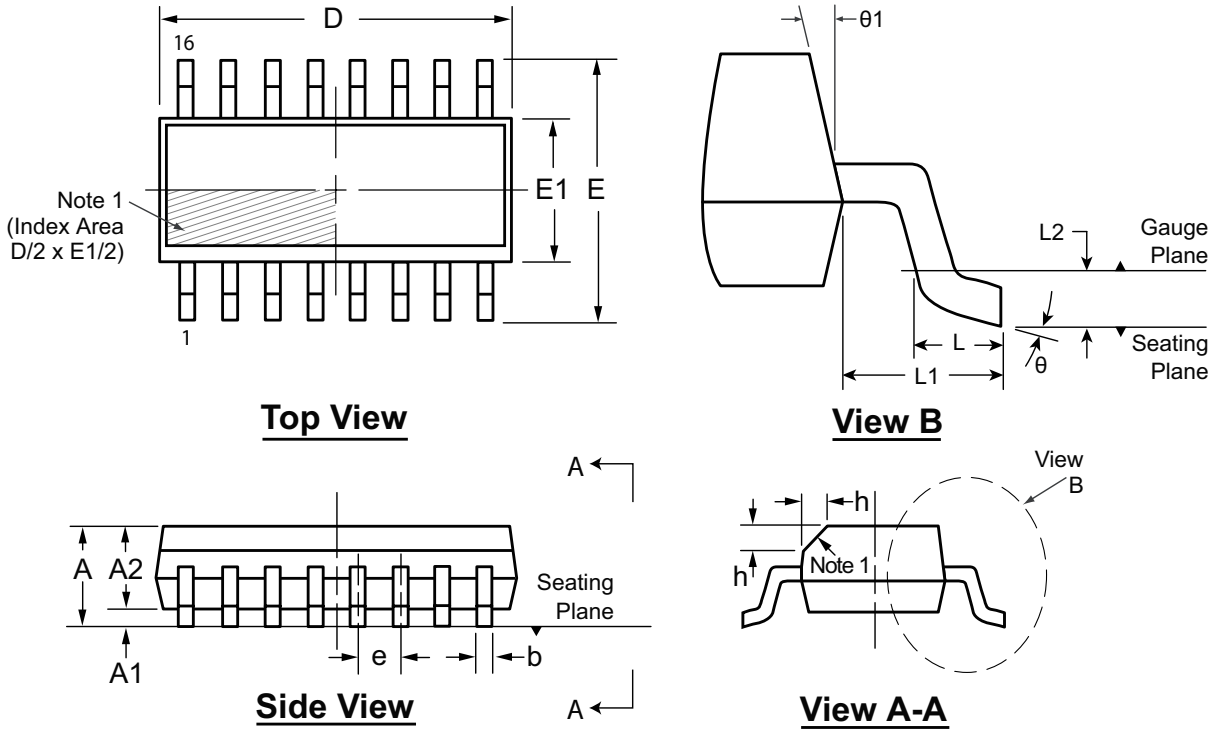
The protection circuit will be reset when the boost power supply is turned off and the output voltage decays to 10% of OVP programmed value. It can also be forced to reset by pulling on the OVP pin using an external pull down FET.

Pin Description (16-Lesd SOIC)

Pin #	Name	Description
1	FBN	This is the negative input of the high voltage current sense amplifier.
2	NC	This is a no-connect pin and should be left open. It provides spacing between the high voltage and low voltage pins of the IC.
3	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode. The switching frequency is synchronized to the PWMD turn on edge.
4	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100ns (min) blanking time.
5	GND	Ground return for all the low power analog internal circuitry as well as the gate drivers. This pin must be connected to the return path from the input.
6	GATE	This is the GATE driver output for the switching FET.
7	VCC	This pin is the power supply input to the IC.
8	DIS	This pin is used to drive an external disconnect FET which disconnects the load from the circuit during a fault condition or during PWM dimming to achieve a very high dimming ratio.
9	VDD	This pin is the output of the low voltage regulator. A low ESR capacitor should be connected from this pin to GND.
10	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 2.0V, the gate output of the HV9990 is turned off and DIS goes low. The IC will turn on when the voltage at the pin goes below 1.8V.
11	COMP	Stable closed loop control can be accomplished by connecting a compensation network between COMP and GND.
12	REF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the VDD pin.
13	FB	This pin provides output current feedback to the HV9990 by using a current sense resistor.
14	PWMD	When this pin is pulled to GND (or left open), switching of the HV9990 is disabled. When an external TTL high level is applied to it, switching will resume.
15	NC	This is a no-connect pin and should be left open. It provides spacing between the high voltage and low voltage pins of the IC.
16	FBP	This pin is the positive input of the high voltage current sense amplifier.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0^O	5^O
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8^O	15^O

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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