



PSMN2R7-30BL

N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

Rev. 1 — 21 March 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

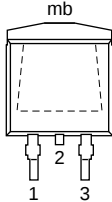
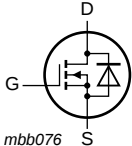
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	1	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	170	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; see Figure 13 ; see Figure 12	-	3.6	4.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 12	-	2.57	3	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 25 A; V _{DS} = 15 V	-	8	-	nC
Q _{G(tot)}	total gate charge	V _{GS} = 4.5 V; I _D = 25 A; V _{DS} = 15 V; see Figure 14 ; see Figure 15	-	32	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	-	300	mJ

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R7-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R7-30BL	PSMN2R7-30BL

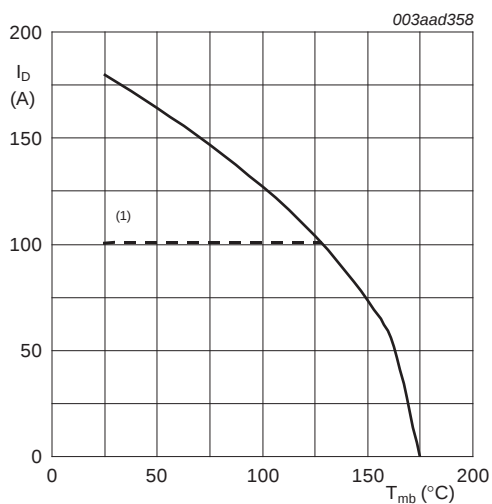
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

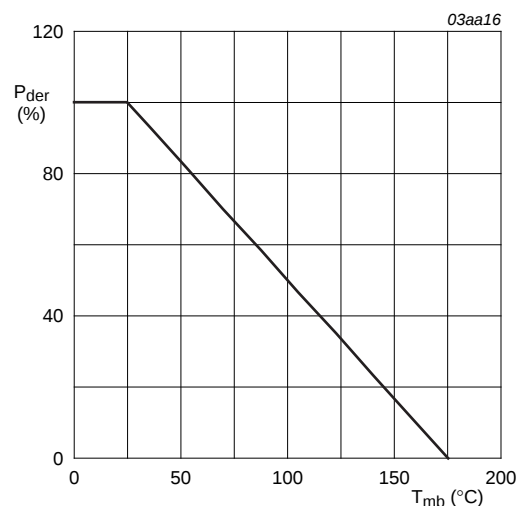
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	[1]	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	[1]	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	730	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	170	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	730	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	300	mJ

[1] Continuous current is limited by package.



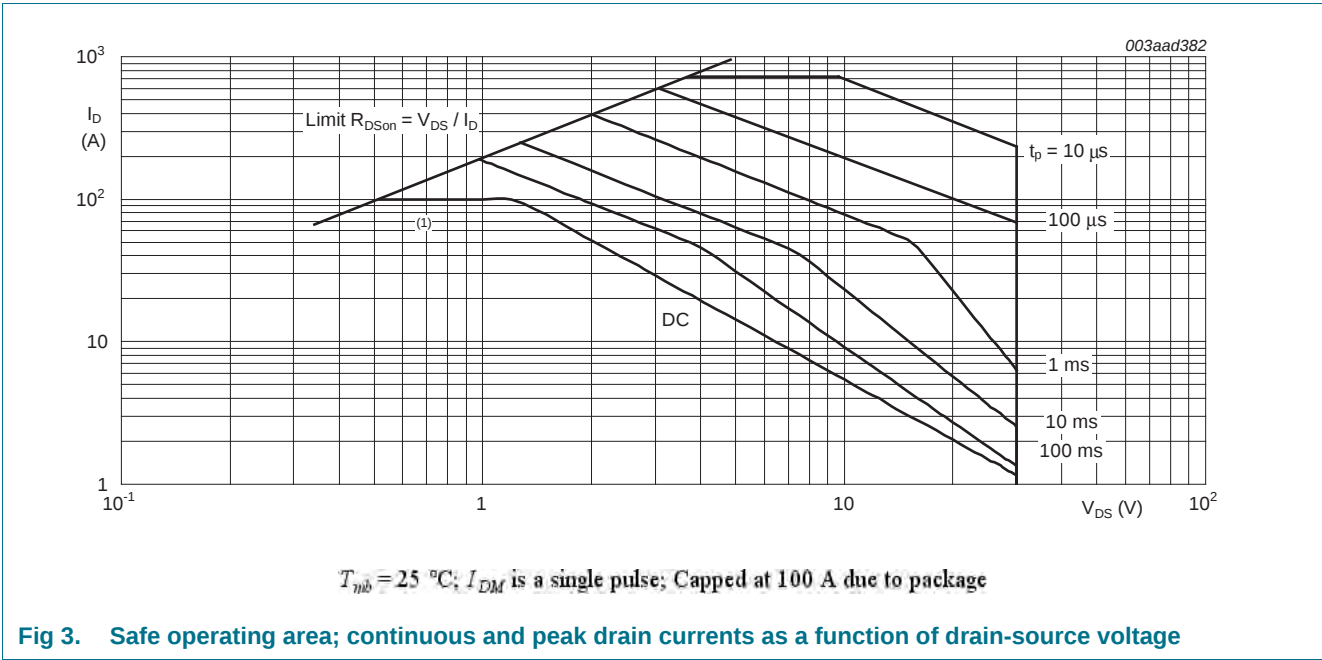
$V_{GS} \geq 10\text{ V}$
(1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

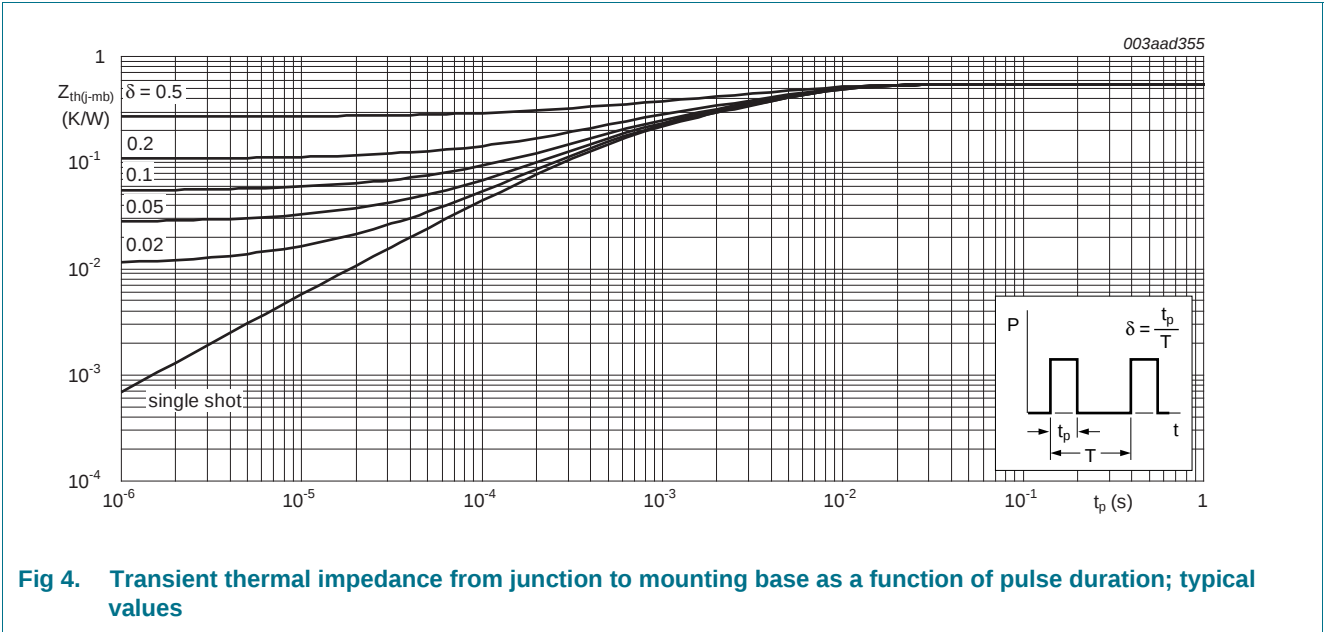
Fig 2. Normalized total power dissipation as a function of mounting base temperature



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.54	0.88	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$; see Figure 10 ; see Figure 11	1.3	1.7	2.15	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 175\ ^\circ C$; see Figure 11	0.5	-	-	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ C$; see Figure 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	0.3	5	μA
		$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_j = 125\ ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; see Figure 12	-	3.16	3.7	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 175\ ^\circ C$; see Figure 13 ; see Figure 12	-	4.88	5.7	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 100\ ^\circ C$; see Figure 13 ; see Figure 12	-	3.6	4.2	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; see Figure 12	-	2.57	3	mΩ
R_G	gate resistance	$f = 1\ MHz$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ A$; $V_{DS} = 15\ V$; $V_{GS} = 10\ V$; see Figure 14 ; see Figure 15	-	66	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	60	-	nC
		$I_D = 25\ A$; $V_{DS} = 15\ V$; $V_{GS} = 4.5\ V$; see Figure 14 ; see Figure 15	-	32	-	nC
Q_{GS}	gate-source charge		-	12	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5.6	-	nC
Q_{GD}	gate-drain charge	$I_D = 25\ A$; $V_{DS} = 15\ V$; $V_{GS} = 4.5\ V$	-	8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ A$; $V_{DS} = 15\ V$; see Figure 14 ; see Figure 15	-	2.6	-	V
C_{iss}	input capacitance	$V_{DS} = 15\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_j = 25\ ^\circ C$; see Figure 16	-	3954	-	pF
C_{oss}	output capacitance		-	822	-	pF
C_{rss}	reverse transfer capacitance		-	356	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ V$; $R_L = 0.5\ \Omega$; $V_{GS} = 4.5\ V$; $R_{G(ext)} = 4.7\ \Omega$	-	46	-	ns

Table 7. Characteristics ...continued
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _r	rise time	V _{DS} = 15 V; R _L = 0.5 Ω; V _{GS} = 4.5 V;	-	82	-	ns
t _{d(off)}	turn-off delay time	R _{G(ext)} = 4.7 Ω	-	74	-	ns
t _f	fall time		-	35	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 17	-	0.7	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	-	40	-	ns
Q _r	recovered charge	V _{DS} = 15 V	-	33	-	nC

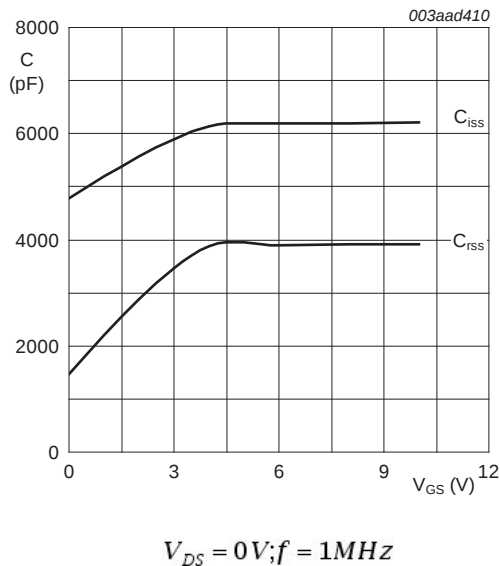


Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

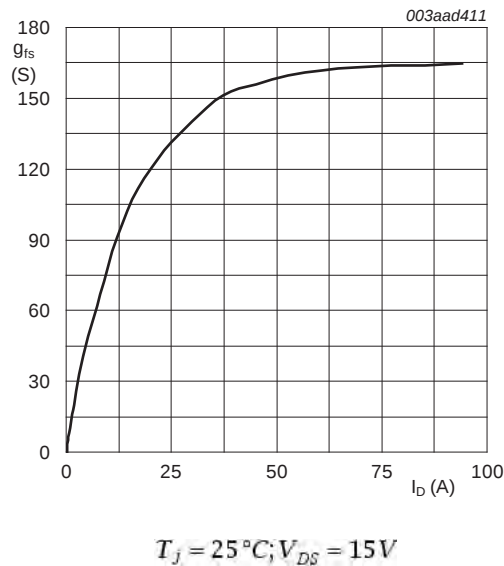
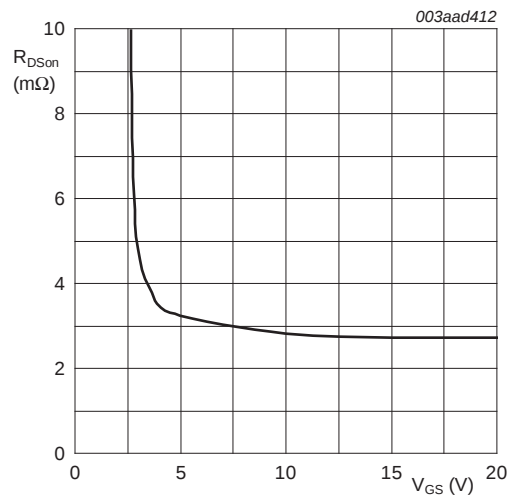
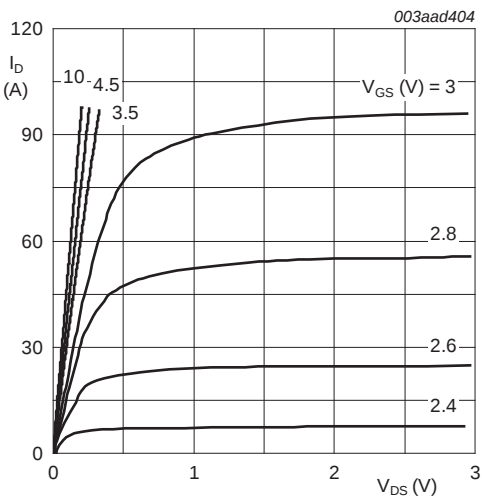


Fig 6. Forward transconductance as a function of drain current; typical values



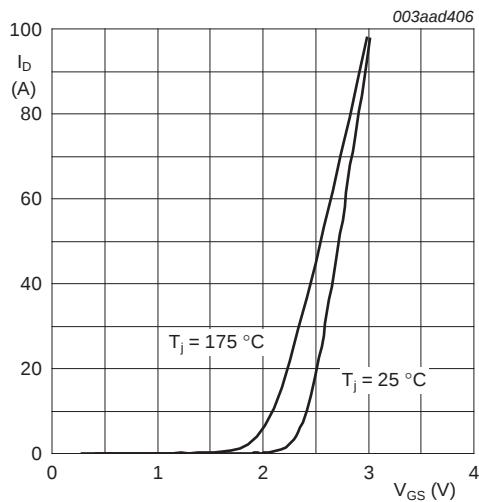
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



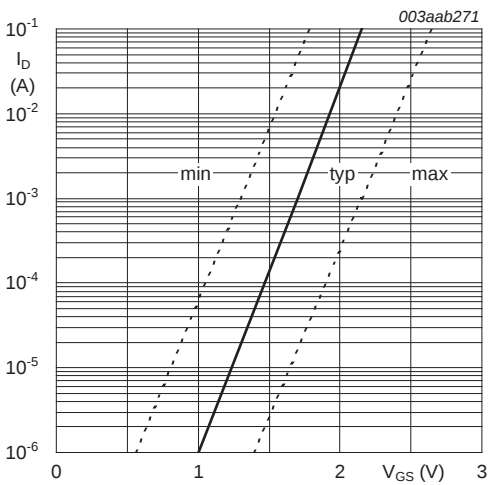
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} > I_D \times R_{DS(on)}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

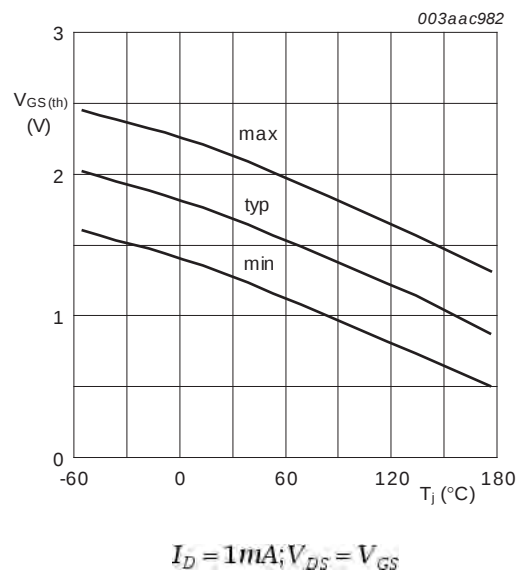


Fig 11. Gate-source threshold voltage as a function of junction temperature

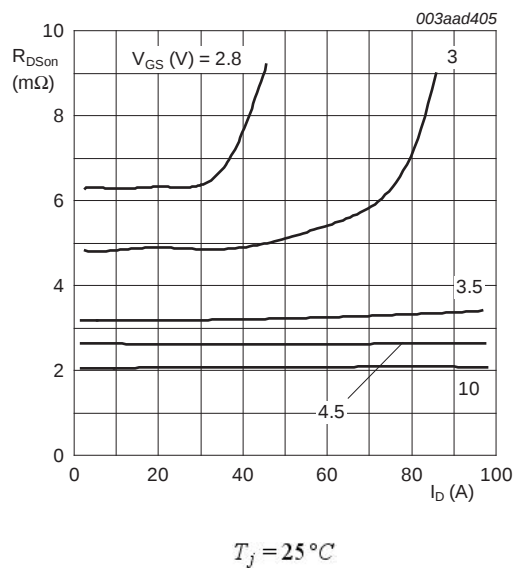


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

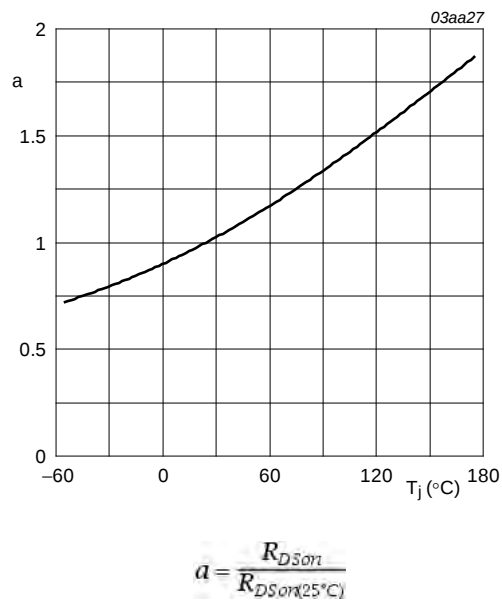


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

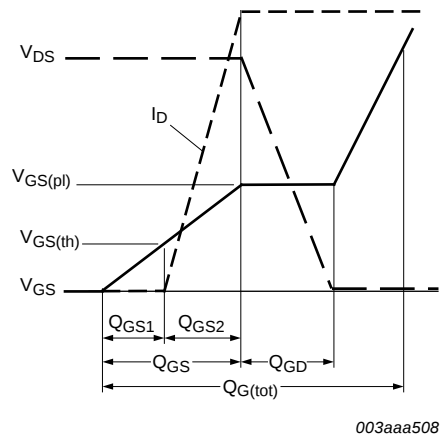
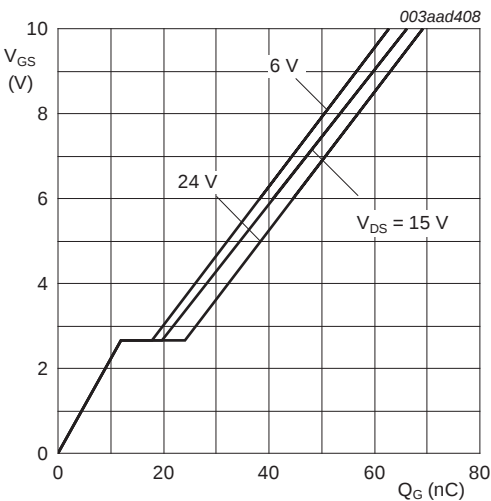
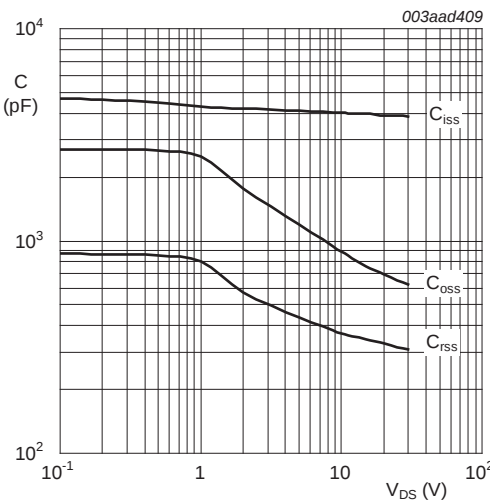


Fig 14. Gate charge waveform definitions



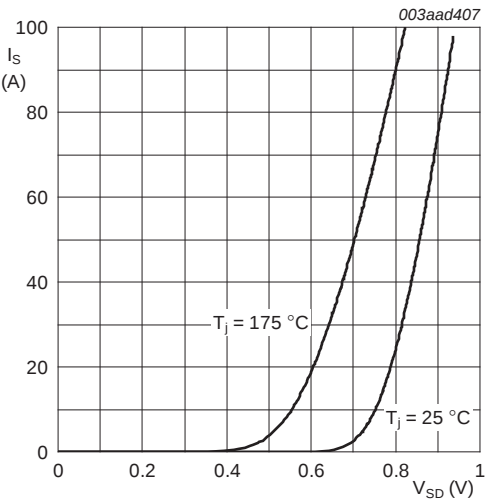
$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

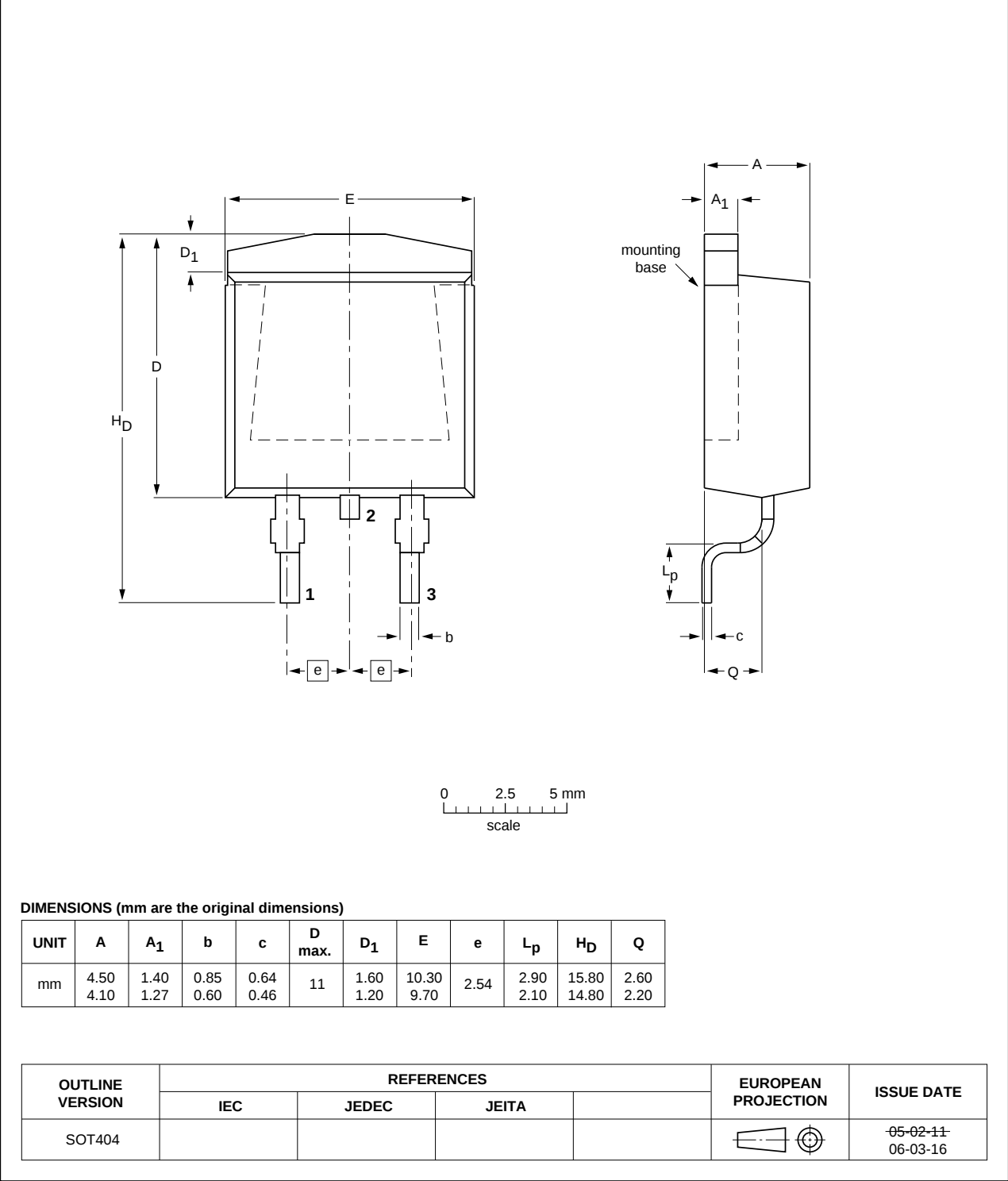


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R7-30BL v.1	20120321	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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For sales office addresses, please send an email to: salesaddresses@nxp.com

12. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	3
6	Thermal characteristics	5
7	Characteristics	6
8	Package outline	11
9	Revision history	12
10	Legal information	13
10.1	Data sheet status	13
10.2	Definitions	13
10.3	Disclaimers	13
10.4	Trademarks	14
11	Contact information	14

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