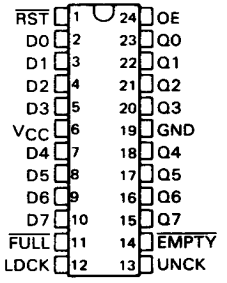
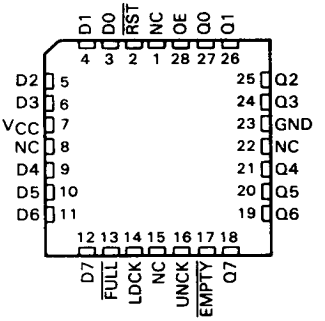
D3091, FEBRUARY 1988—REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 8 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typ**
- **3-State Outputs**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This 512-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not effect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232A is characterized for operation from 0°C to 70°C.

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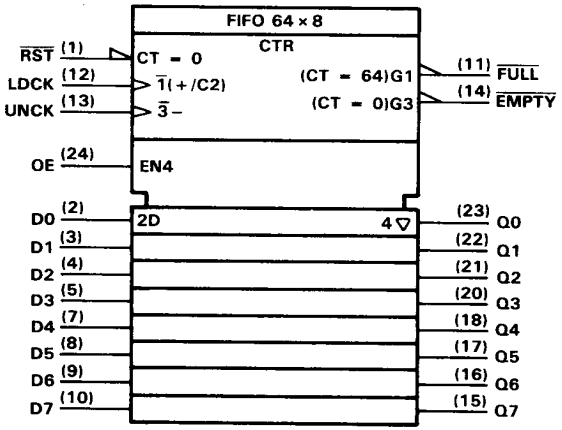
D3091, FEBRUARY 1988—REVISED MARCH 1990

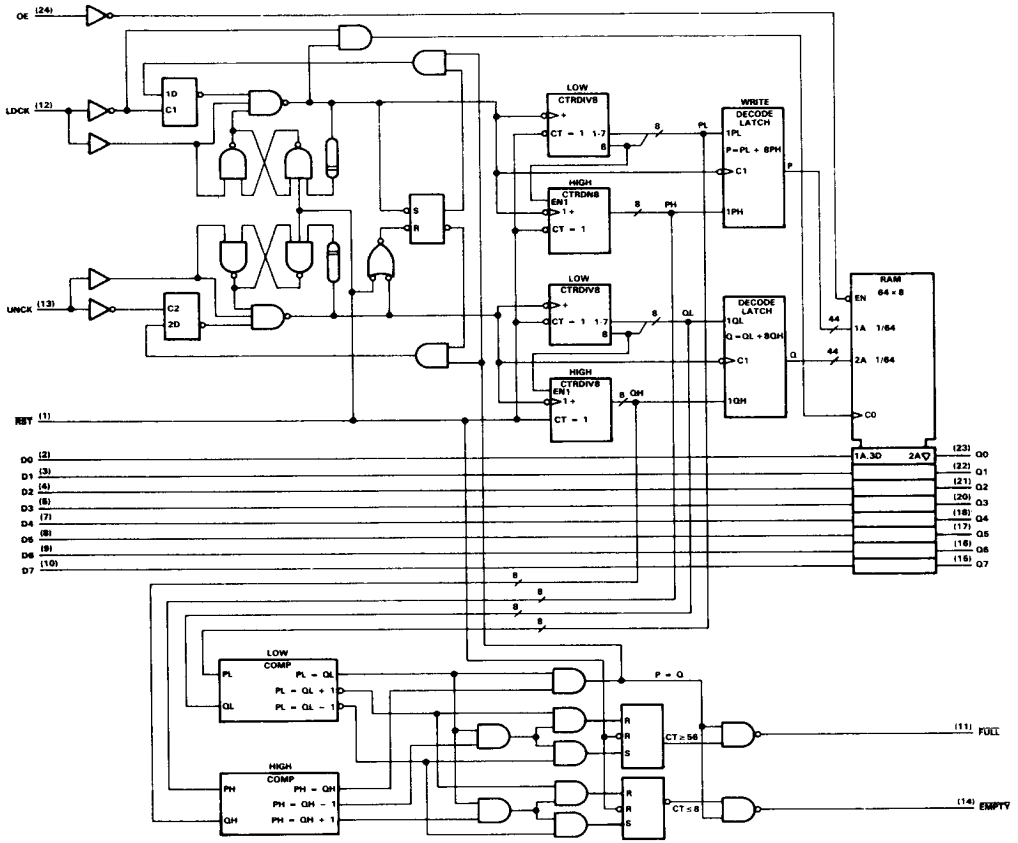
logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

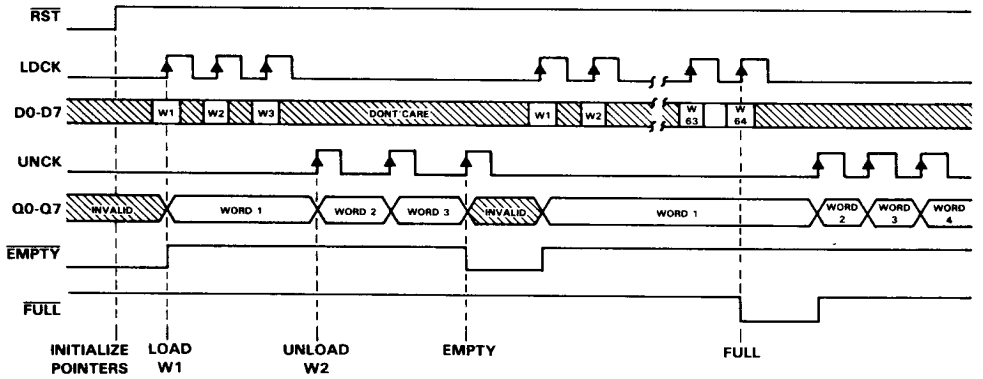
Pin numbers shown are for the NT package.

logic diagram (positive logic)



Pin numbers shown are for the NT package.

timing diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC} − 2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	CLKS	V_{CC} = 5.5 V,	V_{IN} = 0.4 V			−0.2	mA
	Others					−0.1	
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	$\overline{FULL}$, $\overline{EMPTY}$			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	270	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

Note 1: Load circuit and voltage waveforms are shown in Section 1.

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