CX65002

700 – 1400 MHz Linear Power Amplifier Driver

Skyworks' CX65002 Microwave Monolithic Integrated Circuit (MMIC) power amplifier driver offers a desirable combination of features that provide superb performance and ease of use in a low-cost Surface-Mounted Technology (SMT) package. The Gallium Arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) power amplifer driver was developed and optimized for extreme linear performance in a variety of applications. It is ideal as a driver or output stage for transceivers and repeaters in AMPS/CDMA/TDMA/GSM paging base stations, mobile radios, telematics, and many other applications.

Figure 1 shows a functional block diagram for the CX65002. The device package and pinout are shown in Figure 2.

Features

- 5 V single supply operation
- Linear Pout of 24 dBm
- OIP3 of 47 dBm
- Excellent CDMA performance
- Internal bias circuits
- Surface mounted Small Outline Integrated Circuit (SOIC) 8-pin package with downset ground paddle

Applications

- AMPS/CDMA/TDMA/GSM
- Wireless Local Loop (WLL) and Industrial, Scientific, Medical (ISM) bands
- Repeaters
- Paging
- Mobile radios
- Telematics
- UHF TV broadcast

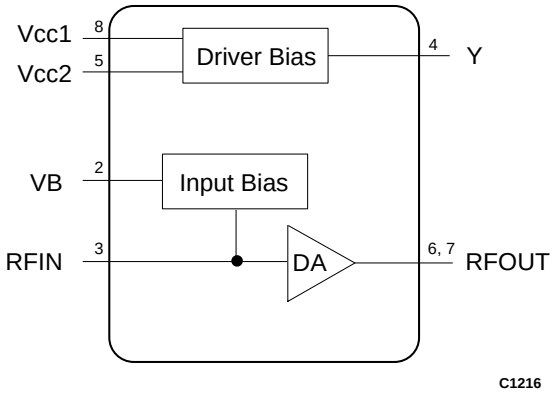


Figure 1. CX65002 Functional Block Diagram

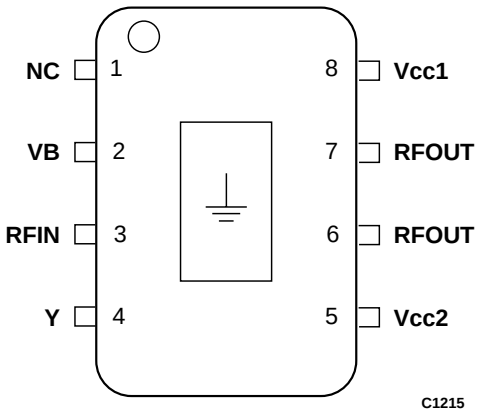


Figure 2. CX65002 Pinout – 8-Pin SOIC Package (Top View)

Electrical and Mechanical Specifications

The signal pin assignments and functions are described in Table 1. The absolute maximum ratings of the CX65002 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics of the CX65002 are illustrated in Figures 3 through 12.

Table1. CX65002 Signal Descriptions

Pin #	Name	Description
1	NC	No connection
2	VB	Input bias for driver amplifier
3	RFIN	RF input
4	Y	Output of internal bias circuit
5	Vcc2	Supply voltage
6	RFOUT	RF output
7	RFOUT	RF output
8	Vcc1	Supply voltage
9	GND	Ground

Table 2. CX65002 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
RF input power	P_{IN}			10	dBm
Supply voltage	Vcc			5.5	V
Supply current (I_D + I_{BIAS})	I_{CC}			240	mA
Power dissipation				1.3	W
Case operating temperature	T_C	–40		+85	°C
Storage temperature	T_{ST}	–55		+125	°C
Junction temperature	T_J			150	°C
Note: No damage to device if only one parameter is applied at a time with other parameters at nominal conditions.					

Table 3. CX65002 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	Vcc		5		V
Frequency range	F	700		1400	MHz
Junction temperature	T_J			140	°C
Maximum bias condition =	$(Vcc \times I_D) < (T_{J\_RECOMMENDED} – T_C)/R_{TH,J-C}$				

Table 4. CX65002 Electrical Characteristics
(Vcc = 5 V, T_C = 25 °C)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
OIP3 Match, Frequency = 900 MHz (Note 1)						
Quiescent current (I_D + I_{BIAS})	Iq	R_{BIAS} = 270 Ω		120	130	mA
Small signal gain	G	P_{IN} = –15 dBm	16.5	18		dB
Linear output power (Note 2)	P_{OUT}	P_{IN} = +7 dBm	22.5	24		dBm
Power Added Efficiency	PAE	P_{IN} = +7 dBm	38	44		%
Noise Figure (NF)	NF			5	6	dB
Output IP3	OIP3	Two CW tones with 1 MHz spacing P_{IN} = –12 dBm per tone	44	47		dBm
Thermal resistance (junction – case)	$R_{TH,J-C}$			91		°C/W
ACP Match, Frequency = 881.5 MHz (Note 3)						
Quiescent current (I_D + I_{BIAS})	Iq	R_{BIAS} = 330 Ω		90	105	mA
Small signal gain	G	P_{IN} = –15 dBm	15.5	17		dB
Peak envelope power (Note 2)	P_{PEP}	IS95 downlink CDMA signal, 9 ch Fwd, P_{IN} = 3 dBm		29		dBm
Average output power @ ACPR = –45 dBc, 750 kHz offset	$P_{OUTACPR}$	IS95 downlink CDMA signal, 9 ch Fwd, P_{IN} = 4.5 dBm	20.5	21.5		dBm

Note 1: Device matched for optimum OIP3 according to circuit shown in Figure 13.

Note 2: For reliable operation, do not violate the maximum input drive level specified in Table 2.

Note 3: Device matched for optimum ACP according to circuit shown in Figure 14.

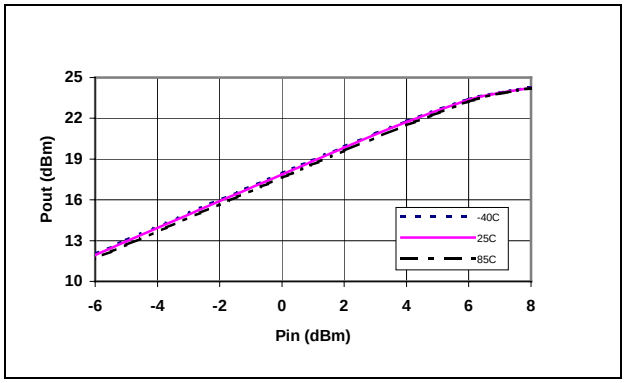


Figure 3. Typical Pout vs Pin @ 900 MHz Over Temperature (Circuit Match for Optimum OIP3)

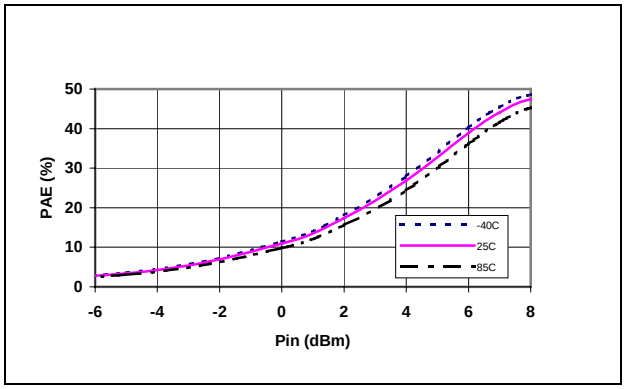


Figure 4. Typical PAE vs Pin @ 900 MHz Over Temperature (Circuit Match for Optimum OIP3)

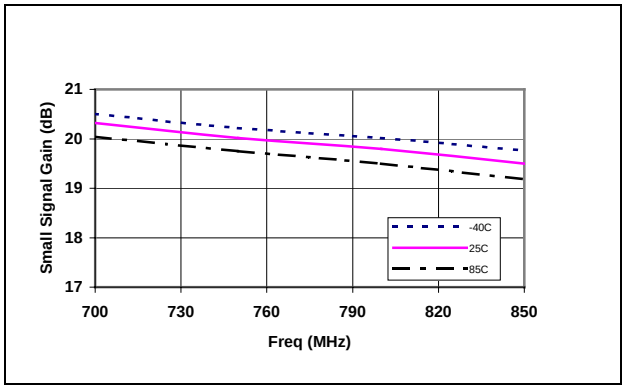


Figure 5. Typical Small Signal Gain From 700 to 850 MHz Over Temperature (Circuit Match for Optimum Gain)

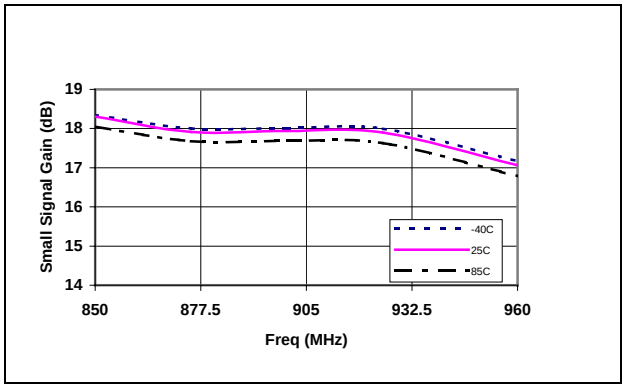


Figure 6. Typical Small Signal Gain From 850 to 960 MHz Over Temperature (Circuit Match for Optimum OIP3)

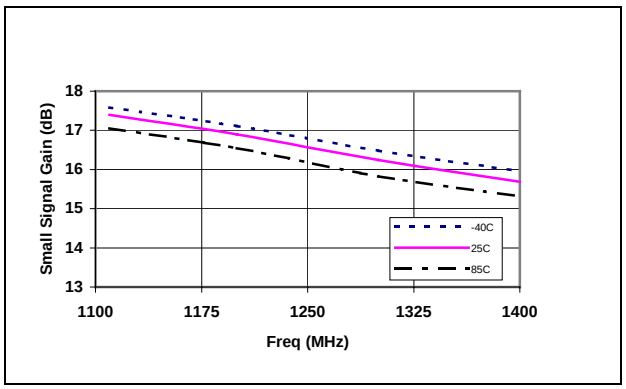


Figure 7. Typical Small Signal Gain From 1.1 to 1.4 GHz Over Temperature (Circuit Match for Optimum Gain)

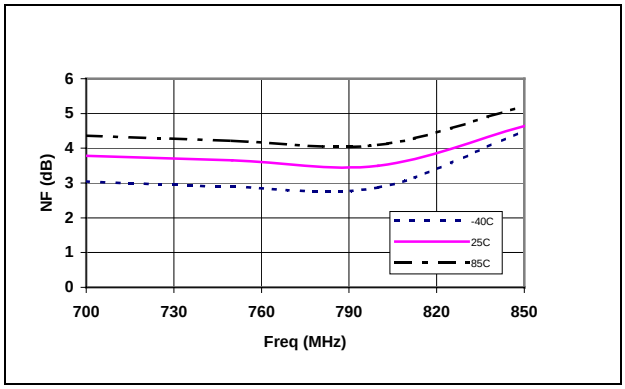


Figure 8. Typical NF From 700 to 850 MHz Over Temperature (Circuit Match for Optimum Gain)

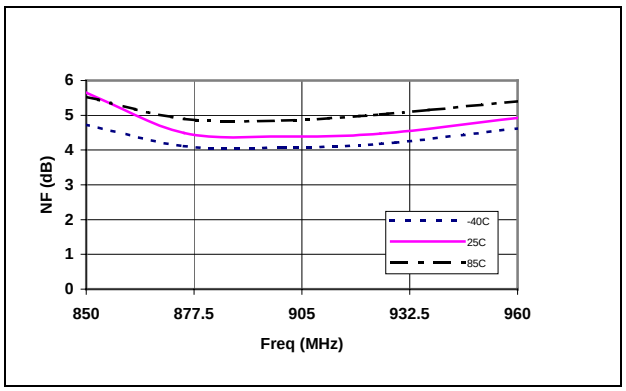


Figure 9. Typical NF From 850 to 960 MHz Over Temperature (Circuit Match for Optimum OIP3)

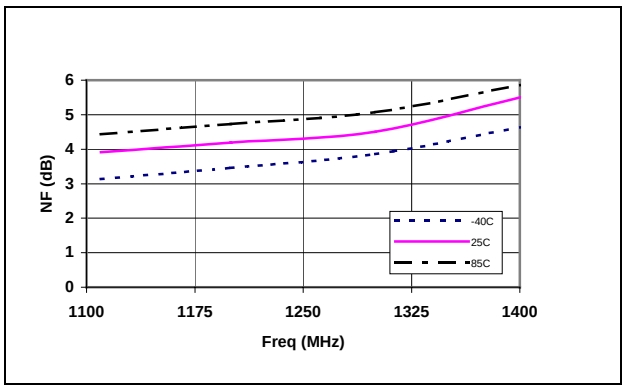


Figure 10. Typical NF From 1.1 to 1.4 GHz Over Temperature (Circuit Match for Optimum Gain)

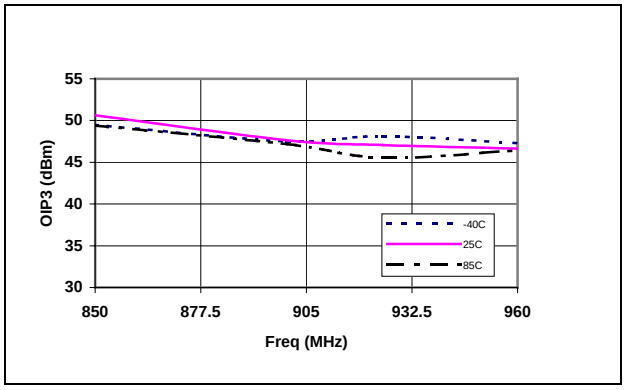


Figure 11. Typical OIP3 vs Frequency Over Temperature (Circuit Match for Optimum OIP3)

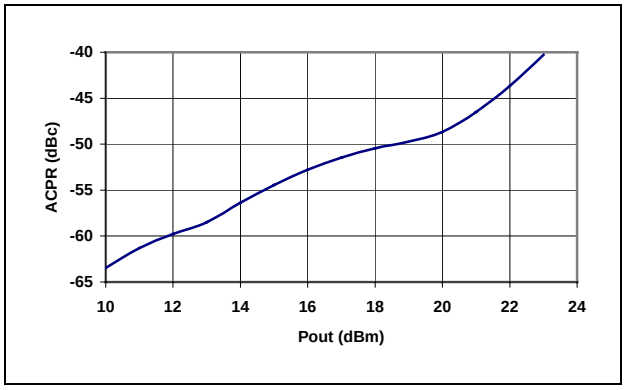


Figure 12. Typical ACPR vs Pout @ 881.5 MHz, 750 kHz Offset, 25 °C (Circuit Match for Optimum ACPR)

Evaluation Board Description

The CX65002 Evaluation Board is used to test the CX65002 power amplifier's performance. The CX65002 Evaluation Board schematic diagrams are shown in Figures 13 and 14 (optimized for OIP3 and ACPR, respectively). The Evaluation Board assembly diagram is shown in Figure 15 and the Evaluation Board layer detail is shown in Figure 16. Figure 17 provides the mounting footprint for the CX65002.

Circuit Design Configurations

The following design considerations (refer to Figure 13) need to be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.
2. The ground pad of the CX65002 power amplifier has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the amplifier. As such, design the connection to the ground pad to dissipate the maximum wattage produced to the circuit board. Multiple vias to the grounding layer are required (see Figures 16 and 17).

Note: Junction temperature (T_J) of the device increases with a poor connection to the slug and ground. This reduces the lifetime of the device.

3. Five external bypass capacitors, a 1 µF, 1000 pF, and three 39 pF capacitors, are required on the Vcc line, and on pin 4, pin 5, and pin 8. Capacitors C7 (39 pF) and C8 (1 µF) are placed in parallel between the supply line and ground, C4 (1000 pF) is placed between pin 4 and ground, C5 (39 pF) is placed between pin 8 and ground, and C6 (39 pF) is placed between pin 5 and ground. The best linearity of the CX65002 is achieved when bypass capacitor C8 (1 µF) is place at 1/8 wave length at 900 MHz from the RF output pins (pin 6 and pin 8).
4. A bias resistor, R1 (270 Ω) is used to control Vcc1 (reference voltage of the bias circuit) at pin 8. The nominal total current with a 270 Ω bias resistor is 125 mA with Vcc1 and Vcc2 equal to 5 V. Resistor R2 (0 Ω) is placed between the RF output transmission line and Vcc supply voltage line.
5. Inductor L2 (33 nH) is placed between pin 4 (bias circuit output) and pin 2 (base of RF transistor) for bias circuit and RF transistor connection.
6. Inductor L1 (3.9 nH) and capacitor C1 (4.7 pF) are the input matching components and capacitor C10 (15 pF) is the output matching component. Use a short transmission line (about 100 mils) between the RF input pin (pin 3) and the RF input matching components (C1 and L1). Also use a short output transmission (about 100 mils) line between the RF output pins (pin 6 and pin 7) and the RF output matching component (C10).

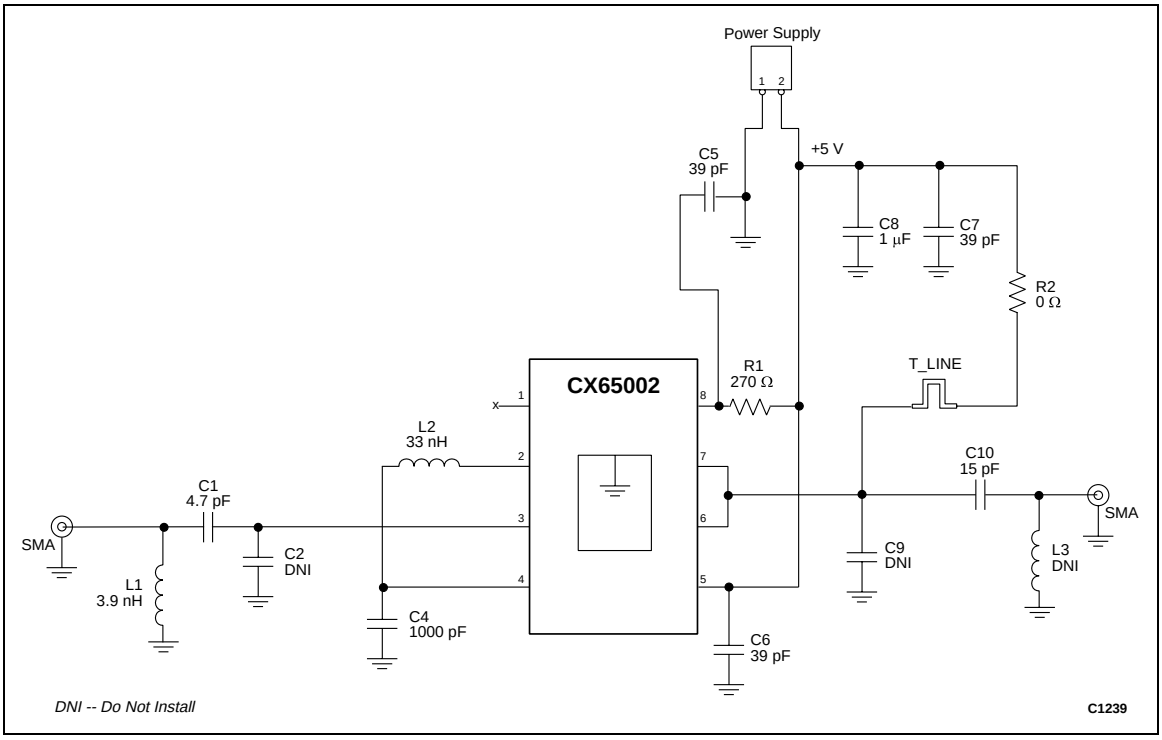


Figure 13. Application Schematic Optimized for OIP3 @ 900 MHz

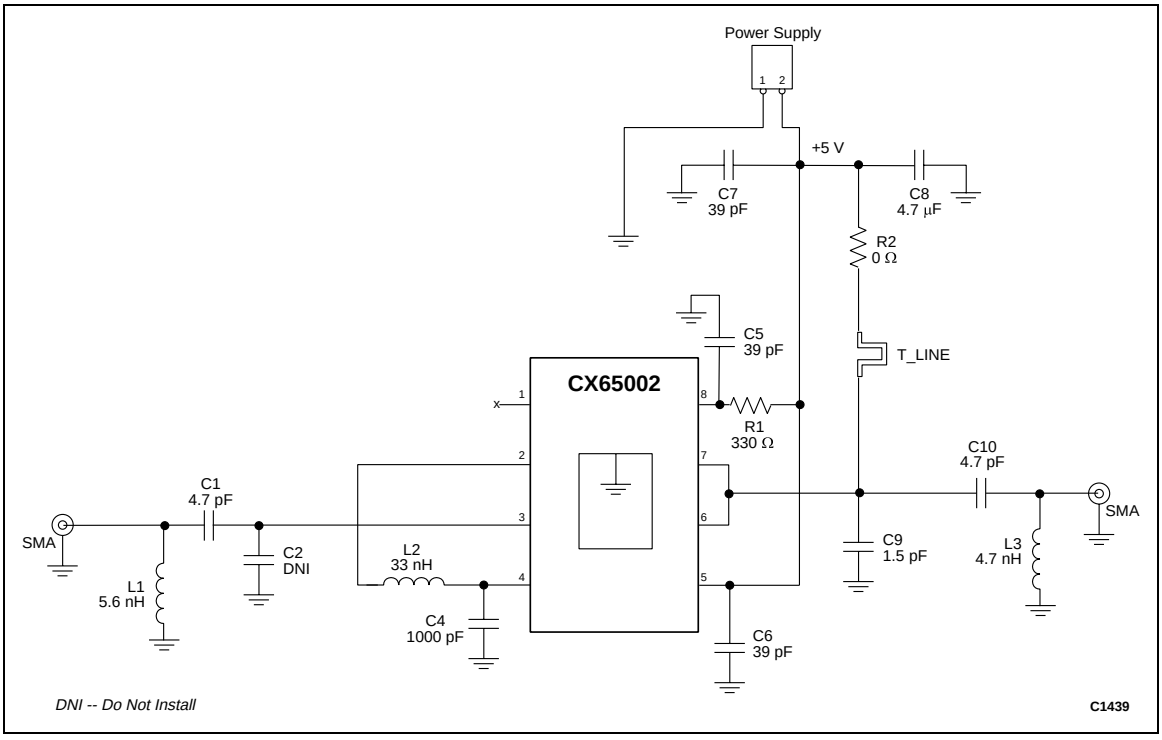


Figure 14. Application Schematic Optimized for ACPR @ 881.5 MHz

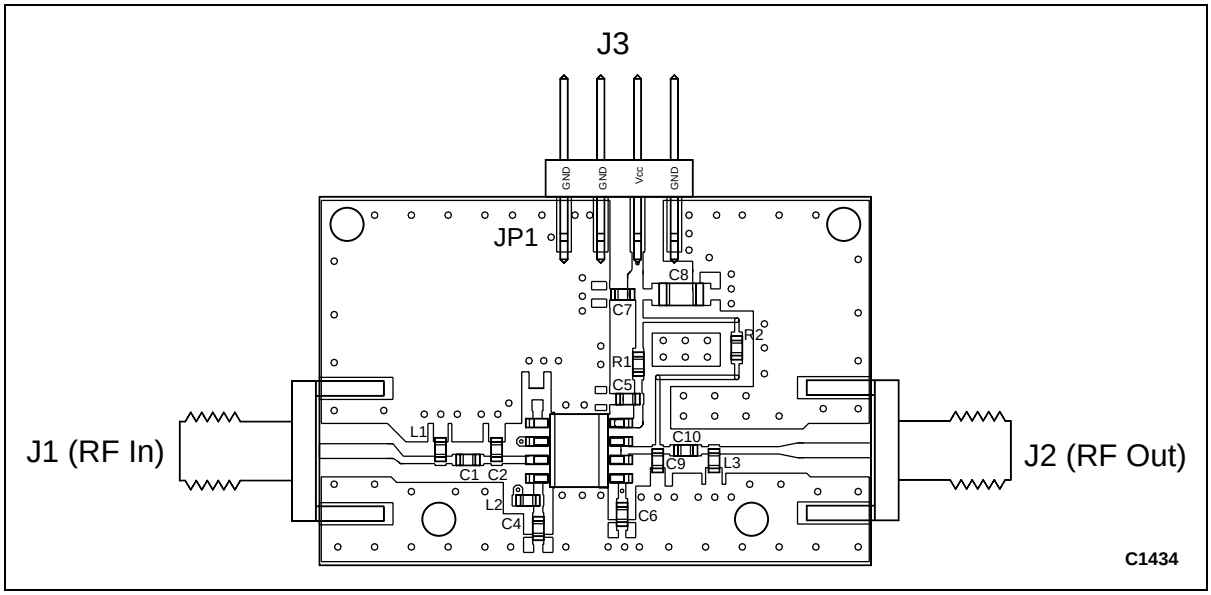
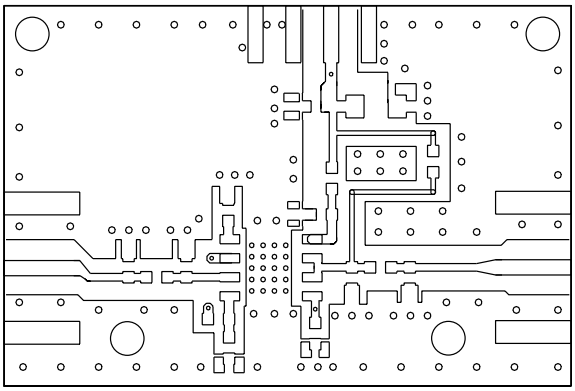
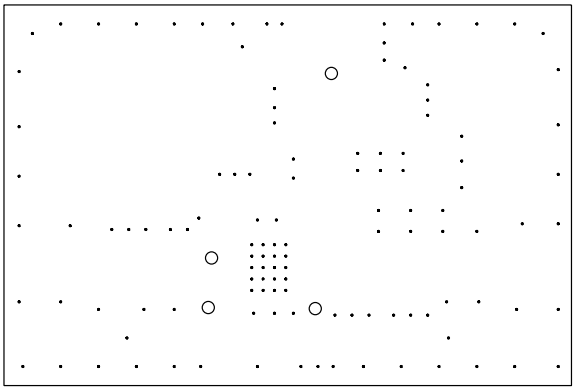


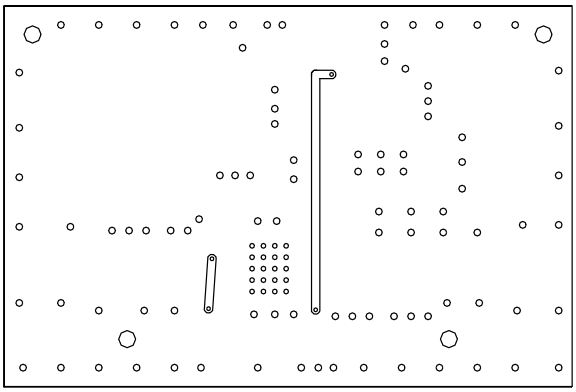
Figure 15. Evaluation Board Assembly Diagram



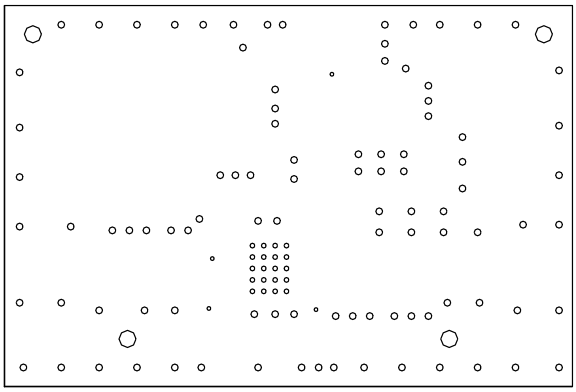
Layer 1: Top Metal



Layer 2: Ground



Layer 3: Inner Traces



Layer 4: Ground

C1440

Figure 16. Evaluation Board Layer Detail

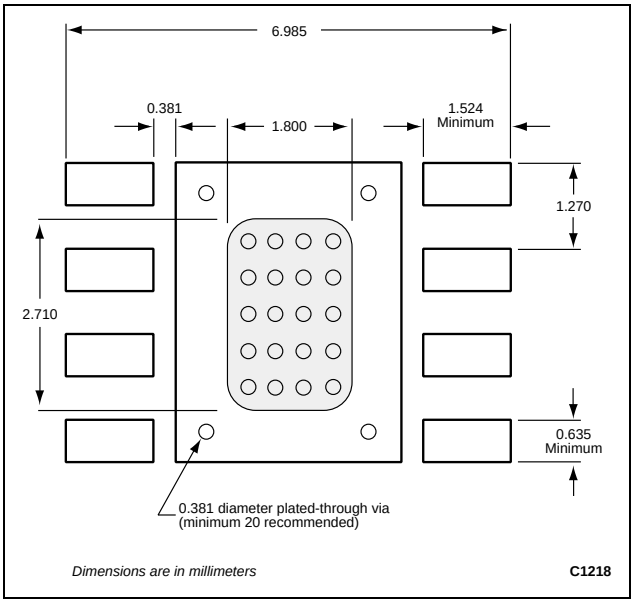


Figure 17. PCB Mounting Footprint

Testing Procedure

Use the following procedure to set up the CX65002 Evaluation Board for testing. Refer to Figure 18 for guidance:

1. Connect a 5.0 V supply to Vcc. If available, enable the current limiting function of the power supply to 240 mA.
2. Connect a signal generator to the RF signal input port. Set it to the desired RF frequency at a power level of –15 dBm or less to the Evaluation Board but do NOT enable the RF signal.
3. Connect a spectrum analyzer to the RF signal output port.
4. Enable the power supply.
5. Enable the RF signal and take measurements.

Caution: *If any of the input signals exceed the rated maximum values, the CX65002 Evaluation Board can be permanently damaged.*

Package Dimensions

Figure 19 shows the package dimensions for the 8-pin SOIC and Figure 20 provides the tape and reel dimensions.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second. Maximum temperature should not exceed 225 °C and the time spent at a temperature that exceeds 210 °C should be limited to less than 10 seconds. If the part is manually attached, precaution should be taken to ensure that the part is not subjected to a temperature that exceeds 300 °C for more than 10 seconds.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. For additional details on both attachment techniques, precautions, and recommended handling procedures, refer to the Skyworks document *Solder Reflow Application Note*, document number 101536.

Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks document *Tape and Reel Information Application Note*, document number 101568.

Electro-Static Discharge (ESD) Sensitivity

The CX65002 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

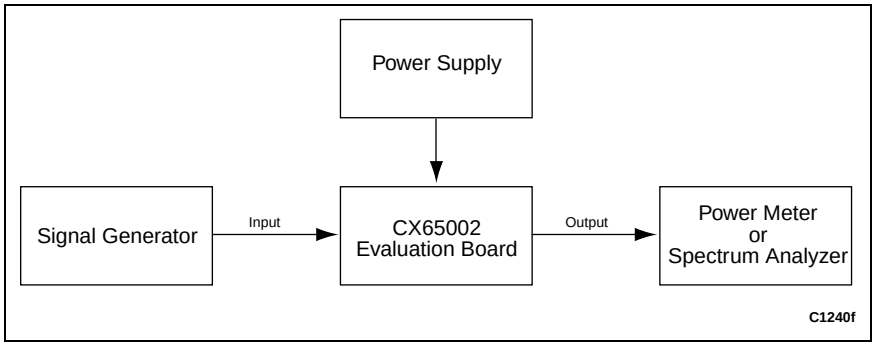


Figure 18. CX65002 Evaluation Board Testing Configuration

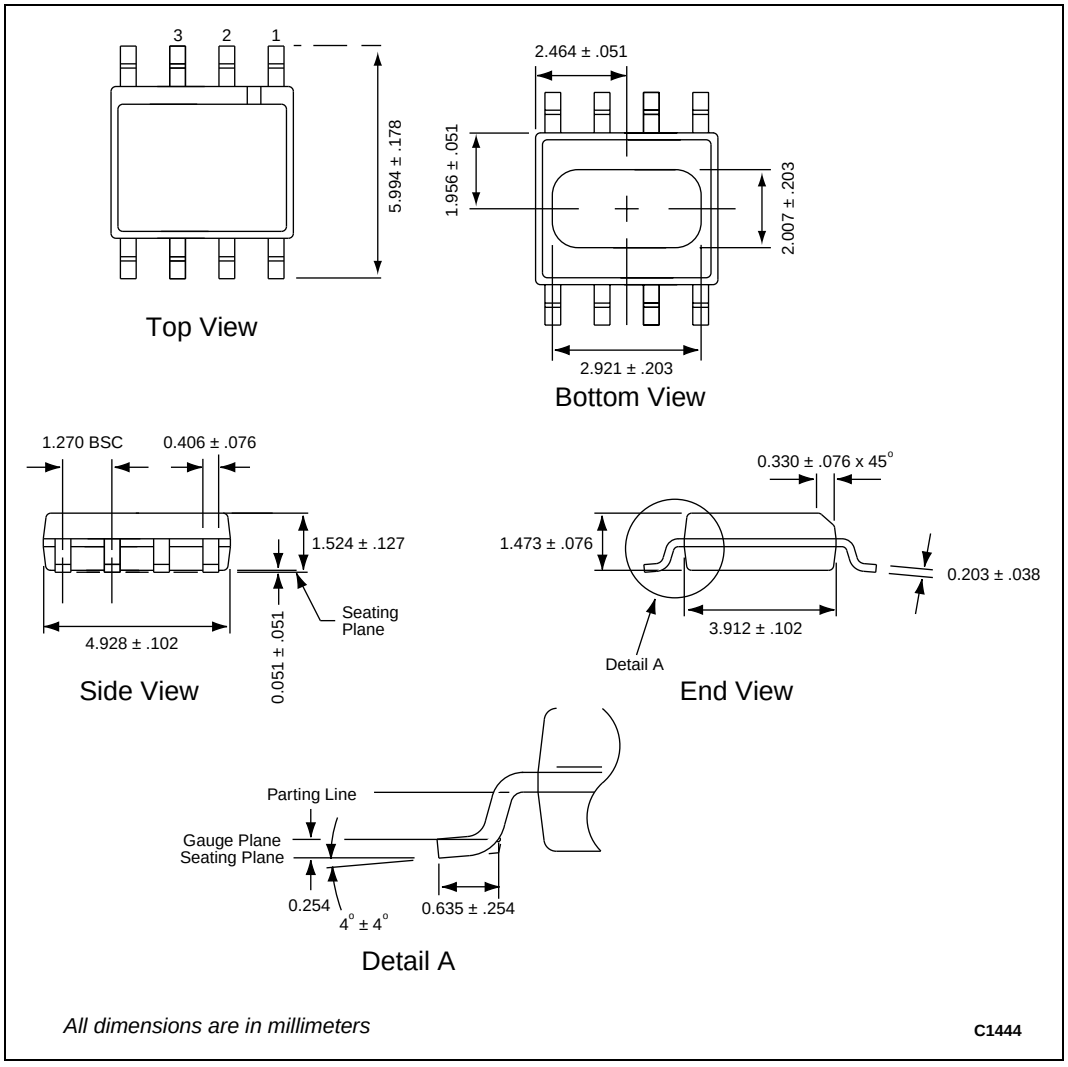


Figure 19. CX65002 8-Pin SOIC Package Dimension Drawing

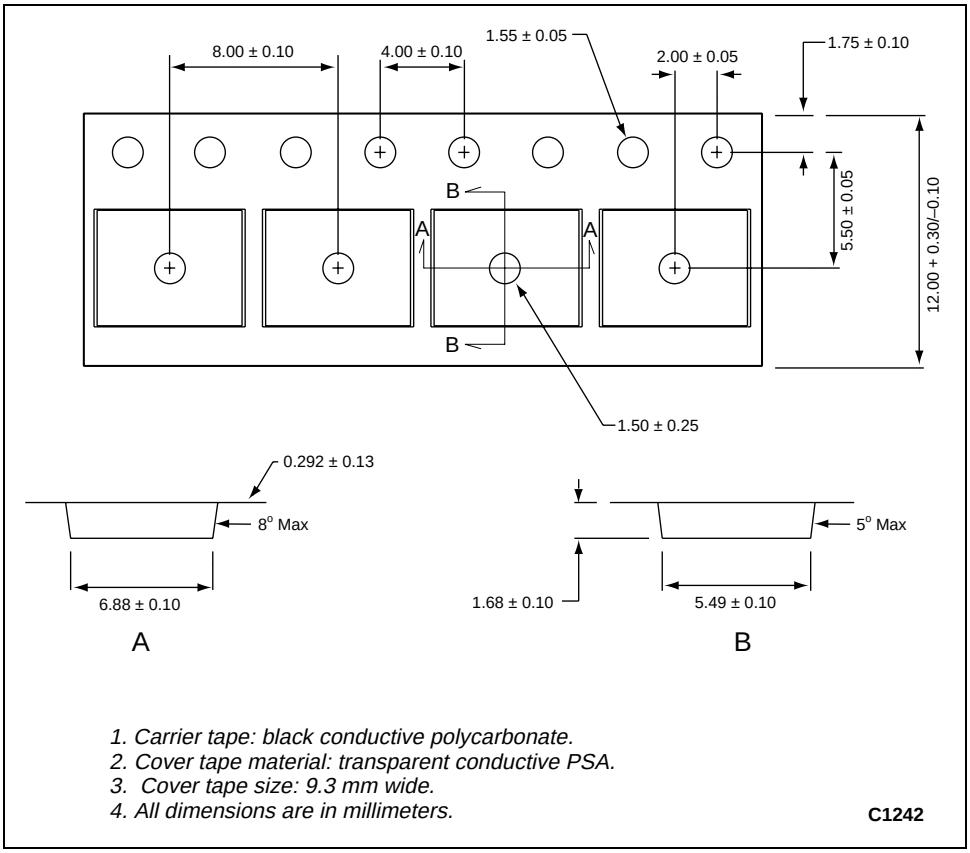


Figure 20. CX65002 8-Pin SOIC Tape and Reel Dimensions

Ordering Information

Model Name	Ordering Part Number	Evaluation Kit Part Number
CX65002 700-1400 MHz Linear Power Amplifier Driver	CX65002-12	TW10-D252 (tuned for optimum OIP3 @ 900 MHz) (see Figure 13) TW10-D253 (tune for optimum ACPR @ 881.5 MHz) (see Figure 14)

General Information:

Skyworks Solutions, Inc.
4311 Jamboree Rd.
Newport Beach, CA 92660-3007

www.skyworksinc.com