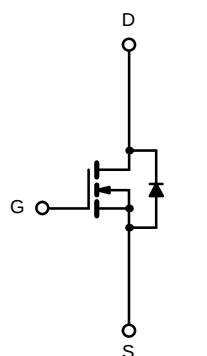
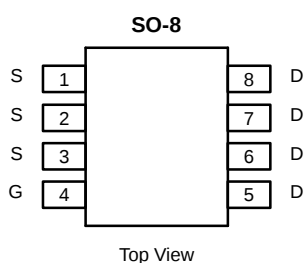




N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.420 @ $V_{GS} = 10$ V	± 1.7

High-Efficiency
PWM Optimized



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^{a, b}	$T_A = 25^\circ\text{C}$	I_D	± 1.7	A
	$T_A = 70^\circ\text{C}$		± 1.3	
Pulsed Drain Current		I_{DM}	± 12	
Avalanche Current		I_{AS}	± 12.5	mJ
Single Avalanche Energy		E_{AS}	8	
Continuous Source Current (Diode Conduction) ^{a, b}		I_S	2.1	A
Maximum Power Dissipation ^{a, b}	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}		50	$^\circ\text{C/W}$
	Steady State		80		

Notes

- a. Surface Mounted on FR4 Board.
b. $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

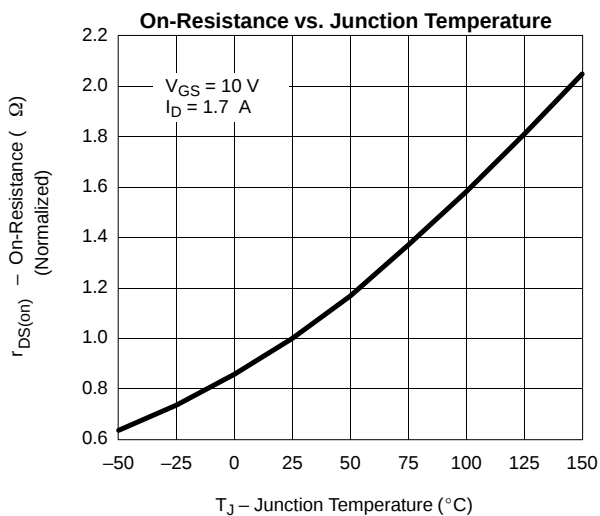
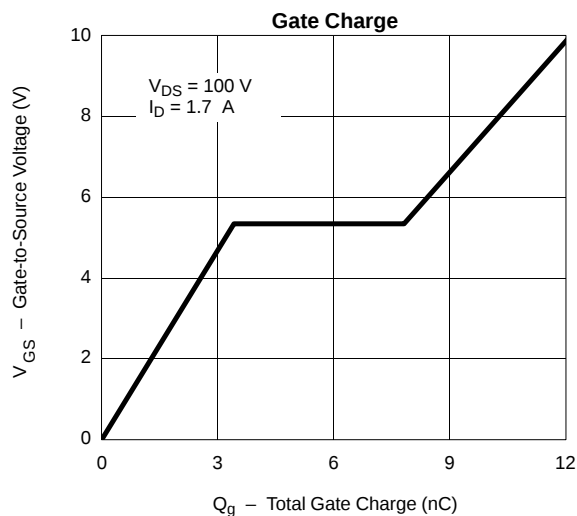
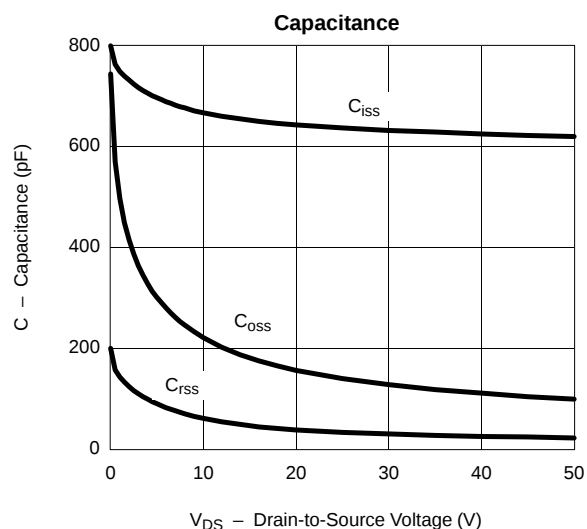
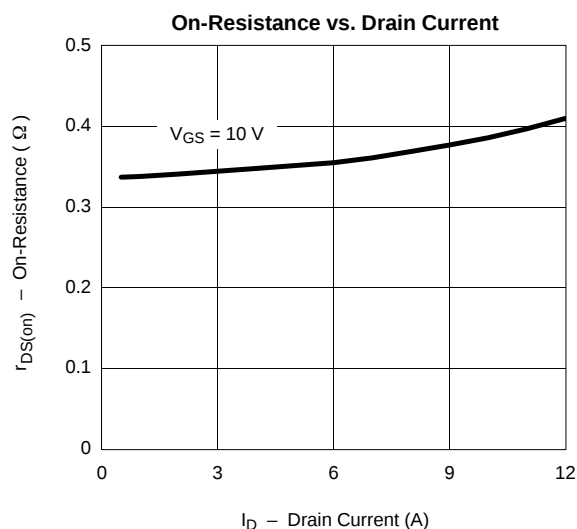
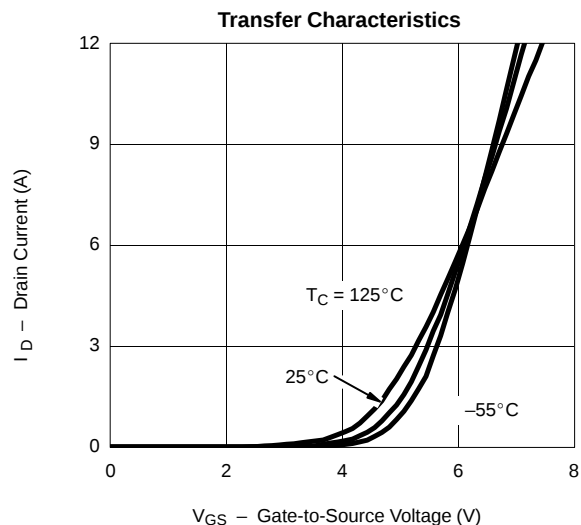
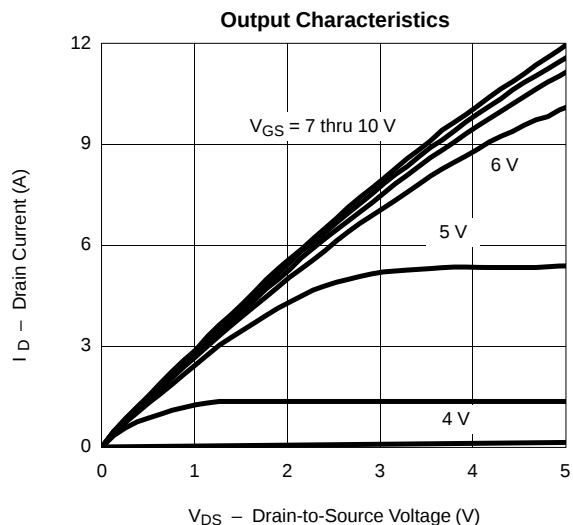
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 160 V, V _{GS} = 0 V			1	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 55 °C			25	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	5			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 1.7 A		0.340	0.420	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.7 A		3.5		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.1 A, V _{GS} = 0 V		0.95	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 100 V, V _{GS} = 10 V, I _D = 1.7 A		13	25	nC
Gate-Source Charge	Q _{gs}			3.5		
Gate-Drain Charge	Q _{gd}			4.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, R _L = 100 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		10	20	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			20	40	
Fall Time	t _f			25	50	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.1 A, di/dt = 100 A/μs		115	150	

Notes

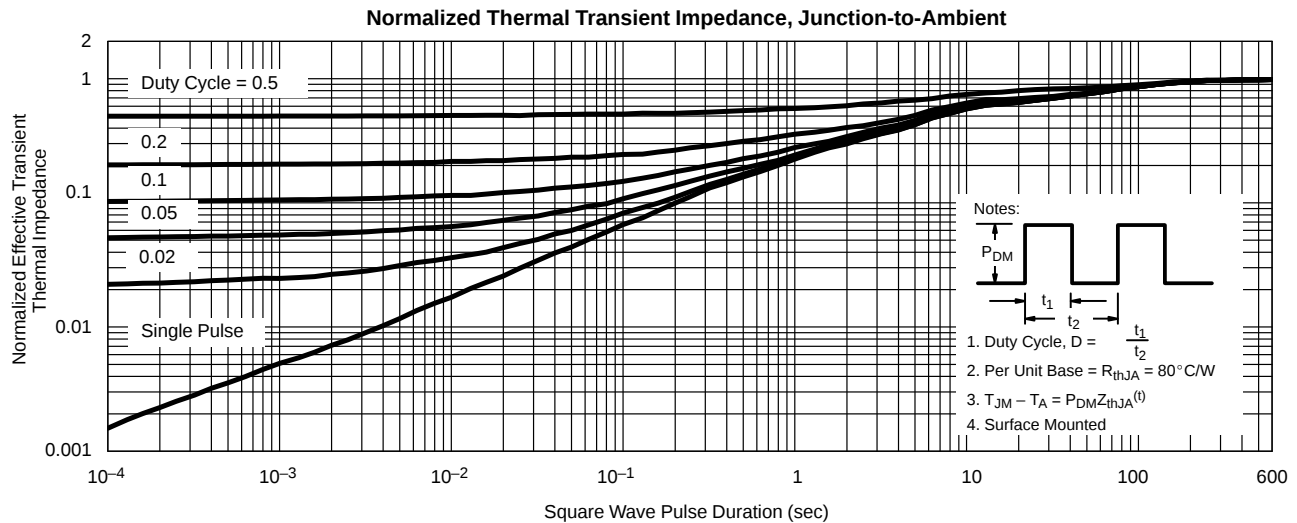
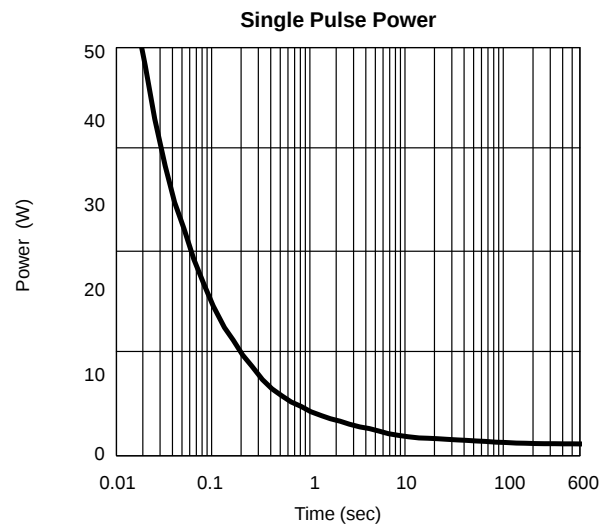
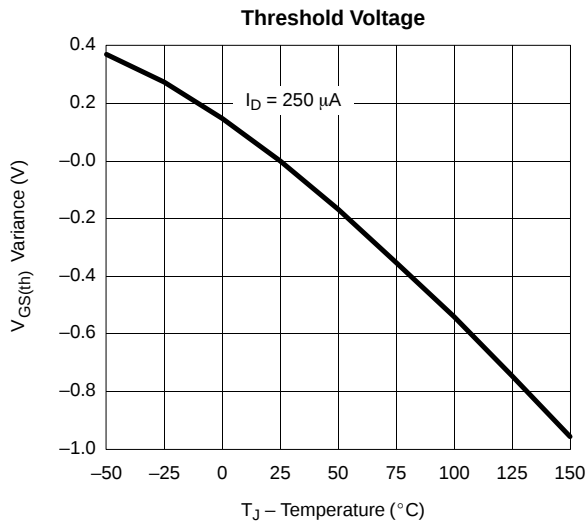
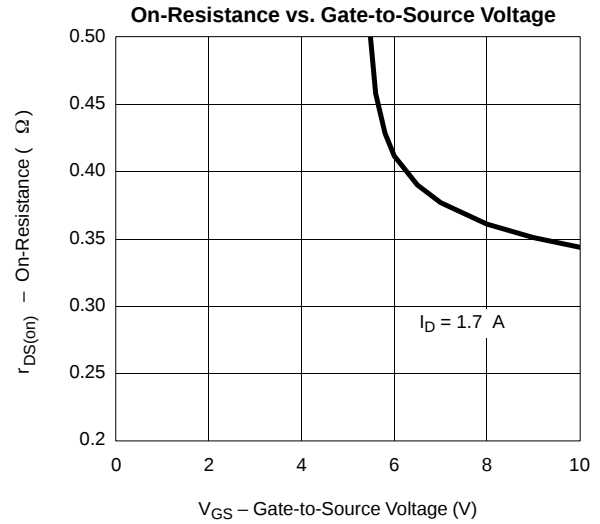
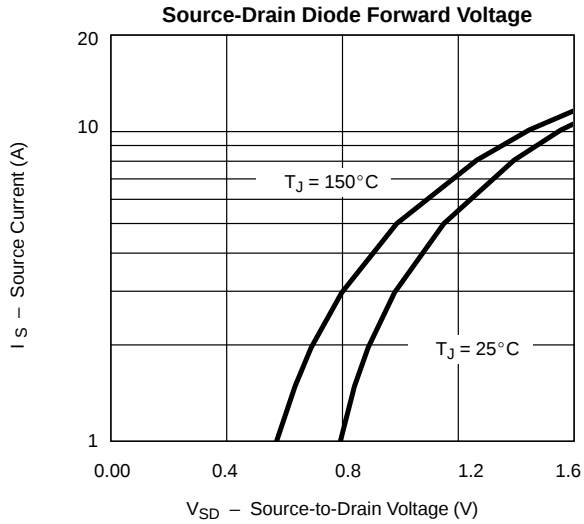
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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