

3.3V ABT Octal Transceiver/register, non-inverting (3-State)

74LVT652

NAPC/PHILIPS SEMICON

63E D

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus

- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6 and 200V per Machine Model

DESCRIPTION

The LVT652 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT652 transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, OEBA) and Select (SAB, SBA) pins are provided for bus management.

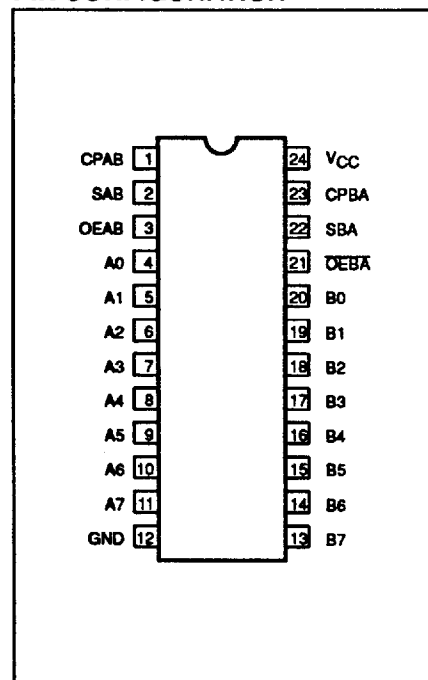
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; $GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$; $V_{CC} = 3.3V \pm 0.3V$	2.8	ns
C_{IN}	Input capacitance	$V_I = 0V$ or $3V$	4.5	pF
C_{IO}	I/O capacitance	$V_I = 0V$ or $3V$	11	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	.13	mA

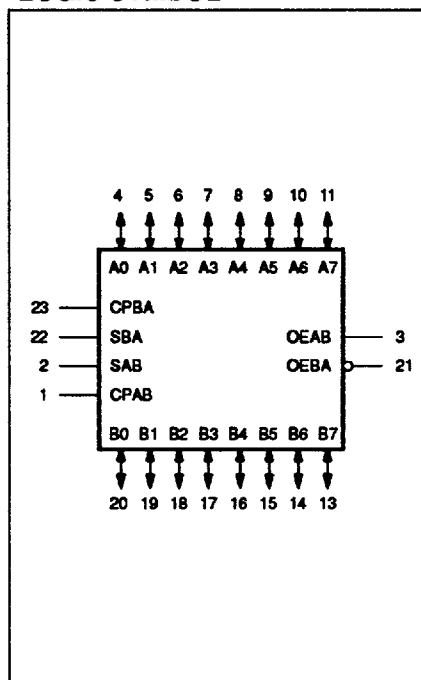
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Small Outline Large (300mil) (SOL)	-40°C to $+85^{\circ}\text{C}$	74LVT652D	0172D
24-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to $+85^{\circ}\text{C}$	74LVT652DB	1640A
24-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to $+85^{\circ}\text{C}$	74LVT652PW	TBD

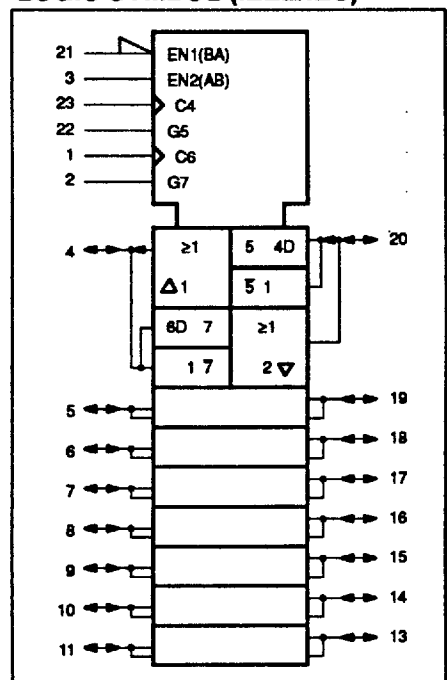
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / OEBA	A to B Output Enable input / B to A Output Enable input (active-Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	OEBA	CPAB	CPBA	SAB	SBA	A _n	B _n	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified** Output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified** Output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H H	L L	H or L H or L	H or L H or L	H H	H H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level

L = Low voltage level

X = Don't care

↑ = Low-to-High clock transition

* The data output function may be enabled or disabled by various signals at the OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

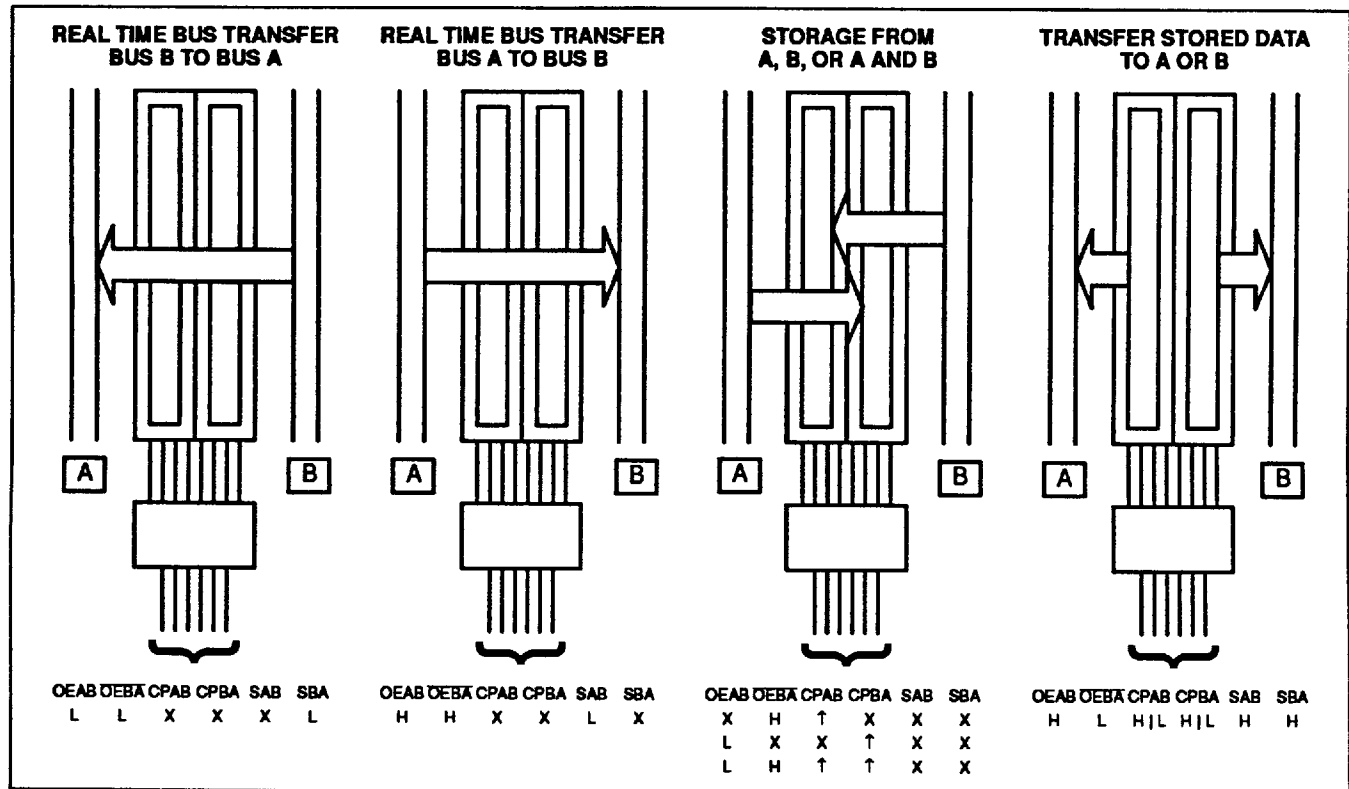
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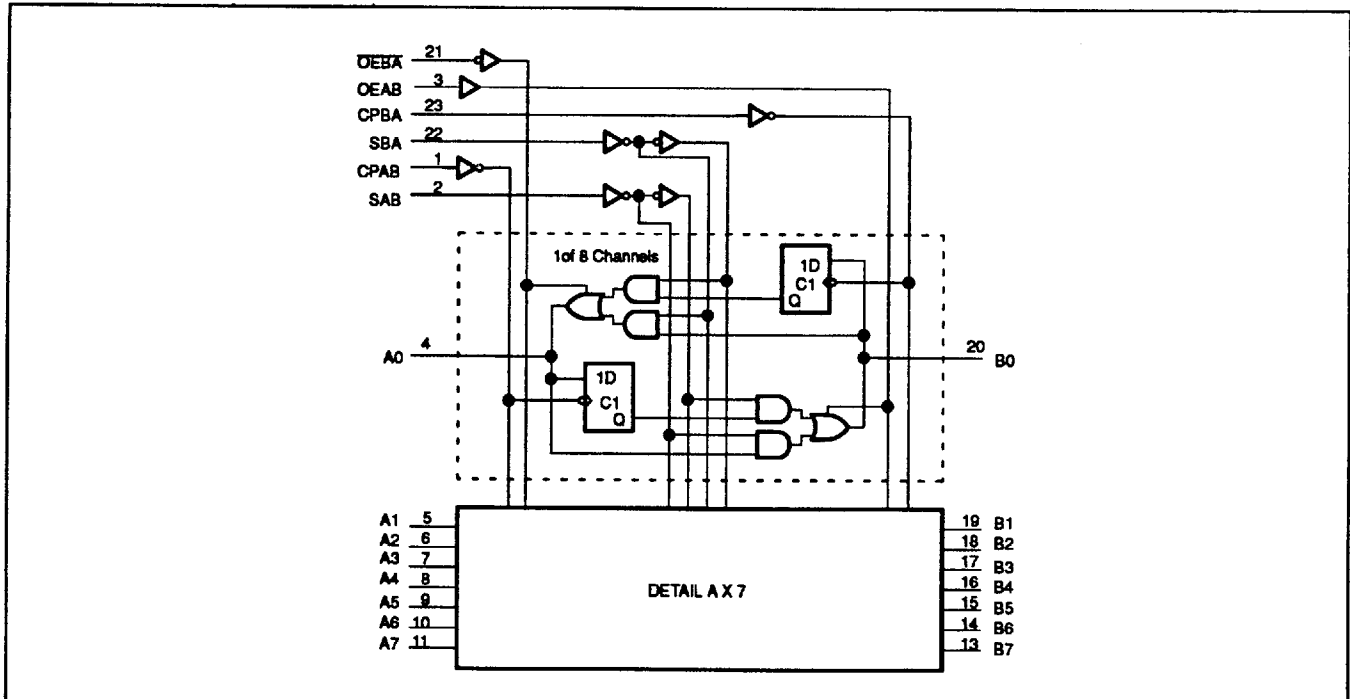
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT652.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1,2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1$ kHz		64	
$\Delta V/\Delta t$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = -18mA				-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = -100μA		V _{CC} -0.2			V
		V _{CC} = 2.7V; I _{OH} = -8mA		2.4			
		V _{CC} = 3.0V; I _{OH} = -32mA		2.0			
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA				0.2	V
		V _{CC} = 2.7V; I _{OL} = 24mA				0.5	
		V _{CC} = 3.0V; I _{OL} = 16mA				0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA				0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA				0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins			±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V				10	
		V _{CC} = 3.6V; V _I = 5.5V	Data pins ⁴			20	
		V _{CC} = 3.6V; V _I = V _{CC}				1	
		V _{CC} = 3.6V; V _I = 0				-5	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V				±100	μA
I _{HOLD}	Bus Hold current A or B ports	V _{CC} = 3V; V _I = 0.8V		75			μA
		V _{CC} = 3V; V _I = 2.0V		-75			μA
I _{EX}	Current into an ouptut in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.7 to 3.3V				100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.13	0.19	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			3	12	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0			0.13	0.19	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND				0.2	mA
I _{PUPD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = X				±100	μA
C _I	Input capacitance	V _I = 3V or 0			4.5		pF
C _O	Output capacitance	V _O = 3V or 0			11		pF

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.3V with a transition time of up to 10msec. From $V_{CC} = 1.3V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100µsec is permitted. X = Don't care.
4. Unused pins at V_{CC} or GND.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
f_{MAX}	Maximum clock frequency	1					MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1		3.7 3.7			ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2		2.8 2.6			ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	3		3.7 4.0			ns
t_{PZH} t_{PZL}	Output enable time OEBA to An	5 6		2.9 3.0			ns
t_{PHZ} t_{PLZ}	Output disable time OEBA to An	5 6		3.9 3.2			ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	5 6		3.3 3.4			ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	5 6		4.5 3.8			ns

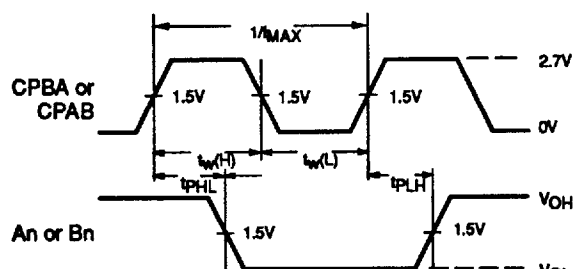
NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

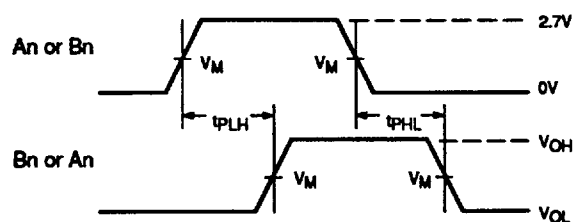
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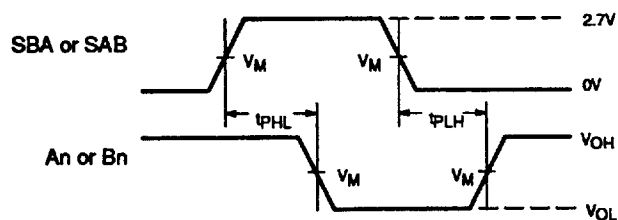
AC WAVEFORMS

 $V_M = 1.5V$, $V_{IN} = GND$ to $2.7V$ 

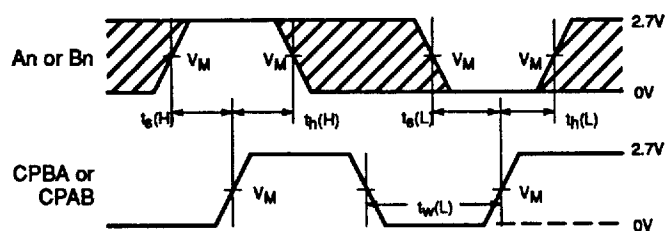
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



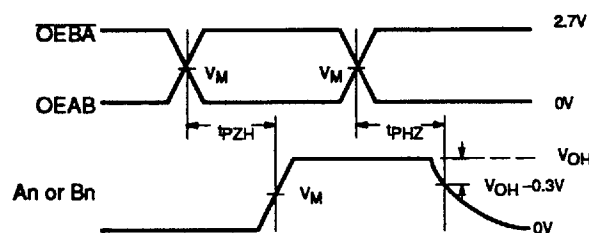
Waveform 2. Propagation Delay, An to Bn or Bn to An



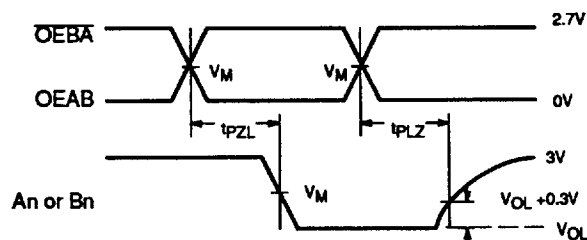
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



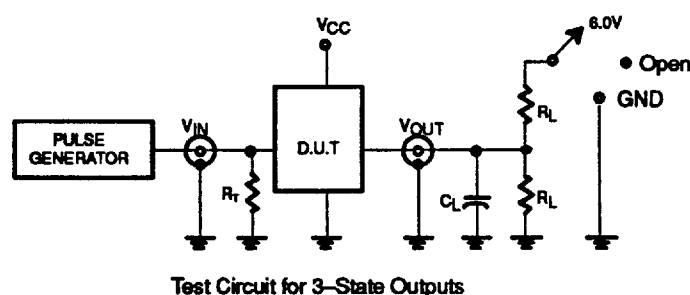
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORM



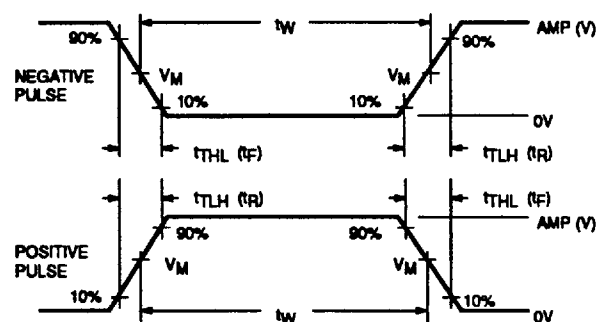
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$