

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ Max}$	I_D $T_A = +25^\circ\text{C}$
60V	40m Ω @ $V_{GS} = 10\text{V}$	5.0A
	55m Ω @ $V_{GS} = 4.5\text{V}$	4.4A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power Management Functions
- Backlighting

Features and Benefits

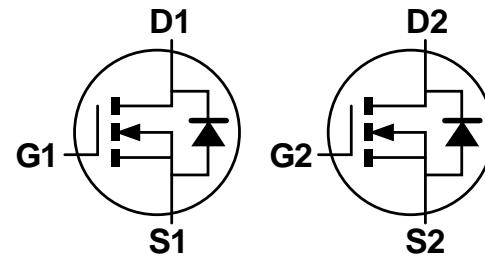
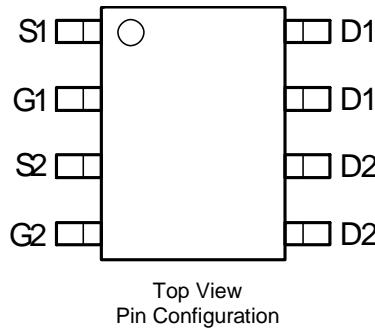
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability
- PPAP Capable (Note 4)

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (Approximate)



Top View



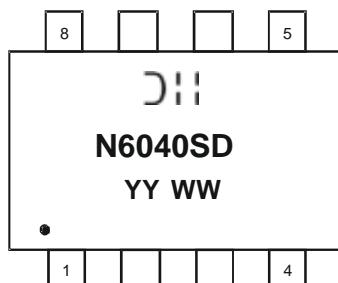
Ordering Information (Note 5)

Part Number	Case	Packaging
DMN6040SSDQ-13	SO-8	2,500/Tape & Reel

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to http://www.diodes.com/product_compliance_definitions.html
5. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



DII = Manufacturer's Marking
 N6040SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 16 = 2016)
 WW = Week (01 – 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$ unless otherwise specified)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 7) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	5.0 4.1	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	6.6 5.3	A
Maximum Body Diode Forward Current (Note 7)			I_S	2.5	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	30	A
Pulsed Body Diode Forward Current (10 μs pulse, duty cycle = 1%)			I_{SM}	30	A
Avalanche Current (Note 8) $L = 0.1\text{mH}$			I_{AS}	14.2	A
Avalanche Energy (Note 8) $L = 0.1\text{mH}$			E_{AS}	10	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$ unless otherwise specified)

Characteristic			Symbol	Value	Units
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$		P_D	1.3	W
	$T_A = +70^\circ\text{C}$			0.8	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		$R_{\theta JA}$	102	$^\circ\text{C/W}$
	$t < 10\text{s}$			61	
Total Power Dissipation (Note 7)	$T_A = +25^\circ\text{C}$		P_D	1.7	W
	$T_A = +70^\circ\text{C}$			1.1	
Thermal Resistance, Junction to Ambient (Note 7)	Steady State		$R_{\theta JA}$	75	$^\circ\text{C/W}$
	$t < 10\text{s}$			50	
Thermal Resistance, Junction to Case (Note 7)	$R_{\theta JC}$			14.5	
Operating and Storage Temperature Range	T_J, T_{STG}			-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	100	nA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	30	40	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 4.5\text{A}$
		—	35	55		$V_{GS} = 4.5\text{V}, I_D = 3.5\text{A}$
Forward Transfer Admittance	$ Y_{FS} $	—	4.5	—	S	$V_{DS} = 10\text{V}, I_D = 4.3\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{ISS}	—	1,287	—	pF	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{OSS}	—	57	—		
Reverse Transfer Capacitance	C_{RSS}	—	44	—		
Gate Resistance	R_G	—	1.2	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_G	—	22.4	—		
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_G	—	10.4	—	nC	$V_{DS} = 30\text{V}, I_D = 4.3\text{A}$
Gate-Source Charge	Q_{GS}	—	4.9	—		
Gate-Drain Charge	Q_{GD}	—	3.0	—		
Turn-On Delay Time	$t_{D(ON)}$	—	6.6	—	ns	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}, R_G = 6\Omega, I_D = 4.3\text{A}$
Turn-On Rise Time	t_R	—	8.1	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	20.1	—		
Turn-Off Fall Time	t_F	—	4.0	—		
Body Diode Reverse Recovery Time	t_{RR}	—	18	—	ns	$I_S = 4.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{RR}	—	11.9	—	nC	$I_S = 4.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$

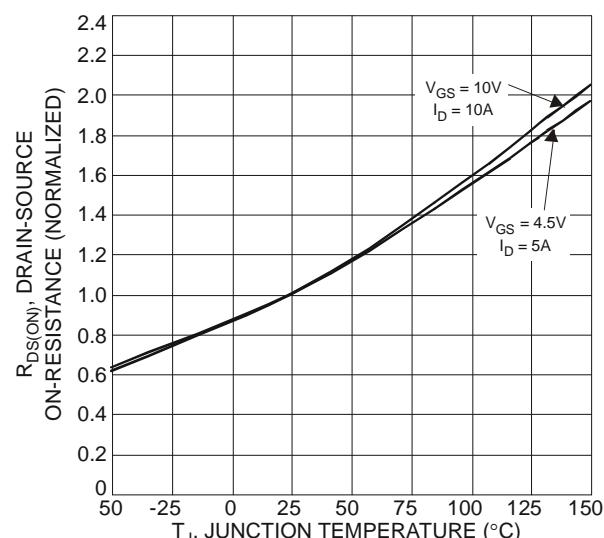
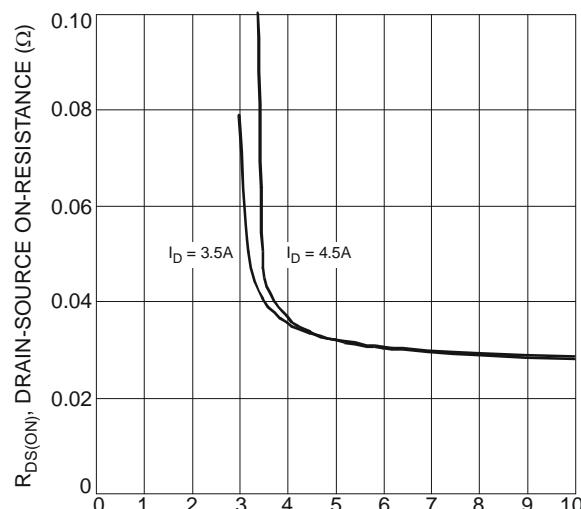
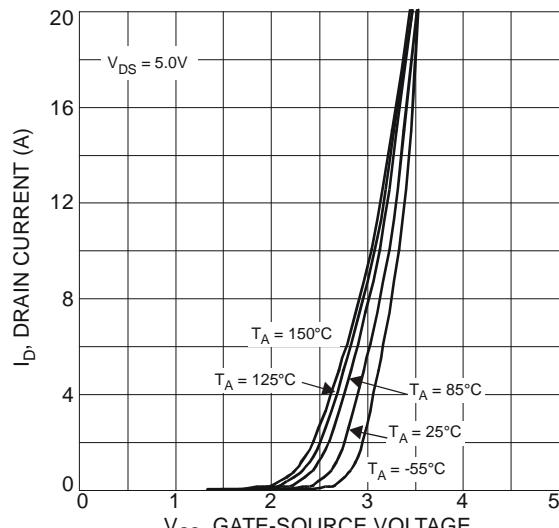
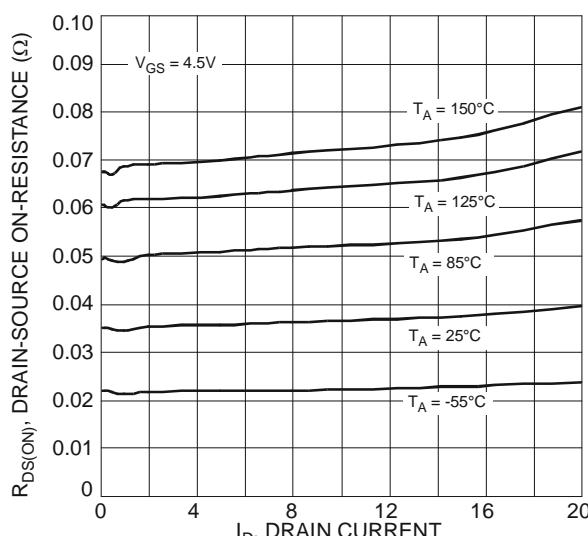
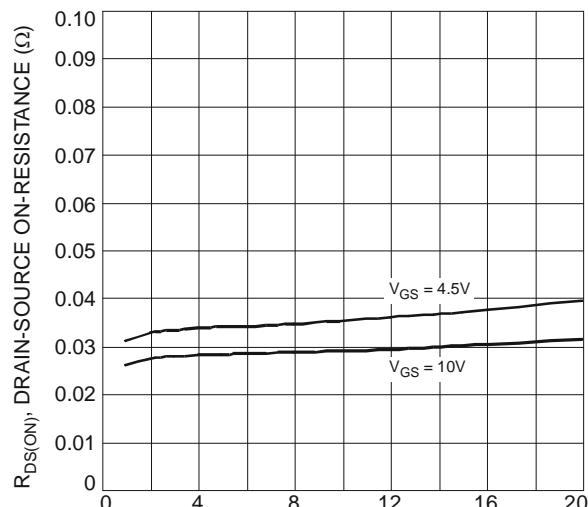
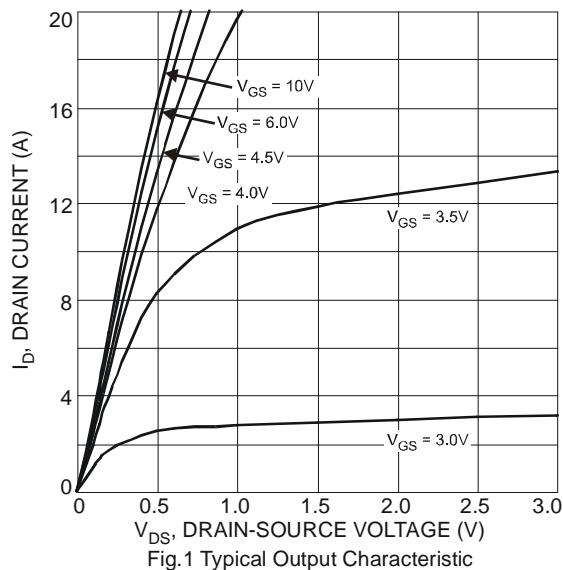
Notes: 6. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.

7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.

8. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.

9. Short duration pulse test used to minimize self-heating effect.

10. Guaranteed by design. Not subject to product testing.



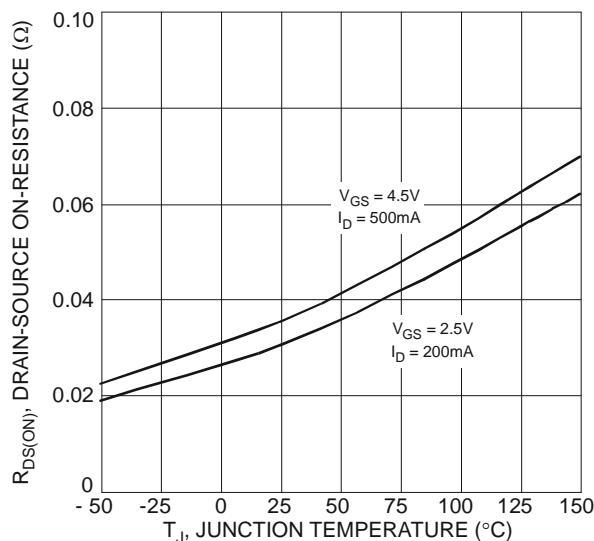


Fig. 7 On-Resistance Variation with Temperature

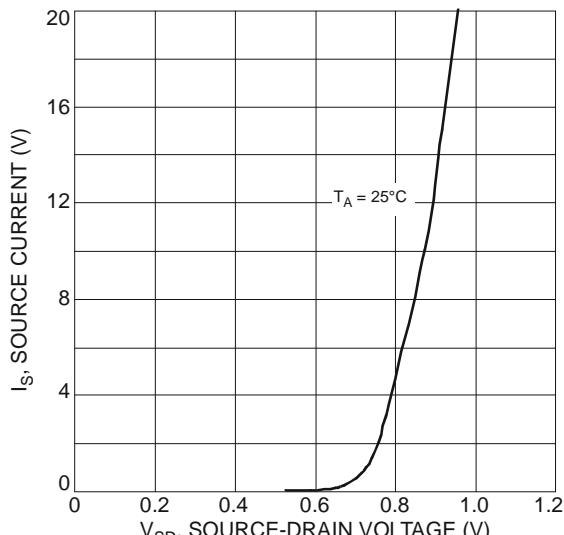


Fig. 9 Diode Forward Voltage vs. Current

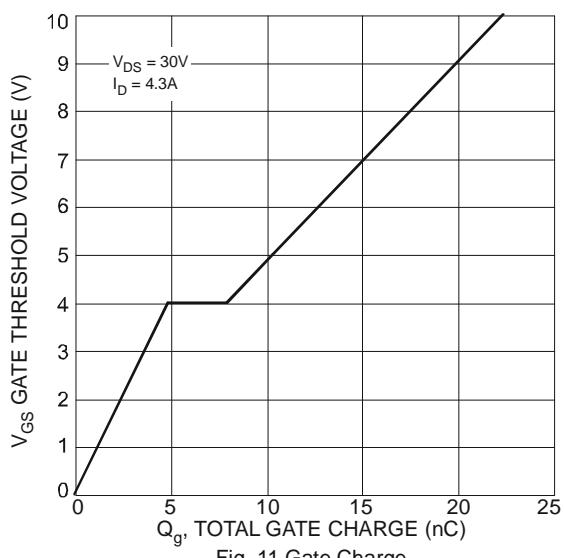


Fig. 11 Gate Charge

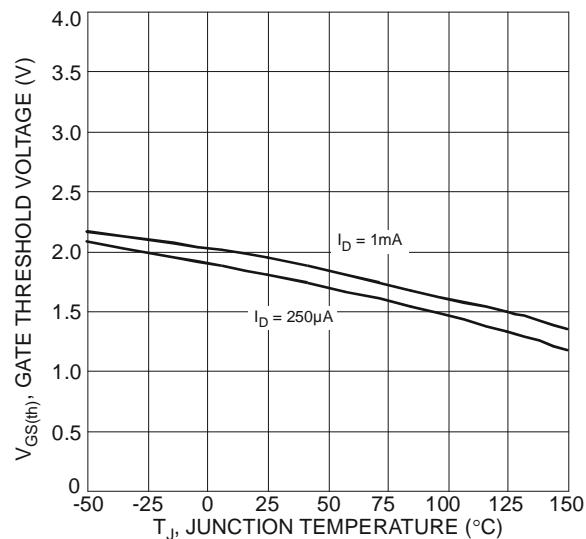


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

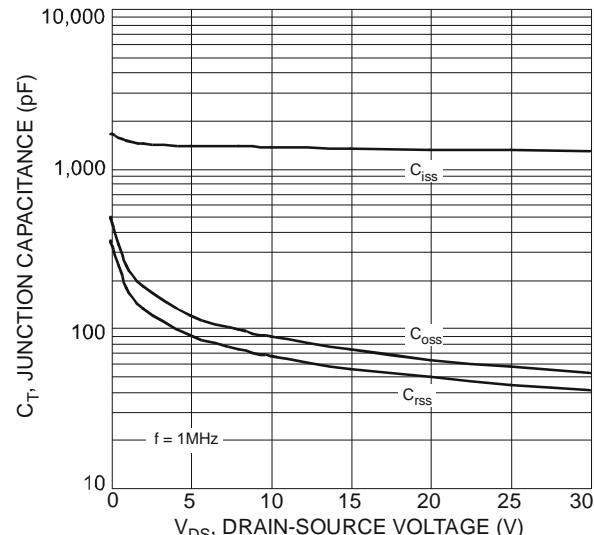


Fig. 10 Typical Junction Capacitance

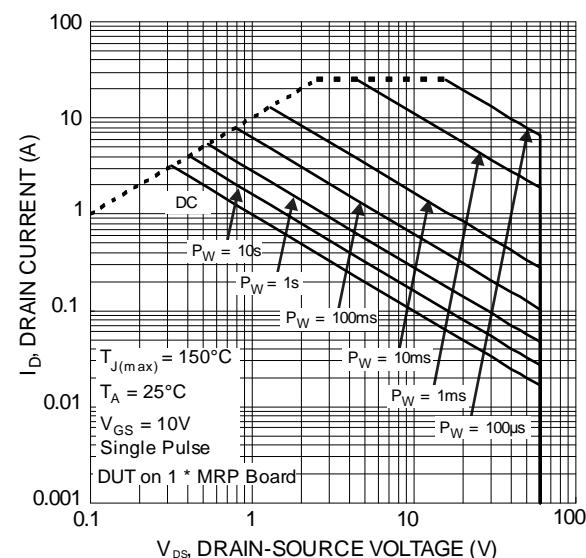


Fig. 12 SOA, Safe Operation Area

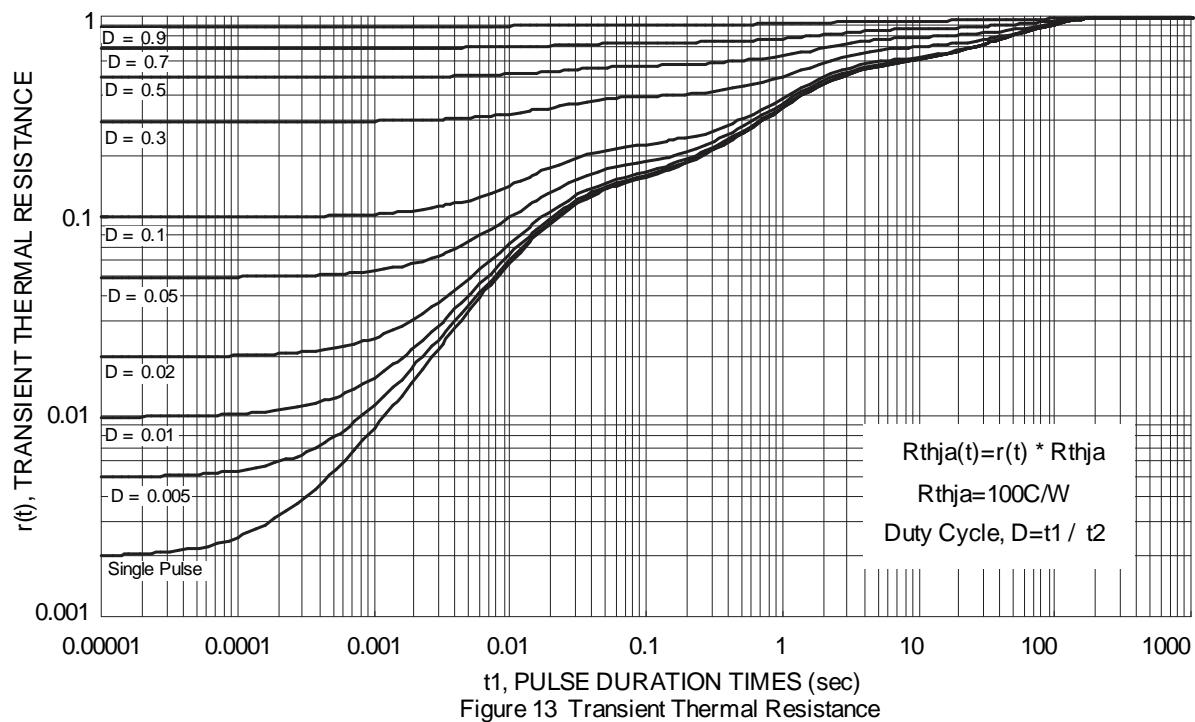
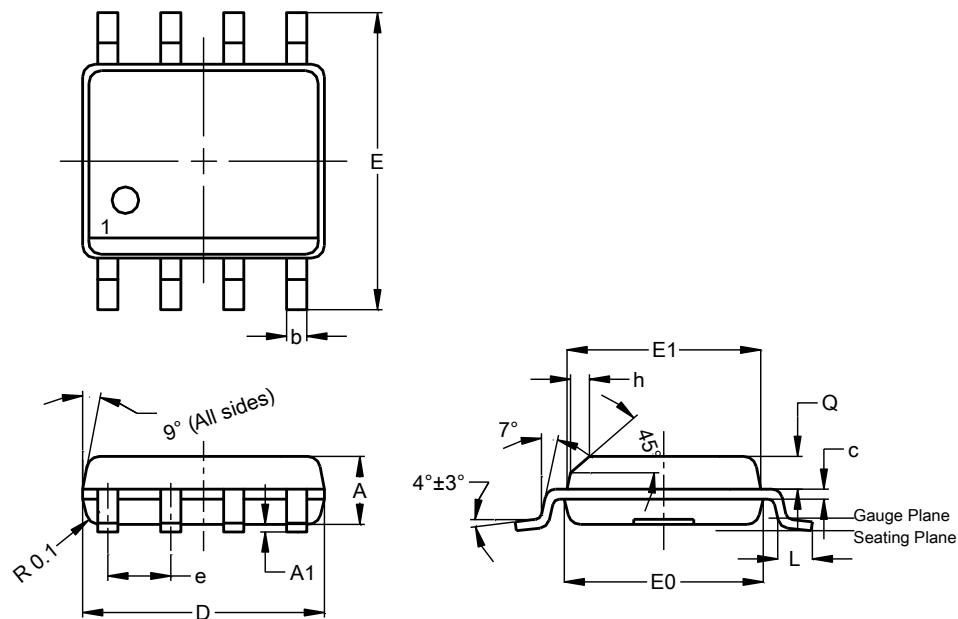


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



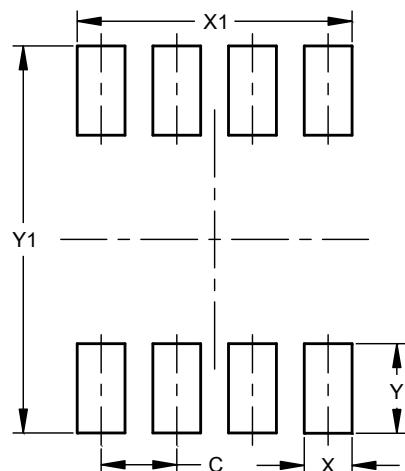
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Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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